Strained-SiGe Complementary MOSFETs Adopting Different Thicknesses of Silicon Cap Layers for Low Power and High Performance Applications

Bongki Mheen, Young-Joo Song, Jin-Young Kang, and Songcheol Hong

We introduce a strained-SiGe technology adopting different thicknesses of Si cap layers towards low power and high performance CMOS applications. By simply adopting 3 and 7 nm thick Si-cap layers in n-channel and p-channel MOSFETs, respectively, the transconductances and driving currents of both devices were enhanced by 7 to 37% and 6 to 72%. These improvements seemed responsible for the formation of a lightly doped retrograde high-electron-mobility Si surface channel in nMOSFETs and a compressively strained high-hole-mobility $Si_{0.8}Ge_{0.2}$ buried channel in pMOSFETs. In addition, the nMOSFET exhibited greatly reduced subthreshold swing values (that is, reduced standby power consumption), and the pMOSFET revealed greatly suppressed 1/f noise and gate-leakage levels. Unlike the conventional strained-Si CMOS employing a relatively thick (typically > 2 μm) Si_xGe_{1-x} relaxed buffer layer, the strained-SiGe CMOS with a very thin (20 nm) $Si_{0.8}Ge_{0.2}$ layer in this study showed a negligible self-heating problem. Consequently, the proposed strained-SiGe CMOS design structure should be a good candidate for low power and high performance digital/analog applications.

Keywords: SiGe, strained-Si, strained-SiGe, hetero-structure MOSFET.

Manuscript received Nov. 5, 2004; revised May 16, 2005.

This work was supported by the Ministry of Information and Communication (MIC) of Korea.

Bongki Mheen (phone: +82 42 860 6217, email: mheen@ieee.org), Young-Joo Song (email: yjs10@etri.re.kr), and Jin-Young Kang (email: jykang@etri.re.kr) are with Basic Research Laboratory, ETRI, Daejeon, Korea.

Songcheol Hong (email: schong@kaist.ac.kr) is with the Department of EECS, KAIST, Daejeon, Korea.

I. Introduction

The aggressive device scaling of complementary metal-oxide-semiconductor (CMOS) devices has significantly improved the device's operating speed and power consumption in digital and analog ICs, expanding its application to the RF and optical communication arena where the compound and SiGe bipolar technology have dominated [1], [2]. CMOS scaling, however, is facing a number of obstacles known as short channel effects, making it very difficult to sustain the trend of device performance improvements. To overcome the scaling obstacles in a conventional Si CMOS, channel engineering using Si_xGe_{1-x} layers has been tried and extensively studied [3]-[6]. In the approach, the 4.2% lattice mismatch between Si and Ge has been used to create tensile and/or compressive forces in Si and Si_xGe_{1-x} layers in order to introduce additional performance enhancements, which cannot be achievable by a simple device scaling at the sub-100 nm device feature size. Therefore, as found in the 2003 International Technology Roadmap for Semiconductors, the Si/Si_xGe_{1-x} CMOS is being considered as one of the key emerging CMOS technologies [7].

The performance enhancement in strained-Si/SiGe CMOS devices primarily depends on improved carrier-transport (that is, larger carrier mobility and high-field velocity [8]) in the strained layers, resulting from the energy band splitting and subsequent effective mass reduction [9]. Up to 170% performance enhancements in drain current, maximum transconductance, and field-effect mobility have been reported for the conventional strained-Si MOSFET, which includes a tensile-strained Si channel on a thick Si_xGe_{1-x} relaxed buffer [5].

However, this device structure suffers from the Si_xGe_{1-x} buffer-related problems. The most significant one is the device performance degradation due to self-heating because of the very low thermal conductivity of Si_xGe_{1-x} material. In addition, the immature and expensive Si_xGe_{1-x} buffer technology is known to significantly deteriorate the production yield and cost. As an alternative choice to alleviate the existing problems in the conventional strained-Si CMOS, the strained-Si_xGe_{1-x} CMOS structure employing a very thin Si_xGe_{1-x} layer (< 20 nm) has been widely studied. Nevertheless, device structure optimizations of the strained Si_xGe_{1-x} CMOS and immunity to self-heating have rarely been reported.

In this paper, we introduce a new strained-$Si_{0.8}Ge_{0.2}$ CMOS device structure utilizing different thicknesses of Si-cap layers in n-channel and p-channel MOSFETs, without incorporating a relatively thick Si_xGe_{1-x} buffer. Using the proposed structure, while a compressively strained SiGe epi layer is used for hole mobility enhancement in p-channel MOSFETs, a relatively thick low doped Si-cap layer is used for the electron channel in an n-channel MOSFET to enhance electron mobility by lightly doped retrograde channel effect [10]. This device structure was proven to be easily adopted in a commercial CMOS process without a significant increase of cost. The resultant device performances were investigated after a brief review of the challenges in strained Si and Si_xGe_{1-x} CMOS approaches.

II. Strained-Si vs. Strained-SiGe

The strained-Si technology enhances electron mobility substantially through biaxial tensile strain. Some drawbacks exist, however, and can be summarized as i) low thermal conductivity of Si_xGe_{1-x} (pure Si : $Si_{0.8}Ge_{0.2}$ = 15 : 1), ii) integration difficulties of pMOSFETs (larger than 50% of Ge mole-fraction in the Si_xGe_{1-x} buffer is required to increase hole mobility), iii) significantly larger defect densities in the Si_xGe_{1-x} buffer (>10^4 cm^{-2}), iv) increased junction capacitance and leakage by a high dielectric constant and narrow energy band gap of Si_xGe_{1-x}, and v) cost increase due to the Si_xGe_{1-x} buffer. Even though there are several modifications to the conventional strained-Si technology to alleviate these problems, the poor thermal conductivity is considered as a key obstacle because of the hot electron channel and increased operating temperature of recent ICs. As known, the increased channel temperature degrades the carrier mobility significantly due to lattice scattering, which indeed makes the mobility enhancement in a strained channel meaningless [4]. The much lower thermal conductivity of Si_xGe_{1-x}, compared to pure Si and pure Ge, is known to originate from the mismatch in acoustic impedance between Si and Ge [11]. The thermal conductivity of $Si_{0.8}Ge_{0.2}$ is about 5.1 Wm^{-1} K^{-1}, while the thermal conductivities of Si and Ge are 148 Wm^{-1} K^{-1} and 60 Wm^{-1} K^{-1}, respectively [12]. Considering the Si_xGe_{1-x} buffer layer thickness (> 2 μm) for full relaxations, its influence on the device's self-heating cannot be neglected [13]. Consequently, with a thick Si_xGe_{1-x} buffer, there is no way to prevent device performance degradation due to self-heating, as similarly seen in Si-on-insulator MOSFETs.

Meanwhile, the strained-SiGe CMOS can easily increase the hole mobility through introducing a biaxial compressive strain by simply inserting a very thin (< 20 nm) Si_xGe_{1-x} layer in the conventional Si CMOS structure at a lower cost. The remaining problem in the strained-SiGe design is the electron mobility enhancement in n-channel MOSFETs because the electron effective mass is relatively large in a compressively strained Si_xGe_{1-x} layer [9]. In this study, using different Si-cap layer thicknesses (7 nm for nMOSFET, 3 nm for pMOSFET), both electron and hole mobility enhancements were successfully achieved.

III. Device Fabrication and Measurements

Prior to Si/$Si_{0.8}Ge_{0.2}$/Si hetero-epitaxy, n-well and local oxidation isolation were formed on three *identical* Si substrates using the conventional 0.5 μm Si CMOS process. After opening active areas, Si/$Si_{0.8}Ge_{0.2}$/Si epi-layers were grown on two of the wafers (B08 and B09) by reduced pressure chemical vapor deposition, and one remaining wafer was used as a Si control (B12). A thin Si cap layer was typically required to avoid the segregation and oxidation of Ge during thermal gate oxidation. The epitaxial structures of $Si_{0.8}Ge_{0.2}$ and Si MOSFETs in this study are shown and described in Fig. 1(a) and Table 1, respectively. Unlike the conventional strained-Si device, shown in Fig. 1(b), with a thick Si_xGe_{1-x} buffer (>2 μm), the strained-SiGe had a thin (20 nm) $Si_{0.8}Ge_{0.2}$ layer below the two different Si-cap layers. The gate oxidation in H_2/O_2 ambient at 800°C ($H_2 : O_2 = 2 : 1$) for 12 minutes was done to produce a 7 nm thick gate-oxide. The unconsumed Si-cap layer thicknesses were measured to be 3 and 7 nm for B08 and B09, respectively, using transmission electron microscopy. No strain relaxation of the $Si_{0.8}Ge_{0.2}$ layer was observed after the oxidation. The in-situ phosphorus-doped (> 10^{19} cm^{-3}) poly-Si by reduced pressure chemical vapor deposition at 550°C was used as a gate material. The samples were characterized by an on-wafer test using an HP4156B semiconductor parameter analyzer for DC measurements. The 1/f noise was measured by a set-up using an Agilent E4440A spectrum analyzer with an EG&G 5185 wideband low noise preamplifier for 10 Hz to 1 MHz. The normalized drain current spectral density (S_I/I_d^2) was derived from the fluctuation in drain voltage (V_{ds}) at the bias condition of V_{ds} = – 0.1 V and V_{gs} = V_{th} – 0.7 V. The

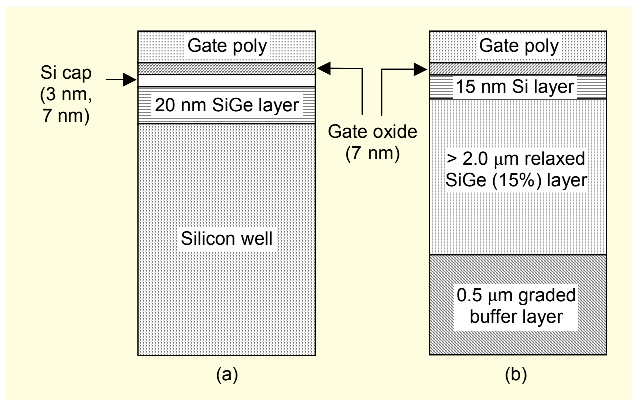

Fig. 1. Structure of (a) strained-Si and (b) strained-SiGe channels.

Table 1. Device species fabricated.

Species		Si cap (nm)	SiGe (nm)	T_{ox} (nm)	Notes
Si	B12	X	X	7	Conventional Si MOSFET
$Si_{0.8}Ge_{0.2}$	B08	4	20	7	Standard strained-SiGe MOSFET
	B09	7	20	7	B08 with approx. 3 nm thicker Si cap

number of averages used in the 1/f noise measurement was 50. All measurements were performed at room temperature.

IV. Results and Discussion

Prior to detailed device characterization, self-heating properties of the $Si_{0.8}Ge_{0.2}$ CMOS were estimated by measuring the device's current-voltage (IV) characteristics both in DC (duty = 99%) and pulsed mode (duty = 1%), as shown in Fig. 2. Contrary to the reported self-heating problem in strained-Si MOSFETs [13], the pulsed IV behavior was nearly the same as in DC IV, ignoring a little deviation due to measurement noise. This indicates that the thin $Si_{0.8}Ge_{0.2}$ layer (20 nm) was sufficiently thin to emit the electron thermal energy in the channel to silicon substrates. This shows that the strained-$Si_{0.8}Ge_{0.2}$ CMOS in this study had negligible self-heating problems during device operation.

As shown in Fig. 3 and Table 2, the strained-$Si_{0.8}Ge_{0.2}$ CMOS with a thinner Si-cap layer (B08) exhibited the increased transconductance and driving current for the pMOSFET case, while the nMOSFET showed degraded properties, compared with the standard Si CMOS (B12). To investigate the carrier (electron) distribution in $Si_{0.8}Ge_{0.2}$ nMOSFETs in this study, device simulations using SILVACO were conducted at the given gate bias. Figure 4 illustrates the conduction band profile of both $Si_{0.8}Ge_{0.2}$ devices. As seen, the conduction band offset due to the $Si_{0.8}Ge_{0.2}$ layer was negligible

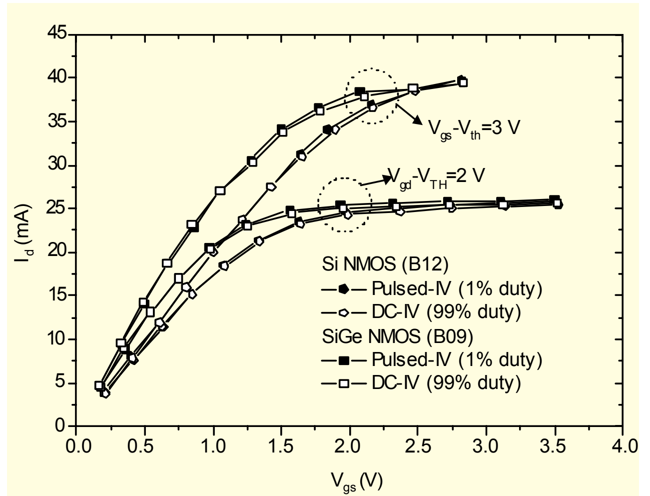

Fig. 2. Comparison of DC- and pulsed-IV characteristics of strained-$Si_{0.8}Ge_{0.2}$ nMOSFET.

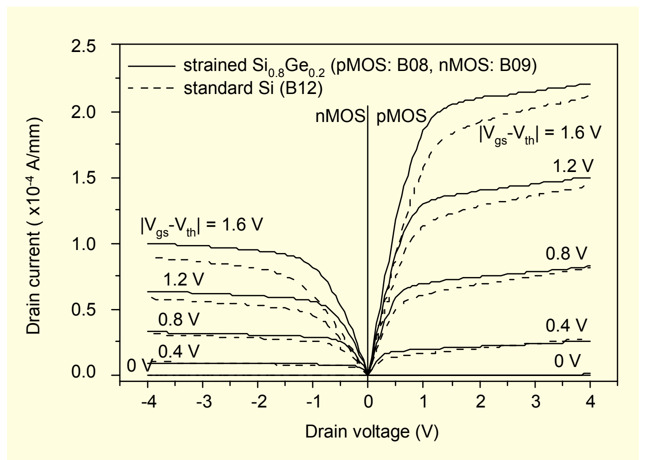

Fig. 3. IV characteristics of Si (B12) and strained-SiGe (B08) channel CMOS devices measured at equivalent V_{gs}.

because of its similar electron affinity value to that of the Si (thus, the band offset mainly occurs in a valence band). We found that more than 50% of the carriers existed in the $Si_{0.8}Ge_{0.2}$ layer for a device with a thinner oxide (B08), whereas less than 15% of those existed in the layer for a device with a thicker oxide (B09). This implies that the Si-cap layer thickness of 3 nm in the $Si_{0.8}Ge_{0.2}$ nMOSFET was not thick enough to include most of the inversion layer carriers in the Si-cap layer, which in turn indicates that electrons partially flow through the lower-electron-mobility region (electron mobility tends to degrade in a compressively strained $Si_{0.8}Ge_{0.2}$ layer [9]).

The resultant transconductance reduction was 12%. However, by increasing the unconsumed Si-cap layer thickness from 3 to 7 nm in the sample B09, the transconductance of the nMOSFET was increased from 1.5 to 1.83 mS (a 22% improvement). This reflected that the 7 nm thick Si-cap layer

Table 2. DC characteristics of Si and $Si_{0.8}Ge_{0.2}$ channel devices.

Type	Parameters		Unit	Si	$Si_{0.8}Ge_{0.2}$	
				B12	B08	B09
NMOS	gm (sat.)		mS	1.71	1.50	1.83
	DIBL		mV/V	36.69	10.45	12.52
	S.S.	V_{ds}=0.1V	mV/dec	72.0	72.1	69.5
		V_{ds}=3.0V		80.5	71.5	68.3
	I_d (sat.)		mA	5.82	4.81	6.18
PMOS	gm (sat.)		mS	0.73	1.00	0.72
	DIBL		mV/V	19.31	4.69	10.45
	S.S.	V_{ds}=0.1V	mV/dec	75.8	82.8	83.0
		V_{ds}=3.0V		73.4	82.4	81.7
	I_d (sat.)		mA	1.45	2.50	1.61

DIBL: drain induced barrier lowering, S.S.: sub-threshold slope

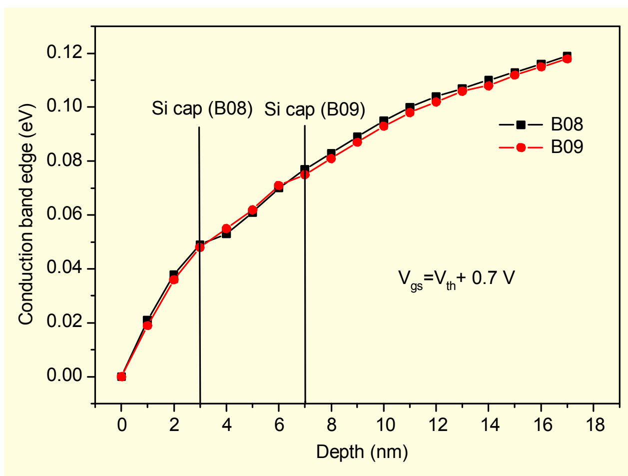

Fig. 4. Electron distribution in $Si_{0.8}Ge_{0.2}$ nMOSFETs resulted from SILVACO device simulation.

could be used as a high-electron-mobility channel, which enhanced its transconductance value even superiorly to the standard Si nMOSFET (a 7% improvement). The transconductance enhancement in the $Si_{0.8}Ge_{0.2}$ device with a thicker Si-cap layer over the standard Si device could be explained by the more lightly-doped channel in the device (that is, the impurity scattering is reduced) rather than the possible tensile-strained enhanced electron mobility by the SiGe epitaxial layer. The secondary ion mass depth profile of boron concentrations for sample B09 in Fig. 5 explained that the $Si_{0.8}Ge_{0.2}$ layer in the device acted as an effective boron diffusion barrier [14], preventing boron out-diffusion into the Si-cap layer during epitaxy and subsequent annealing processes. This device design concept was similar to that of the

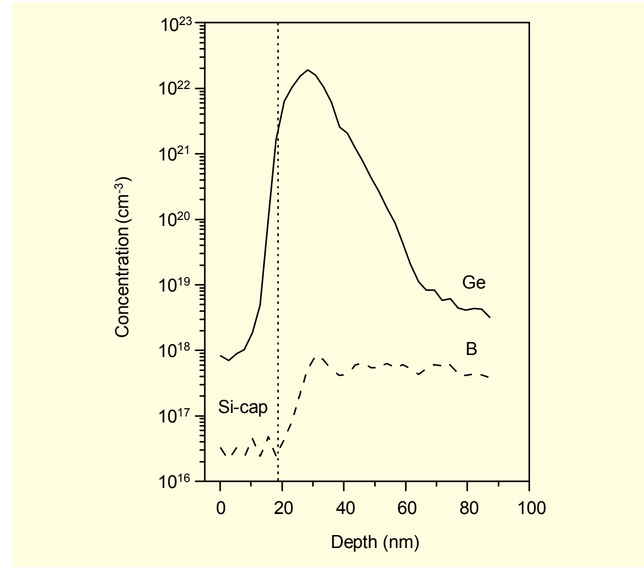

Fig. 5. SIMS depth profile of boron concentrations in n-channel MOSFET using $Si_{0.8}Ge_{0.2}$ epitaxial layer.

Si MOSFET with a retrograde structure [10], in which a specially formed lightly-doped channel could minimize both impurity scattering and short channel effects.

In pMOSFET cases, it is well known that a compressively strained SiGe channel increases hole mobility [9], and this was also verified in this study such that the device's transconductance was enhanced from 0.73 mS (B12) to 1.0 mS (B08, a 37% improvement). Using a thicker Si-cap layer (B09), the transconductance was not enhanced significantly in this experiment because it is too far to affect the holes in the SiGe valence band offset (that is, the hole density in the SiGe layer is reduced). Consequently, by simply applying 7 and 3 nm of Si-cap thicknesses to n-channel and p-channel MOSFETs, respectively, the transconductance could be enhanced by 7 and 37%, when compared with those of the standard Si CMOS.

The subthreshold characteristics of $Si_{0.8}Ge_{0.2}$ and Si CMOS are shown in Fig. 6. It shows that the subthreshold swing in $Si_{0.8}Ge_{0.2}$ nMOSFETs is reduced to 70 mV/dec nearly independent of V_{ds}, which results in standby power consumption reduction in digital applications because the leakage current in higher supply voltage can be reduced substantially. This attributes to the lightly-doped channel (retrograde structure), resulting in the channel carrier confinement, which is supposed to reduce junction leakage currents when the device is operated in the subthreshold regime. Meanwhile, the subthreshold swing of the $Si_{0.8}Ge_{0.2}$ pMOSFET was slightly degraded because the inversion-charge centroid was further away from the gate (buried channel) [9]. However, the drain-induced barrier lowering in the $Si_{0.8}Ge_{0.2}$ pMOSFETs is improved to 4.69 mV/V, while that in Si-control is 19.31 mV/V, because of the channel confinement

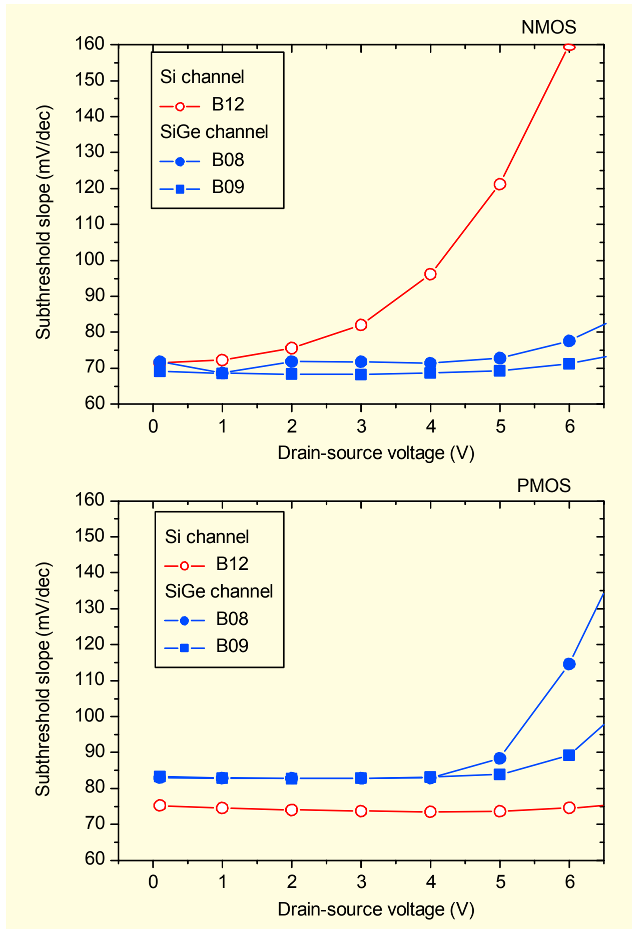

Fig. 6. Sub-threshold slope of strained-SiGe and strained-$Si_{0.8}Ge_{0.2}$ CMOS devices.

effect as proposed in the simulation results [15].

The low frequency noise (1/f noise) and gate leakage current properties in $Si_{0.8}Ge_{0.2}$ and Si pMOSFETs were measured and compared in Figs. 7(a) and 7(b), respectively. The low frequency noise (normalized drain current noise level) in the $Si_{0.8}Ge_{0.2}$ device was reduced by about 1/100 [16], compared with that in the Si device even though the measurement was limited by a system noise limitation below 10 kHz. Judged from the fact that the 1/f noise magnitude was reduced while the slope was sustained, it could be thought that the 1/f noise mechanism was not changed and only the effective defect density was reduced. This improvement may be explained by two main reasons. One reason is due to the hole confinement in the $Si_{0.8}Ge_{0.2}$ buried channel, which separates the channel charge from the oxide traps at the gate oxide surface [17]. Since the probability of direct tunneling is known to be low even at a 1 nm thick unconsumed Si-cap thickness [14], the 3 nm thick Si cap is sufficient to prevent the direct tunneling to the oxide traps. The other reason is the reduction of effective oxide trap density [18], because the involved oxide-trap density close

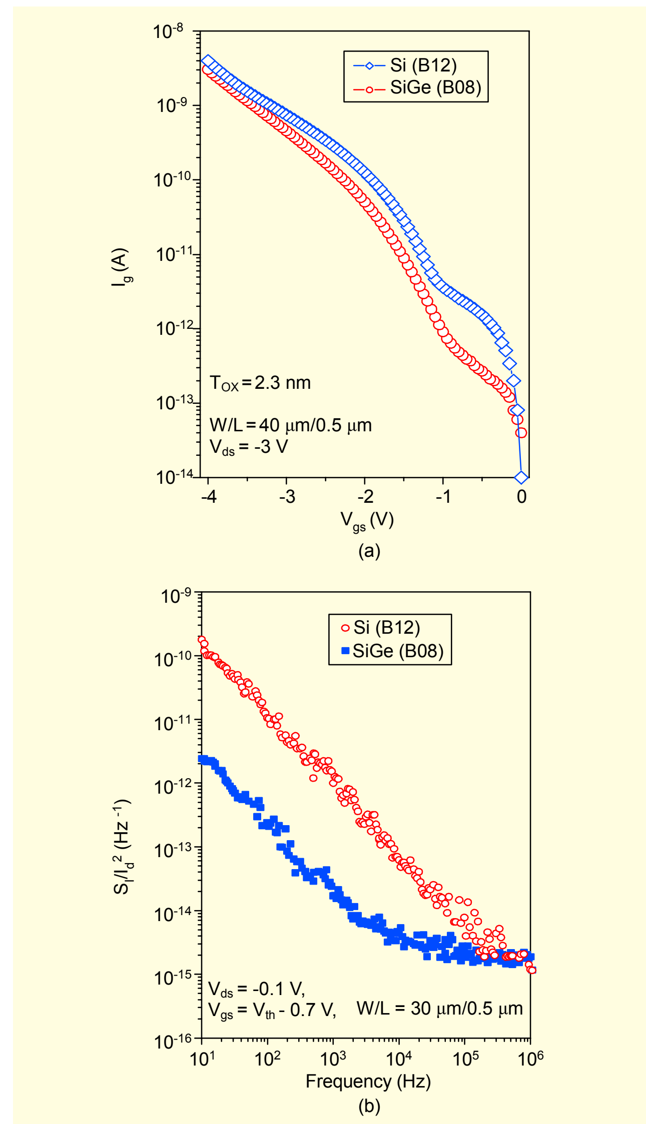

Fig. 7. Properties of (a) 1/f noise and (b) gate leakage in a strained-$Si_{0.8}Ge_{0.2}$ pMOSFET.

to the Fermi level is much lower in the $Si_{0.8}Ge_{0.2}$ pMOSFET by larger displacement of the hole quasi-Fermi level from the valence band edge at the oxide interface. Additionally, the enhanced transconductance also contributes to reduction of the normalized drain current noise level. Actually, the low frequency noise is one of the formidable problems in device scaling because the current noise spectral density can be increased by about more than a factor of L^{-3} as the gate length is shrunken [19]. Considering that the 1/f noise mainly affects the knotty design problems such as DC offsets in direct-conversion receivers, the reduced 1/f noise is expected to relieve the design constraints. The gate leakage current was also reduced over 0.3 at the direct tunneling regime because of the buried hole channel due to the valence band offset, as

shown in Fig. 7(b).

Finally, Figs. 8(a) through 8(d) illustrate one of the possible device fabrication sequences that selectively reduce the Si-cap layer thickness for pMOSFET.

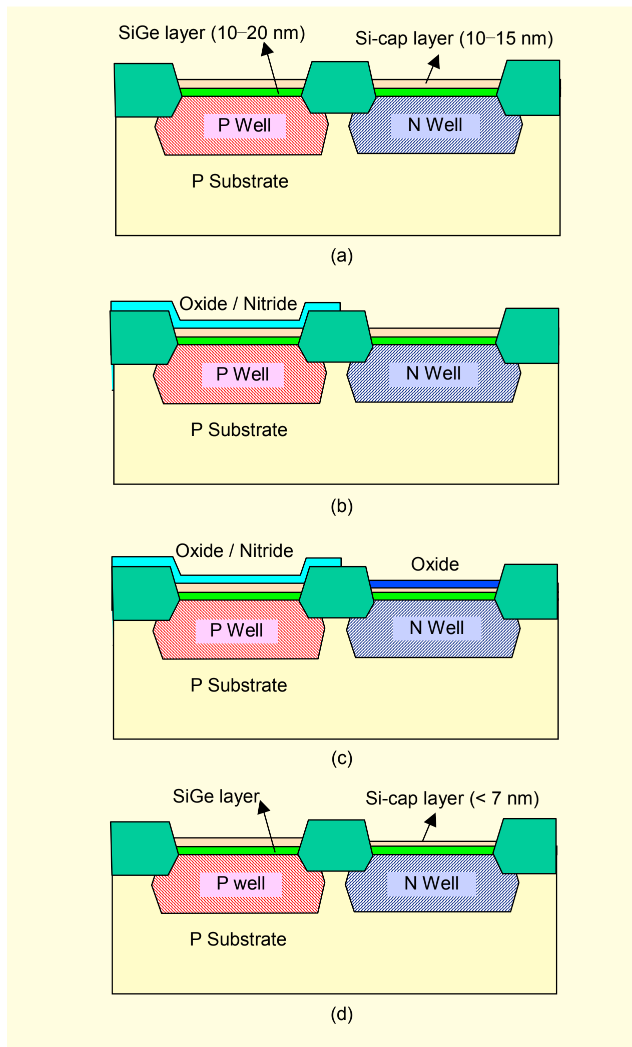

Fig. 8. Illustrative device fabrication sequences accommodating the difference in Si-cap layer thickness for nMOSFET and pMOSFET, simultaneously: (a) selective epitaxial growth of SiGe (10–20 nm) and Si-cap (10–15 nm) layers on active regions, (b) oxide/nitride deposition and active area opening in n-well region, (c) selective oxidation of the Si-cap layer for pMOSFETs, and (d) oxide/nitride removing.

V. Conclusion

In this paper, strained-SiGe complementary MOSFETs using different Si-cap layer thicknesses were proposed and fabricated for low power and high performance applications. Unlike the strained-Si devices which suffer from a self-heating problem, the proposed strained-SiGe CMOS devices with different Si-cap layers improved transconductance, leakage power, and 1/f noise without self-heating or significant increase of fabrication cost. By simply inserting a strained-SiGe epitaxial layer in the conventional CMOS structure, the transconductance of n-channel and p-channel MOSFETs are enhanced by 7 and 37%, respectively, compared with conventional Si CMOS devices, with several enhancements (lower drain leakage current, lower 1/f noise, and lower gate leakage current). This indicates that high-performance and low power properties can be achieved by the present strained-SiGe CMOS technology towards advanced digital/analog applications.

References

[1] Seok-Bong Hyun, Geum-Young Tak, Sun-Hee Kim, Byung-Jo Kim, Jinho Ko, and Seong-Su Park, “A Dual-Mode 2.4-GHz CMOS Transceiver for High-Rate Bluetooth Systems,” *ETRI J.*, vol. 26, no. 3, 2004, pp. 229-240.

[2] Cheon Soo Kim, Sung Do Kim, Mun-Yang Park, and Hyun-Kyu Yu, “Trenched-Sinker LDMOSFET (TS-LDMOS) Structure for 2 GHz Power Amplifiers,” *ETRI J.*, vol. 25, no. 3, June 2003, pp. 195-202.

[3] S. Verdonckt-Vandebroek, E.F. Crabbe, B.S. Meyerson, D.L. Harame, P.J. Restle, J.M.C. Stork, and J.B. Johnson, “SiGe-Channel Heterojunction p-MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 41, no. 1, Jan. 1994, pp. 90-101.

[4] Jung-Suk Goo Qi Xiang Takamura, Y. Arasnia, F. Paton, E.N. Besser, P. Pan, and J. Ming-Ren Lin, “Band Offset Induced Threshold Variation in Strained-Si nMOSFETs,” *Electron Device Lett.*, vol. 24, no. 9, 2003, pp. 568-570.

[5] S.H. Olsen, A.G. O'Neill, L.S. Driscoll, K.S.K. Kwa, S. Chattopadhyay, A.M. Waite, Y.T. Tang, A.G.R. Evans, D.J. Norris, A.G. Cullis, D.J. Paul, and D.J. Robbins, “High-Performance nMOSFETs Using a Novel Strained Si/SiGe CMOS Architecture,” *IEEE Trans. Electron Devices*, vol. 50 , no. 9, 2003, pp. 1961-1969.

[6] J.G. Fossum and Weimin Zhang, “Performance Projections of Scaled CMOS Devices and Circuits with Strained Si-on-SiGe Channels,” *IEEE Trans. Electron Devices*, vol. 50, no. 4, 2003, pp. 1042-1049.

[7] The International Technology Roadmap for Semiconductor 2003.

[8] M.V. Fischetti and S.E. Laux, “Band Structure, Deformation Potentials, and Carrier Mobility in Strained Si, Ge, and SiGe Alloys,” *J. of Applied Physics*, vol. 80, no. 4, 1996, pp. 2234-2252.

[9] Y.-C. Yeo, Q. Lu, T.-J. King, C. Hu, T. Kawashima, M. Oishi, S. Mashiro, and J. Sakai, “Enhanced Performance in Sub-100 nm CMOSFETs Using Strained Epitaxial Silicon-Germanium,” *IEDM Technical Digest.*, 10-13, Dec. 2000, pp. 753-756.

[10] S.T. Ma and J.R. Brews, “Comparison of Deep-Submicrometer Conventional and Retrograde n-MOSFETs,” *IEEE Trans. Electron Devices*, vol. 47, no. 8, 2000, pp. 1573-1579.

[11] D.G. Cahill, W.K. Ford, K.E. Goodson, G.D. Mahan, A. Majumdar, H.J. Maris, R. Merlin, and S.R. Phillpot, "Nanoscale Thermal Transport," *J. Appl. Phys.*, vol. 93, no. 12, 2003, pp. 793-818.

[12] J.P. Dismukes, L. Ekstrom, E.F. Steigmeier, I. Kudman, and D.S. Beers, "Thermal and Electrical Properties of Heavily Doped Ge-Si Alloys up to 1300°K ," *J. Appl. Phys.*, vol. 35, no. 10, 1964, pp. 2899-2907.

[13] K.A. Jenkins and K.Rim, "Measurement of the Effect of Self-Heating in Strained-Silicon MOSFETs," *Electron Device Lett.*, vol. 23, no. 6, 2002, pp. 360-362.

[14] G. Ghibaudo and J. Chroboczek, "On the Origin of the LF Noise in Si/Ge MOSFETs," *Solid State Electron.*, vol. 46, 2002, pp. 393-398.

[15] P.W. Li and W.M. Liao, "Analysis of Si/SiGe Channel pMOSFETs for Deep-Submicron Scaling," *Solid-State Electronics*, vol. 46, 2002, pp. 39-44.

[16] Y-J Song, K-H Shim, J-Y Kang, and K-I Cho, "DC and RF Characteristics of $Si_{0.8}Ge_{0.2}$ pMOSFETs: Enhanced Operation Speed and Low 1/f Noise," *ETRI J.*, vol. 25, no. 3, June 2003, pp. 203-209.

[17] M.J. Palmer, G. Braithwaite, T.J. Grasby, P.J. Phillips, M.J. Prest, E.H.C. Parker, T.E. Whall, C.P. Parry, A. M. Waite, A.G.R. Evans, S. Roy, J.R. Watling, S. Kaya, and A. Asenov, "Effective Mobilities in Pseudomorphic Si/SiGe/Si p-channel Metal-Oxide-Semiconductor Field-Effect-Transistors with Thin Silicon Capping Layers," *Appl. Phys. Lett.*, vol. 78, 2001, pp. 1424-1426.

[18] S.J. Mathew, G. Niu, W.B. Dbbelday, J.D. Cressler, J.A. Ott, J.O. Chu, P.M. Mooney, K.L. Kavanagh, B.S. Meyerson, and I. Lagnado, "Hole Confinement and its Impact on Low-Noise in SiGe pFETs on Sapphire," *IEDM Tech. Dig.*, 1997, pp. 815-818.

[19] Ming-Horn Tsai and Tso-Ping Ma, "The Impact of Device Scaling on the Current Fluctuations in MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 11, 1994, pp. 2061-2068.

Bongki Mheen received the BS degree in electronics from Chungnam National University in 1996, and the MS degree in electronics from Pohang University of Science and Technology (POSTECH) in 2000. He joined Electronics and Telecommunications Research Institute (ETRI) at Daejeon in 2000, and is currently working toward the PhD degree in Korea Advanced of Science and Technology (KAIST). His research interests include Si-based microelectronic devices including SiGe HBT and strained MOSFET, low frequency and high frequency noise, microwave circuit design and its applications including radar systems, and CMOS image sensors.

Young-Joo Song received BS degree in electronic engineering from Sogang University in 1993 and PhD degree in electrical engineering from State University of New York at Buffalo in 2000. He worked for Samsung Electronics Developing Large-Area TFT-LCDs during 2000 to 2001. He is currently working as a Senior Engineer at ETRI. His research includes CMOS Image sensors, TFT-LCDs, strained silicon and germanium channel MOSFETs, and nanotechnology.

Jin-Young Kang received his BS degree in physics and astronomy from Seoul National University in 1975, and the MS and PhD degrees in physics from KAIST in 1979 and 1991. He joined ETRI in 1979. He has been working on the development of Si-based high performance microelectronic devices for wireless telecommunications including SiGe HBT and BiCMOS, and their integrated circuits for RF and high speed digital applications. At present, he is a head of SiGe Devices Section at ETRI-Basic Research Laboratory.

Songcheol Hong received the BS and MS degrees in electronics from Seoul National University, Seoul, Republic of Korea, in 1982 and 1984. He received the PhD degree in electrical engineering from the University of Michigan, Ann Arbor, in 1989. In May 1989, he joined the faculty of Dept. of Electrical Engineering and Computer Science at KAIST. He held short visiting professorships at Stanford University, Palo Alto and Samsung Microwave Semiconductor, USA in 1997. His research interests are microwave integrated circuits and systems including power amplifiers for mobile communications, miniaturized radar, millimeterwave frequency synthesizers, and novel semiconductor devices.