A Low Power Analog CMOS Vision Chip for Edge Detection Using Electronic Switches

Jung-Hwan Kim, Jae-Sung Kong, Sung-Ho Suh, Minho Lee,
Jang-Kyoo Shin, Hong Bae Park, and Chang Auck Choi

An analog CMOS vision chip for edge detection with power consumption below 20 mW was designed by adopting electronic switches. An electronic switch separates the edge detection circuit into two parts: one is a logarithmic compression photocircuit, and the other is a signal processing circuit for edge detection. The electronic switch controls the connection between the two circuits. When the electronic switch is off, it can intercept the current flow through the signal processing circuit and restrict the magnitude of the current flow below several hundred nA. The estimated power consumption of the chip, with 128 × 128 pixels, was below 20 mW. The vision chip was designed using 0.25 μm 1-poly 5-metal standard full custom CMOS process technology.

Keywords: Vision chip, CMOS vision chip, retina chip, edge detection, low power consumption.

I. Introduction

Recently, many researchers have been working on the development of a vision chip using CMOS process technology [1]-[8]. The CMOS vision chip for edge detection is based on the edge detection mechanism of the vertebrate retina. The cells in the retina perform signal processing in analog mode, but they can realize real-time image processing according to parallelism [4]-[9]. If these characteristics of the retina are imitated, the calculation amount will be reduced and real-time image information processing will be accomplished.

It is well known that photoreceptors, horizontal, and bipolar cells in the retina, deal with edge detection from an image. Photoreceptors receive an optical signal and transform it into electrical signals. Horizontal cells spatially smooth the electrical signal of the photoreceptor. Bipolar cells yield the difference between the electrical signal of the photoreceptor and the smoothed signal of the horizontal cell [4]-[8]. Given this mechanism, the edges from an image can be extracted. A vision chip for edge detection consists of an electrical circuit model based on the edge detection mechanism of the retina.

In order to realize an analog CMOS vision chip for edge detection with high resolution, power consumption should be considered. For instance, there was a report that the power consumption of an analog CMOS vision chip with 40 × 46 pixels was 40 mW under power-saving mode [8]. This is an inherent problem in analog mode. If the resolution of the analog CMOS vision chip increases, it will cause power consumption to increase.

In this paper, we propose a 128 × 128 analog CMOS vision chip for edge detection with electronic switches for low power consumption. An edge detection circuit, which is an important

---

Manuscript received Jan. 12, 2005; revised Aug. 31, 2005.

This work was supported by the Brain Science Research Center at KAIST and the BK21 program in Korea. The material in this work was presented in part at IT-SoC 2004, Seoul, Korea, Oct. 2004.

Jung-Hwan Kim (phone: +82 53 940 8631, email: ricehome@ee.knu.ac.kr), Jae-Sung Kong (email: kongjs@ee.knu.ac.kr), and Sung-Ho Suh (email: ssh0823@ee.knu.ac.kr) are with the Department of Electronics, Kyungpook National University, Daegu, Korea.

Minho Lee (email: mholee@knu.ac.kr), Jang-Kyoo Shin (email: jkshin@ee.knu.ac.kr), and Hong Bae Park (email: hbpark@ee.knu.ac.kr) are with the School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, Korea.

Chang Auck Choi (email: cachoi@etri.re.kr) is with Basic Research Laboratory, ETRI, Daejeon, Korea.

element of the vision chip, can be selectively operated according to the state of electronic switches. As a result, power consumption could be minimized below 20 mW, and this milestone was confirmed using SPICE (simulation program with integrated circuit emphasis).

II. Theory and Electrical Circuit Design

Figure 1 shows the principle of an edge detection mechanism. Photoreceptors transform optical signals into electrical signals, while horizontal cells spatially smooth the photoreceptor output. Bipolar cells yield the difference between the output signal of the photoreceptor and the smoothed signal of the horizontal cell.

To realize a vision chip based on the retina, it is necessary to model the cells concerned with edge detection in the retina. An electrical circuit model for edge detection is proposed and shown in Fig. 2.

The logarithmic compression photocircuit is shown in Fig. 2(a), and it acts as a photoreceptor. Figure 2(b) shows the electronic switch that controls the connection between the photocircuits and the signal processing circuits for edge detection. Figure 2(c) is the signal processing circuit for edge detection, which includes horizontal and bipolar cells. The horizontal cell is replaced by a p-MOSFET (M_{P4}), and the bipolar cell is replaced by current mirrors that consist of p-MOSFET (M_{P2} and M_{P3}) and n-MOSFET current mirrors (M_{N1} and M_{N2}).

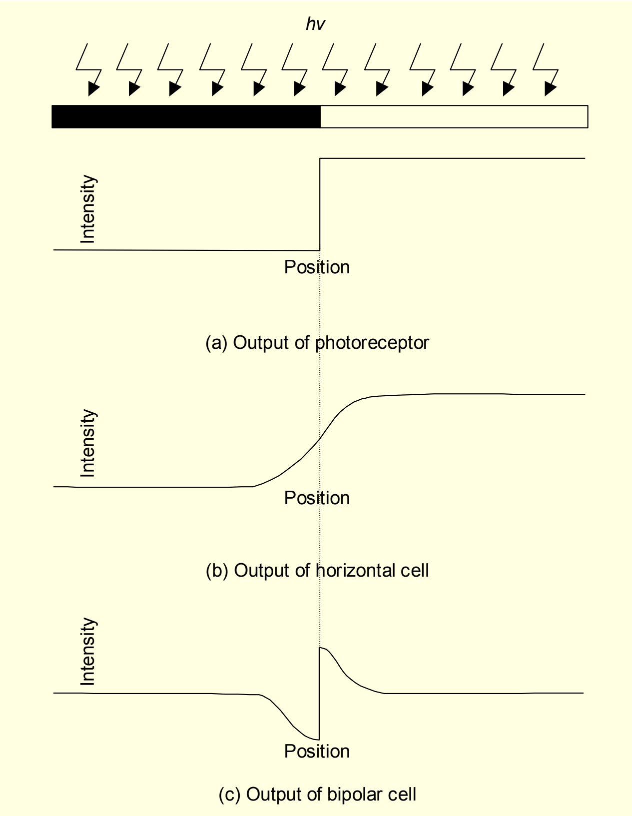

Fig. 1. Principle of edge detection.

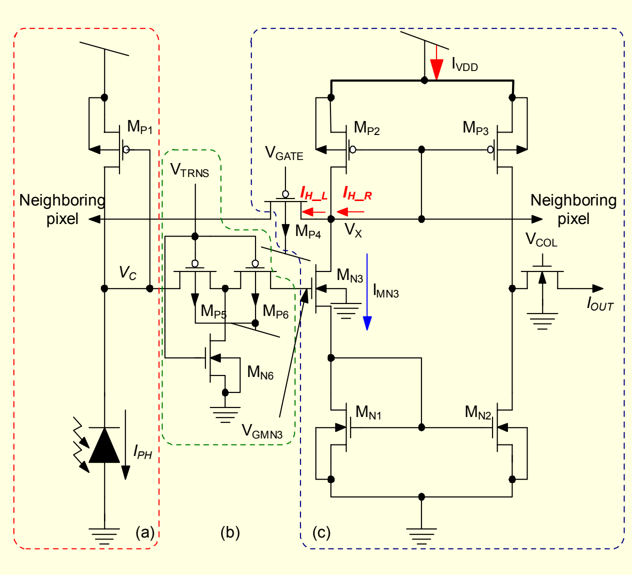

Fig. 2. Electrical retina model.

We consider a one-dimensional array of the pixel circuit and a change of the output with an input photocurrent. As shown in Fig. 2(a), the optical signal through the photodiode is transformed into an electrical signal. If I_{PH} is so low that M_{P1} operates in the subthreshold region, the voltage V_C is logarithmically dependent on the input photocurrent in [10],

$$V_C = V_{DD} - \frac{U_T\, n}{I_{D0}}\frac{L}{W}\ln I_{PH}\,, \qquad (1)$$

where W and L are the width and length of M_{P1}, respectively, U_T is thermal voltage (kT/q), I_{PH} is the input photocurrent, n is the subthreshold slope factor, I_{D0} is a process dependent parameter, and V_C is the output voltage of the logarithmic circuit with the input photocurrent. Voltage V_C decreases with an increasing I_{PH}. We utilize the change of V_C with an input photocurrent to detect edges.

The operational states of the electronic switch, shown in Fig. 2(b), are determined by V_{TRNS}. When V_{TRNS} is connected to the ground, the switch is on (M_{P5} and M_{P6}: on, M_{N6}: off). Voltage V_{GMN3} is equal to V_C and controls I_{MN3}. When there is a current flow of I_{MN3} in the signal processing circuit for edge detection, this circuit begins to detect the edge information. On the other hand, when V_{TRNS} is connected to V_{DD}, the switch is off (M_{P5} and M_{P6}: off, M_{N6}: on). Voltage V_C is no longer concerned with I_{MN3}, and the signal processing circuit for edge detection does not operate. Using this operation, power consumption can be lowered by controlling the operation of the signal processing circuit for edge detection according to the states of the switch. In addition, this electronic switch separates the edge detection circuit into two parts; the edge detection circuit is separated into a 128 × 128 logarithmic compression photocircuit and a 1 × 128 signal processing circuit array for edge detection. This helps in increasing the number of pixels in the vision chip.

As shown in Fig. 2(c), M_{P4} connects the unit pixel circuit to the neighboring pixels and acts just like the horizontal cell. This is the intermediate stage for transmitting the change of I_{H_L} and I_{H_R} with an input photocurrent. The magnitude of output I_{OUT} is determined by the existence or nonexistence of I_{H_L} and I_{H_R}. Output I_{OUT} can be represented by applying Kirchhoff's current law.

$$I_{OUT} = I_{MP3} - I_{MN3} = I_{MP2} - I_{MN2}\,. \qquad (2)$$

As the input light with constant distribution is projected onto the one-dimensional array, we obtain a constant I_{OUT} because there is no current flow of I_{H_L} and I_{H_R} that can affect I_{MP2} due to the constant voltage distribution between the node voltage V_Xs. On the other hand, as the input light with halftone (bright and dark) distribution is projected onto the one-dimensional array, I_{OUT} changes at the neighborhood edge because there are current flows of I_{H_L} and I_{H_R} due to the voltage difference between the voltage V_Xs. Thus, I_{MP2} is changed by I_{H_L} and I_{H_R}. Current I_{OUT} at the boundary of the halftone is represented in (3) and (4).

At the end of the bright light,

$$I_{OUT} = I_{MP3} - I_{MN3} = -I_{H\_R} + I_{H\_L} \quad (|I_{H\_R}| > |I_{H\_L}|)\,. \qquad (3)$$

At the start of the dark light,

$$I_{OUT} = I_{MP3} - I_{MN3} = -I_{H\_R} + I_{H\_L} \quad (|I_{H\_R}| < |I_{H\_L}|)\,. \qquad (4)$$

Output I_{OUT} at the end of the bright light has a negative value because of incoming current I_{H_R}. On the other hand, output I_{OUT} at the start of the dark light has a positive value because of the outflow of current I_{H_L}. That is, we obtain a large peak at the boundary of the halftone.

In this work, a CMOS vision chip with 128 × 128 pixels has been realized, in which a 128 × 128 logarithmic compression photocircuit array uses a common 1 × 128 signal processing circuit array for edge detection. Figures 3 and 4 show the block diagram and layout of an analog CMOS vision chip for edge detection with 128 × 128 pixels, respectively. This chip was designed using 0.25 μm 1-poly 5-metal standard full custom CMOS process technology.

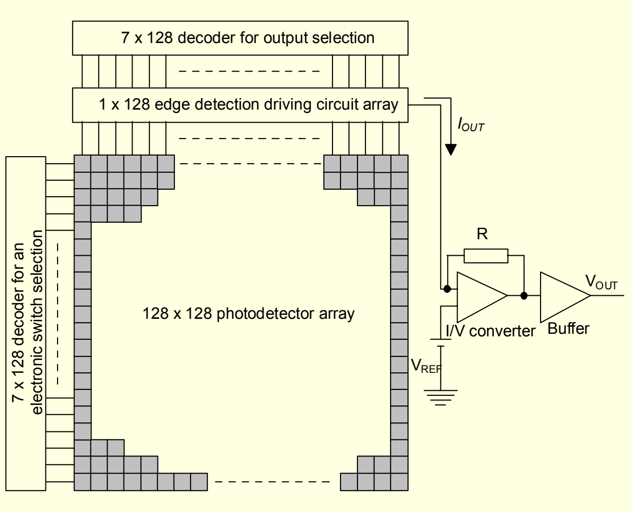

Fig. 3. Block diagram of an analog CMOS vision chip.

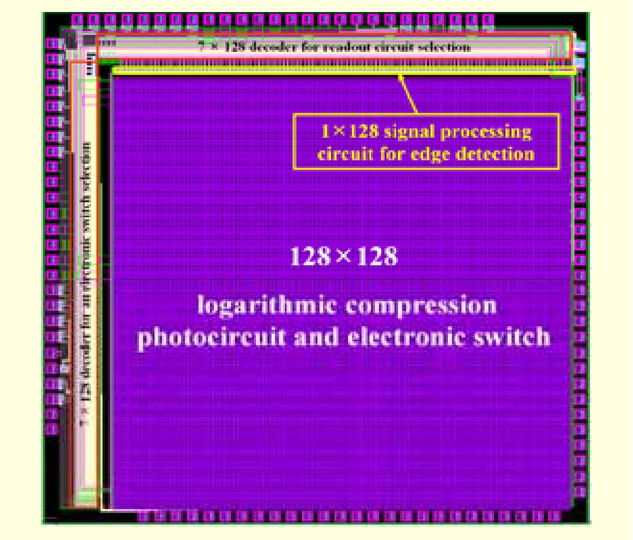

Fig. 4. Whole chip layout.

The final stage consists of a current-to-voltage converter (I/V converter) and an analog buffer. The size of the designed chip is 4 mm × 4 mm. The sizes of the photocircuit and signal processing circuit for edge detection are 27.02 μm × 25.64 μm and 26 μm × 24.35 μm, respectively, which includes a metal wire for interconnection.

III. Simulation Results and Discussion

Figure 5 shows the simulation results of the logarithmic compression photocircuit, shown in Fig. 2(a), with varying input photocurrent levels, I_{PH}. The input photocurrent I_{PH} changed from 0.1 pA to 1 μA on the logarithmical scale. As in (1), we confirm that voltage V_C of the photocircuit decreases with an increase in input photocurrent I_{PH}, which is logarithmically related to I_{PH}.

The transfer characteristics of an electronic switch with varying I_{PH} are shown in Fig. 6. When V_{TRNS} is connected to the ground and I_{PH} varies from 0.1 pA to 1 µA on the logarithmical scale, I_{MN3} has values between 16.1 µA and 4.3 µA according to V_{GMN3}, which is transferred from V_C because voltage V_C decreases with an increasing I_{PH}. When V_{TRNS} is connected to V_{DD}, I_{MN3} is constant at about 160 nA. That is, it is not concerned with input photocurrent I_{PH}. That value can be negligible, and the signal processing circuit for edge detection is not in operation since V_{TRNS} is connected to V_{DD}.

To confirm the edge detection capability of the proposed edge detection circuit according to the state of the electronic switches, a one-dimensional array of 1 × 128 pixels was simulated. The background current level was assumed to be 1 pA. Both V_{TRNS} and V_{GATE} were connected to the ground and V_{REF} of the current-to-voltage converter was set to 1 V. Simulation results for the input photocurrent of 10 pA, 100 pA, and 1 µA, against the background current level of 1 pA, are shown in Fig. 7.

From the above results, we confirmed that the proposed edge detection circuits are able to extract edges with varying input photocurrent levels effectively. There are only large peaks at the boundary of the dark and bright regions. Otherwise, there is a constant voltage distribution of V_{OUT} when the constant input photocurrent (dark or bright regions) is projected onto the array. We confirm that this is in accordance with the principles of retina edge detection. As shown in Fig. 7, one reason for the time scale of the x-axis is that the output voltage is displayed according to the decoder for output selection.

Figure 8 shows the timing diagram of the decoder for the electronic switch and output selections. While an electronic switch is selected by V_{TRNS} for about 260 µs, the pulse period of the decoder for the output selection is about 2 µs because it is necessary to realize 30 frames per second. An appropriate pulse period is 2 µs per unit pixel.

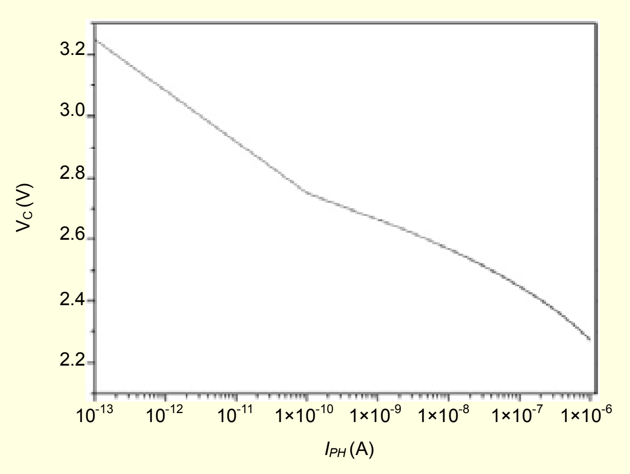

Fig. 5. Transfer characteristics of a logarithmic compression photocircuit.

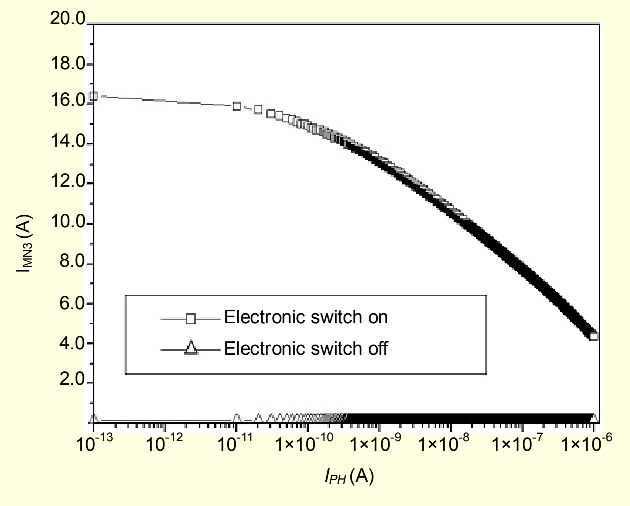

Fig. 6. Transfer characteristics of an electronic switch.

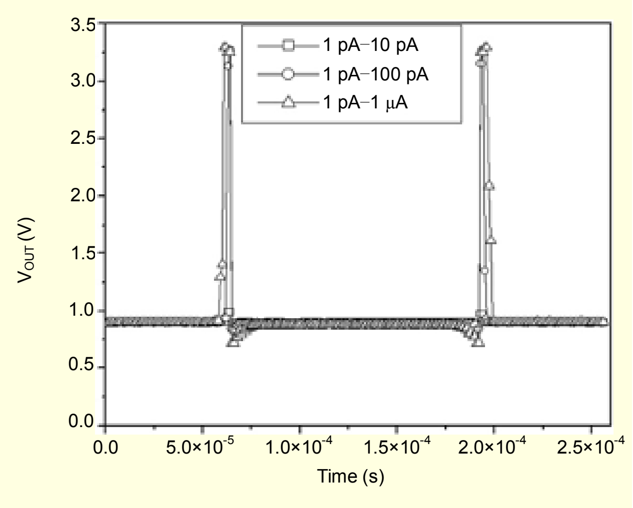

Fig. 7. Simulation results of the one-dimensional array of the edge detection circuit.

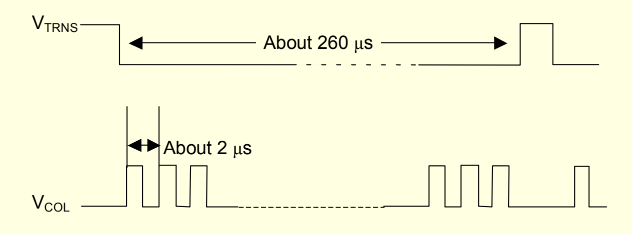

Fig. 8. Timing diagram of a decoder for an electronic switch and output selection.

We also calculated power consumption when V_C is at its highest, which is the worst condition. At that time, I_{VDD}, shown in Fig. 2(c), was about 32 μA. This current always flows through the signal processing circuit for edge detection even if the electronic switch does not exist under even the worst conditions. Figure 9 shows the power consumption estimation of the vision chip with and without an electronic switch. With an electronic switch, which can be reduced to the 1/100 level with increasing pixels, we confirmed that the power consumption is below 20 mW.

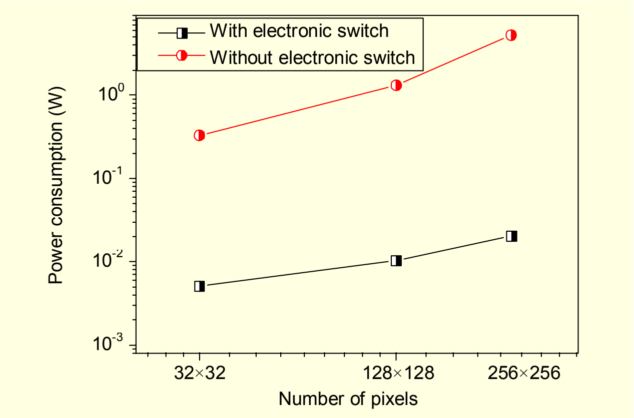

Fig. 9. Estimation of power consumption.

IV. Conclusions

In designing an analog CMOS vision chip for edge detection, power consumption should be considered. To reduce power consumption, an electronic switch was applied to the vision chip. The signal processing circuit for edge detection, with a one-dimensional array of 1 × 128 pixels, was designed and simulated using SPICE to confirm the edge detection capability and power consumption. From the simulated results, we confirmed that our circuit with an electronic switch could effectively detect edges with varying input photocurrent levels. The edge output of the proposed edge detection circuit was confirmed to be in accordance with the principles of edge detection. In addition, its power consumption is below 20 mW and could be reduced significantly compared to circuits without an electronic switch. This vision chip for edge detection with the 128 × 128 pixels was designed using 0.25 μm 1-poly 5-metal standard full custom CMOS process technology. By applying electronic switches to the vision chips, we expect that it is possible to design a vision chip with a higher resolution and lower power consumption. Also, we expect that it is possible to apply the designed vision chip for edge detection to a variety of systems such as target tracking, direction detection, robot vision, and fingerprint recognition [11], [12].

References

[1] C. A. Mead, *Analog VLSI Implementations of Neural Systems*, Kluwer Academic Publishers, Massachusetts 1989.

[2] K. A. Boahen and A. G. Andreou, "A Contrast Sensitive Silicon Retina with Reciprocal Synapses," *Advances in Neural Information Processing Systems*, vol. 4, 1992, pp. 764-772.

[3] E. Funatsu, Y. Nitta, Y. Miyake, T. Toyoda, J. Ohta, and K. Kyuma, "An Artificial Retina Chip with Current-Mode Focal Plane Image Processing Functions," *IEEE Transaction on Electron Devices*, vol. 44, no. 10, 1997, pp. 1777-1782.

[4] C. A. Mead and M. A. Mahowald, "A Silicon Model of Early Visual Processing," *Neural Networks*, vol. 1, 1998, pp. 91-97.

[5] D. S. Park, J. H. Kim, H. S. Kim, J. H. Park, J. K. Shin, and M. H. Lee, "A Foveated-Structure CMOS Retina Chip for Edge Detection with Local Light Adaptation," *Sensors and Actuators*, A108, 2003, pp. 75-80.

[6] S. Kameda and T. Yagi, "An Analog VLSI Chip Emulating Sustained and Transient Response Channels of the Vertebrate Retina," *IEEE Trans. Neural Networks*, vol. 14, no. 5, 2003, pp. 1405-1412.

[7] H. Yamada, T. Miyashita, M. Ohtani, K. Nishio, H. Yonezu, and Y. Furukawa, "Signal Formation of Image-Edge Motion Based on Biological Retina Networks and Implementation into an Analog Metal-Oxide-Silicon Circuit," *Optical Review*, vol. 8, no. 5, 2001, pp. 336-342.

[8] T. Yagi and S. Kameda, "A Parallel Analog Intelligent Vision Sensor with a Variable Receptive Field," *Systems and Computers in Japan*, vol. 30, no. 1, 1999, pp. 60-69.

[9] C. A. Mead, *Analog VLSI and Neural Systems,* Addison-Wesley, Massachusetts 1989.

[10] Alireza Moini, *Vision Chips*, Kluwer Academic Publishers, Massachusetts, 1999.

[11] Kyoung-Ho Choi, Jae-Joon Yoo, Tae-Hyun Hwang, Jong-Hyun Park, and Jong-Hoon Lee, "A Probabilistic Network for Facial Feature Verification," *ETRI J.*, vol. 25, no. 2, Apr. 2003, pp. 140-143.

[12] Sang Kyun Im, Hwan Soo Choi, and Soo-Won Kim, "A Direction-Based Vascular Pattern Extraction Algorithm for Hand Vascular Pattern Verification," *ETRI J.*, vol. 25, no. 2, Apr. 2003, pp. 101-108.

Jung-Hwan Kim received the BE degree in electronic engineering from Kyungil University, Hayang, Korea in 1997 and the ME degree in electronics from Kyungpook National University, Daegu, Korea in 1999. He is now working for the PhD degree at Kyungpook National University. His current fields of interest are in vision chips and intelligent sensors systems.

Jae-Sung Kong received the BE degree in electronic engineering from Kyungpook National University, Daegu, Korea in 2002 and the ME degree in electronics from the same university in 2005. He is now working for the PhD degree at Kyungpook National University. His current fields of interest are in vision chips and neural networks.

Sung-Ho Suh received the BE degree in electronic engineering from Kyungpook National University, Daegu, Korea in 2003 and the ME degree in electronics from the same university in 2005. He is now working in Samsung Electronics Company. His current fields of interest are in CMOS circuit design and memory circuit development.

Minho Lee received the BE degree in electronic engineering from Kyungpook National University, Daegu, Korea in 1988. He received the MS and PhD degrees in electrical engineering from Korea Advanced Institute of Science and Technology(KAIST), Daejon, Korea in 1992 and 1995. He is now an Associate Professor in the School of Electrical Engineering and Computer Science at Kyungpook National University, Daegu, Korea. His current fields of interest are in intelligent information technology and active vision systems.

Jang-Kyoo Shin received the BE degree in electronic engineering from Seoul National University, Seoul, Korea in 1978 and the MS degree in electrical engineering from KAIST, Korea in 1980. He received the PhD degree in electrical engineering from Colorado State University, Fort Collins, USA in 1991. He is now a Professor in the School of Electrical Engineering and Computer Science at Kyungpook National University, Daegu, Korea. His current fields of interest are in semiconductor sensors and intelligent sensor systems.

Hong Bae Park was born in Korea, on March 6, 1951. He received the BE and MS degrees in electronic engineering from Kyungpook National University, Daegu, Korea in 1977 and 1979, and the PhD. degree in electrical and computer engineering from the University of New Mexico, Albuquerque, New Mexico, in 1988. He is currently a Professor in School of Electrical Engineering & computer Science, Kyungpook National University. He received the 'Hae-Dong Paper Award' from IEEK in 1998. His current research interests include robust control, optimal control to industrial applications, guidance control, and mobile systems. He is a member of IEEE, IEEK, ICASE, and ASK.

Chang Auck Choi received the MS and PhD degrees in electronic engineering from Kyungpook National University, Daegu, Korea, in 1988 and 1999, respectively. Since 1980, he is working for ETRI in the area of developing microelectromechanical (MEMS) devices and advanced semiconductor process technology. He is now the Director of the IT-BT Technology Development Department. His current research topics are micro-opto-electromechanical systems (MOEMS), semiconductor sensors, and bio-MEMS.