An Analytical Framework for Imperfect DS-CDMA Closed-Loop Power Control over Flat Fading

Sangho Choe

ABSTRACT—This letter presents an analytical framework for a performance analysis of the imperfect direct-sequence code division multiple access (DS-CDMA) closed-loop power control (CLPC) loop with loop delay, channel estimation error, and power control command bit error as the parameters under a Rayleigh flat fading environment. The proposed model is verified through a comparison between analytical results and simulation ones.

Keywords—Closed loop power control, Rayleigh fading.

I. Introduction

A power control strategy has become more and more important due to the impending arrival of various energy-aware wireless communication systems in the near future, such as multimedia cellular systems, ad-hoc networks, and wireless sensor networks [1]. Thus, a lot of power control issues need to be refined, specified further, or (even) redesigned. Closed-loop power control (CLPC) is a powerful tool to mitigate near-far problems in a direct-sequence code division multiple access (DS-CDMA) system over Rayleigh fading channels. In the literature so far, most of the CLPC related work has relied on Monte-Carlo simulations because the feedback CLPC loop introduces nonlinearity, limiting analytical approaches [2]-[5]. Although Song and others presented some analytical results in [6], they assumed ideal (but impractical) loop conditions, that is, perfect channel estimation, a single loop delay, and a zero power control command bit (PCB) error. In this letter, we extend the statistical linearized method in [6] and present a rigorous analysis including imperfect channel estimation, multiple loop delays[1], and PCB error.

The rest of the letter is organized as follows. In section II, we describe the analytical CLPC model under consideration. In section III, we present the numerical and simulation results, and finally, we conclude in section IV.

II. System Model

We consider a wireless CDMA system where the overall propagation loss is caused by the path loss, large-scale shadowing, and small-scale Rayleigh fading. The path loss and shadowing effects can be compensated by the open loop power control while CLPC is employed for the Rayleigh fading mitigation. In this letter, the Jakes fading model is used for a small-scale Rayleigh flat fading channel [2].

Figure 1 illustrates a typical reverse link CLPC block diagram under non-ideal conditions [3]. Besides the basic delay of one power control group (PCG), the unit of power control

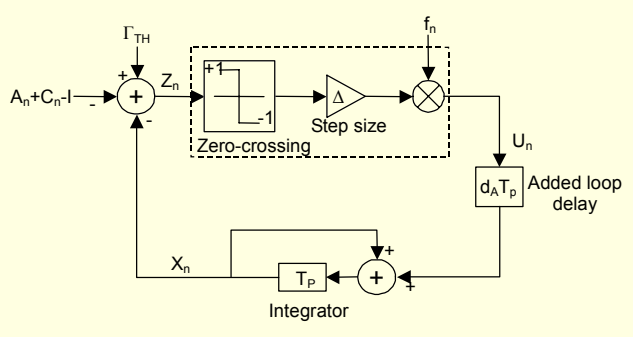

Fig. 1. A block diagram of the closed-loop power control loop for a CDMA system.

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1) The power control loop delay d is typically greater than 2 to 3 power control group (PCG) units due to the processing delay, the round-trip delay, and the frame delay [7].

cycle, for every power control update, in the CLPC loop the additional delay of $d_A(\geq 1)$ PCG intervals is included to represent the overall processing delay and round-trip delay. Thus, the total power control loop delay would be $d \times T_p = (d_A+1) \times T_p$, where T_p is the PCG interval with the sampling rate $f_p = 1/T_p$. To represent the PCB transmission error, the PCB is multiplied by a $f_n = \{\pm 1\}$ binary random variable with a specified error rate. The $f_n = -1$ indicates the error in the PCB transmission. The channel estimation error C_n (unit dB) is also included in Fig. 1 to consider the imperfect channel estimation. The additive white Gaussian noise (AWGN) plus (intracell and intercell) interference power is denoted as I, which is assumed to be a stationary process (constant)[2].

The additional notations are listed in the following. Here, the capital letters denote the random processes in dB, and the subscript n is the index of the PCG in the CLPC loop.

- X_n: The mobile station transmit power level which is controlled by its base station;
- A_n: The power attenuation due to the fading;
- $Y_n = A_n - I$: The channel power variation in the reverse link;
- Z_n: The CLPC loop error;
- U_n: The ± 1 PCB random process from the base station to mobile station;
- C_n: The channel estimation error;
- Γ_n: The received signal-to-noise plus interference (SINR) power ratio in dB;
- Γ_{TH}: The desired SINR threshold ratio in dB used for the PCB decision;
- Δ: The power control step size in dB.

1. Perfect Channel Estimation

In this section, we assume perfect channel estimation, that is, $C_n = 0$ dB, so drop $C_n = 0$ in Fig. 1. For the n-th PCG, the base station measures the received SINR Γ_n from the mobile station as $\Gamma_n = X_n + Y_n = X_n + A_n - I$. The base station compares Γ_n with Γ_{TH} to generate a single PCB. If $\Gamma_n \geq \Gamma_{TH}$, then the base station transmits a negative PCB for the mobile station to decrease its transmitting power by Δ dB for the next PCG interval; otherwise, the base station transmits a positive PCB for the mobile station to increase its transmitting power by Δ dB. The state equation for the CLPC can be written as in [6] as

$$\begin{aligned} X_n &= X_{n-1} + U_{n-d_A-1} \\ &= X_{n-1} + \Delta\Psi(\Gamma_{TH} - X_{n-d_A-1} - Y_{n-d_A-1}) f_{n-d_A-1} \\ &= X_{n-1} + \Delta\Psi(\Gamma_{TH} - \Gamma_{n-d_A-1}) f_{n-d_A-1}, \end{aligned} \tag{1}$$

where the nonlinear function Ψ is the signum function given as

$$\Psi(x) = \begin{cases} 1 & \text{if } x \geq 0, \\ -1 & \text{otherwise.} \end{cases}$$

The nonlinear part in the CLPC is illustrated by dashed lines in Fig. 1 [6]. Using the statistical linearization as in [6], the received PCB signal $U_n = \Delta\Psi(Z_n) f_n$ at the mobile station is approximated as $\hat{U}_n = gZ_n + W_n$, where g is a positive relative coefficient. The Z_n and W_n are assumed to be independent Gaussian random variables with mean zero and variances σ_Z^2 and σ_W^2, respectively. Hereafter, we drop the subscript n of all random variables for the sake of notational convenience. Then, the mean square error (MSE) $= E\{(U - gZ)^2\} = \Delta^2 + g^2\sigma_Z^2 - 2gE\{UZ\}$, where $E\{UZ\} = \Delta E\{\Psi(Z)\}E\{f\}$. The optimum g^*, which minimizes the MSE, is found as

$$g^* = \frac{\sqrt{2/\pi}\,\Delta}{\sigma_Z}(1-2p), \tag{2}$$

assuming that the PCB error probability is defined as $P(f=-1) = p$. The variance of W is then given by

$$\sigma_W^2 = E\{U^2\} - (g^*)^2 E\{Z^2\} = \Delta^2 \left\{ 1 - \frac{2}{\pi}(1-2p)^2 \right\}. \tag{3}$$

The input to the CLPC in Fig. 1 is redefined as $Y' = \Gamma_{TH} - Y$ for analytical convenience. The frequency transfer functions from the input Y' to Z can be written as

$$H_{Y',Z}(e^{-j\omega}) = \frac{1 - e^{-j\omega}}{1 - e^{-j\omega} + g^* e^{-j\omega d}}, \tag{4}$$

where the loop delay $d = d_A + 1$. Also, the frequency transfer function from the input W to Z can be written as

$$H_{W,Z}(e^{-j\omega}) = \frac{-e^{-j\omega d}}{1 - e^{-j\omega} + g^* e^{-j\omega d}}. \tag{5}$$

Let $S_{Y'}(e^{-j\omega})$ represent the power spectral density of input Y' which depends on the fading channel power attenuation factor A. Then, the variance of power control loop error Z is

$$\begin{aligned} \sigma_Z^2 &= E\{Z^2\} \\ &= \frac{1}{2\pi}\left\{ \int_{-\pi}^{\pi} |H_{Y',Z}(e^{-j\omega})|^2 \, S_{Y'}(e^{-j\omega}) d\omega \right. \\ &\qquad \left. + \sigma_W^2 \int_{-\pi}^{\pi} |H_{W,Z}(e^{-j\omega})|^2 \, d\omega \right\}. \end{aligned} \tag{6}$$

2) By considering many users in cellular networks, the interference can be approximated as a Gaussian (stationary) random variable with a constant variance by the central-limit theorem [6].

2. Imperfect Channel Estimation

In this section, we assume imperfect channel estimation, where the channel estimation error C is modeled as a white Gaussian random process with unit dB and a variance of σ_C^2, and is statistically independent of Y' [8]. Defining the ratio, $\alpha = \sigma_C^2 / \sigma_Z^2$, the variance of power control error Z can be written as

$$\sigma_Z^2 = \frac{\frac{1}{2\pi}\left\{\int_{-\pi}^{\pi}\left|H_{Y',Z}(e^{-j\omega})\right|^2 S_{Y'}(e^{-j\omega})\right\}d\omega + \sigma_W^2\int_{-\pi}^{\pi}\left|H_{W,Z}(e^{-j\omega})\right|^2 d\omega}{1-\frac{\alpha}{2\pi}\int_{-\pi}^{\pi}\left|H_{C,Z}(e^{-j\omega})\right|^2 d\omega,} \tag{7}$$

where $H_{C,Z}(e^{-j\omega})$ has the same form as $H_{Y',Z}(e^{-j\omega})$. The power control error variance σ_Z^2 in (6) and (7) can be solved easily by numerical approach once the channel variation input spectrum $S_{Y'}(e^{-j\omega})$ is known [6].

III. Numerical Results

We consider a wireless system with a 2 GHz carrier frequency, 10 Kbps data rate, and 2 KHz PCG rate. We adopt the Jakes flat fading model with the normalized maximum Doppler frequencies $f_D T_b$ = 0.0037 and 0.0185, which correspond to mobile station speeds of 20 km/h and 100 km/h, respectively. And to evaluate the input channel power spectral density $S_{Y'}(e^{-j\omega})$ in (6) and (7) we employ a quasi-analytic approach, which is based on a set of simulated fading samples [6]. Assume that a single bit is used to represent the transmitted PCB and that the power control step size Δ is set to 1 dB.

Figure 2 illustrates the standard deviation of the power control loop error σ_Z (dB) for the case of perfect channel estimation, that is, $\alpha = 0\%$. Both the analytical and simulation results are given for various loop delays d = 1, 2, and 3 and PCB error = 0 and 10%. We observe that the simulation and analytical results provide a good match lying within 0.2 to 0.3 dB of each other. It should be further noted that the analytical curves are somehow pessimistic in comparison to simulations. This is due to the linearlization of the signum function in the CLPC loop. Figure 2 demonstrates that a loop delay increment of one unit increases the PC loop error by 0.6 to 0.7 dB; Corazza and others [9] presented that a 1 dB PC loop error corresponds to a capacity loss of about 20 users per cell. Furthermore, it is observed that the slope of the standard deviation of the PC loop error is larger at a low speed (for example, 20 to 40 km/h) than that at a high speed. Finally, it is interesting to note that the increment of the PCB error rate from 0 to 10%

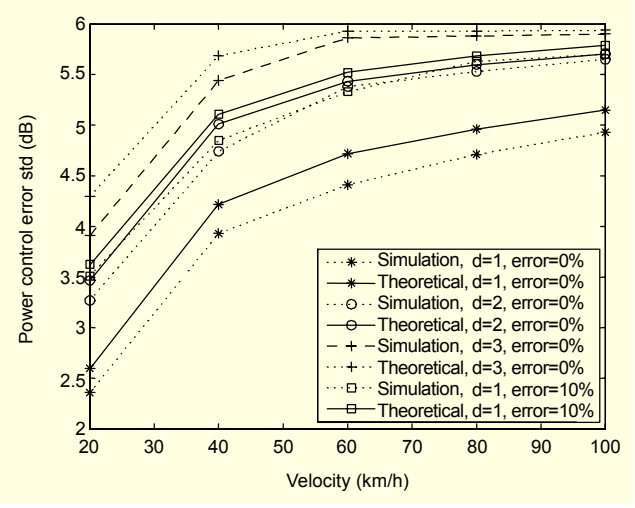

Fig. 2. Comparison between the analytical and simulation results of the power control error standard deviation (dB) with the loop delay d and the PCB error rate as the parameters in the flat fading channels.

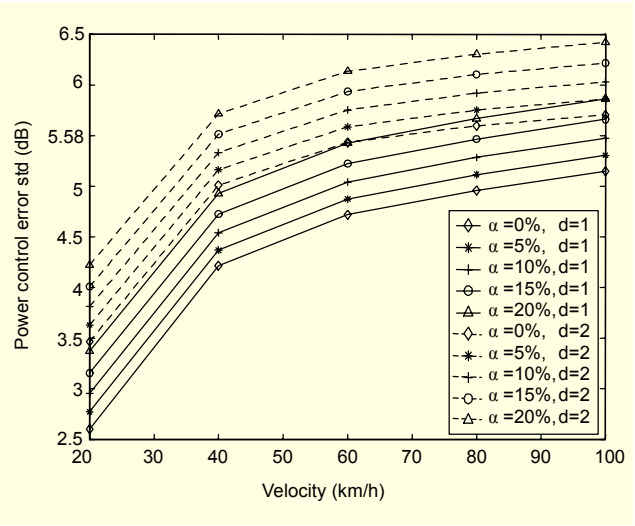

Fig. 3. The power control loop error standard deviation (dB) with the loop delay d and the channel estimation error rate α as the parameters in the flat fading channels.

does not change the PC loop error standard deviation significantly. This verifies that the PC loop is robust to the feedback channel error [3].

Figure 3 shows the analytical results of the power control error standard deviation σ_Z (dB) for the case of imperfect channel estimation, that is, $\alpha \neq 0$. The PCB error rate is assumed to be 0%, and the loop delay d varies from 1 to 2. Observe from Fig. 3 that the channel estimation error degrades the PC loop performance. For example, when the channel estimation error rate α changes from 0 to 10%, it increases the standard deviation of the PC loop error by 0.4 dB.

IV. Conclusion

This letter presented an analysis tool for the imperfect DS-CDMA CLPC over flat fading, considering channel estimation error, PCB error, and multiple loop delays. The simulation results verified that the proposed analysis method works well, and the proposed analysis can be employed for simulation, which typically requires heavy computation. It was observed that a loop delay increment by one PCG unit causes 0.6 to 0.7 dB degradation on the PC loop error σ_Z, which corresponds to a capacity loss of about 15 users per cell. In addition, for every 10% increase of the channel estimation error, the standard deviation σ_Z of the PC loop error increases 0.4 dB.

References

[1] A. J. Goldsmith and S. B. Wicker, "Design Challenges for Energy-Constrained Ad Hoc Wireless Networks," *IEEE Wireless Communications*, vol. 9, no. 4, Aug. 2002, pp. 8-27.

[2] A. Chockalingam, P. Dietrich, L. B. Milstein, and R. R. Rao, "Performance of Closed-Loop Power Control in DS-CDMA Systems," *IEEE Trans. on Vehicular Technology*, vol. 47, no. 3, Aug. 1998, pp. 774-789.

[3] S. Ariyavisitakul and L. F. Chang, "Signal and Interference Statistics of a CDMA System with Feedback Power Control," *IEEE Trans. on Commun.*, vol. 41, no. 11, Feb. 2001, pp. 1626-1634.

[4] K. Shoarinejad, J. L. Speyer, and G. J. Pottie, "Integrated Predictive Power Control and Dynamic Channel Assignment in Mobile Radio Systems," *IEEE Trans. on Wireless Commun.*, vol. 2, no. 5, Sept. 2003, pp. 976-988.

[5] C. C. Lee and R. Steele, "Closed Loop Power Control in CDMA Systems," *IEE Proc.-Commun.*, vol. 143, no. 4, Aug. 1996, pp. 231-239.

[6] L. Song, N. B. Mandayam, and Z. Gajic, "Analysis of an Up/DownPower Control Algorithm for the CDMA Reverse Link under Fading," *IEEE J. on Select. Areas in Commun.*, vol. 19, no. 2, Feb. 2001, pp. 227-286.

[7] K. Leibnitz, P. Tran-Gia, and J. E. Miller, "Analysis of the Dynamics of CDMA Reverse Link Power Control," *Proc. IEEE Globecom*, Sydney, Australia, Nov. 1998, pp. 2109-2114.

[8] J. R. Gallego, A. Valdovinos, M. Canales, and J. Mingo, "Analysis of Closed Loop Power Control Modes in UTRA-FDD under Time-Varying Multipath Channels," *Proc. IEEE PIMRC*, Sept. 2002, pp. 1616-1620.

[9] C. E. Corazza, G. D. Maio, and F. Vatalaro, "CDMA Celluar Systems Performance with Fading, Shadowing, and Imperfect Power Control," *IEEE Trans. on Vehicular Technology*, vol. 47, no. 2, May 1998, pp. 450-459.