Analysis of the Influence of the Address Electrode Width on High-speed Addressing Using the Vt Close Curve and Dynamic Vdata Margin

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Abstract - In order to drive the high-density plasma displays, a high-speed driving technology must be researched. In this experiment, the relationship between the width of the address electrode and high-speed driving is analyzed using the Vt close curve and the panel structure for high-speed driving is proposed. In addition we show that the wider the width of the address electrode is, the narrower the width of the scan pulse becomes. Therefore, we could achieve the minimum data voltage of 50.1V at a scan pulse width of 1.0μs and a ramp voltage of 210V at an address electrode width of 180μm for the high-speed driving 4-inch test PDP.

Keywords: address discharge characteristics, address electrode width, Vt close curve, plasma display panel

1. Introduction

A Plasma Display Panel is a self-emitting display device that gives light by discharge. Recently, the development of fabrication and driving technology have allowed for the production of high-density PDPs. Currently, the main topics of PDP research are high quality image, low power consumption, environmentally friendly materials, high luminance efficiency, and low cost.

The principle of PDP lamination is the discharge in the narrow vacuum space. The driving technique is a time-separate method. In these results, dynamic false contours occur in the case of a moving image and we must reduce the scan pulse width in order to drive the high-density PDPs. So, in order to drive the PDP by high-speed address, the scan pulse width must be reduced[1-4]. In terms of the image information processing of 10 bits and the improvement of dynamic false contours, we must increase the number of sub-fields per TV-frame. For the increase of the number of sub-fields and the driving of high-density PDPs, a high speed addressing technique, which reduces the scan pulse width, is demanded.

We can study the high-speed driving technique by two methods. One is a driving waveform that can reduce the discharge delay time at the scan/address period[3-5]. The other is an optimization of the PDP-cell structure for reducing this delay time[2-3], [6]. In the former procedure, we can reduce discharge delay time by studying driving methods that provide a strong reset discharge at reset periods in each sub-field and use the priming particles or selective erase-type addressing technology. In the latter, we are able to optimize the specification of cell structures that influences the threshold voltage.

In general, among the PDP-cell structures, the thickness of the front dielectric layer, the width of the sustain electrodes, the gap between the electrodes, the height of the barrier rib for the discharge space[6], the width of the address electrode for the scan and address discharge, the materials of the MgO protecting layer in order to protect the dielectric layer from scattering at a plasma discharge, and gas compositions influence the characteristics of a discharge[2-3].

In order to drive the high-speed addressing, we have to reduce the discharge delay time. The lower the data voltage is, the faster the address discharge becomes. In this research, when the width of the address electrode varied from 60 to 180μm, we analyzed that these had an influence on high-speed addressing in the AC-PDP panels, which were 4-inch stripe type. At that time, the basic ramp-reset driving waveform was applied and we measured the dynamic margin between the ramp-reset voltage and the data voltage as the width of scan pulse is varied. We analyzed the influence of the address electrode width on the address discharge characteristics using the Vt close curve. The Vt close curve is the close curve that links each threshold voltage of the three-electrode structure. We developed the wall voltage measuring system and measured the 6 threshold voltages to graph the Vt close curve.

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Received 10 May, 2005 ; Accepted 23 July, 2005

2. Experiments

2.1 The Fabricated Test Panels

In order that we might analyze the relationship between the address electrode width and characteristics of the address discharge, 4″ test panels of a stripe-type were used, as presented in Fig. 1.

Fig. 1 shows the fabricated PDP panel structure. The front glass composes the scan and sustain electrodes by the ITO, dielectric layer, and MgO as a protected layer. The address electrode is laid on the rear glass, the rear dielectric layer is deposited on the address electrode, and the barrier rib is printed onto the rear dielectric layer. The last step is the bonding of the two glasses after degassing and injecting the composed discharge gas. We used the fabricated panels with a dielectric layer thickness of 30μm, barrier-rib height of 140μm, and width and gap of sustain electrodes of 320 and 90μm, respectively, within the He-Ne-Xe gas mixture. Data voltages that are supplied to the address electrode decide between the ON-cell and OFF-cell.

In this experiment, the used panels had varied widths of the address electrode at 60, 100, 140, and 180μm. In order to allow for the panel variation, we fabricated 3-5 test panels per type.

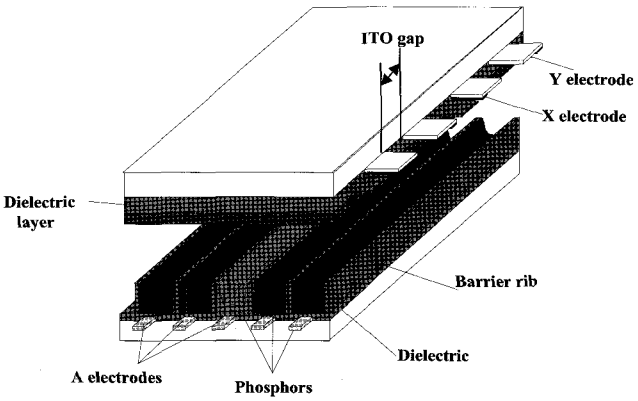


Fig. 1 Fabricated panel structure

2.2 Driving Waveform for Experiments

In order to analyze the relationships between the address electrode width as the panel structure and the high-speed scan/address discharge characteristics, a basic ramp reset driving waveform was applied to the test panels, as illustrated in Fig. 2, and the dynamic margins of the data voltage were measured as the voltage was applied to the address electrodes. The driving waveforms Y, X and A were supplied to the scan, sustain, and data (address) electrodes, respectively.

In order to compare the electrical address discharge characteristics of high-speed addressing, when the total scan/address period was maintained and the scan pulse width varied between 0.8μs and 2.0μs, the dynamic data voltage margins were measured. Before measuring the margin, all voltages of the driving waveform were optimally selected for all panels. For these experiments, the measured voltages were the dynamic margin between the ramp top voltage (Vramp) and data voltage (Vdata), because these were conducive for the discharge characteristics in the address period.

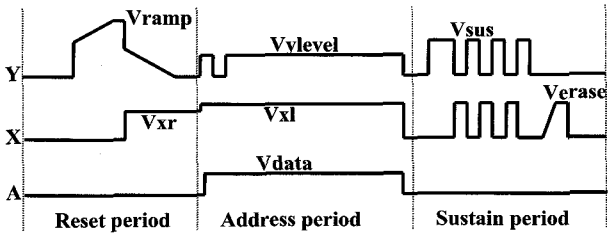


Fig. 2 Driving waveform for experiments.

2.3 The Measurement of the Wall Voltage Using the Vt Close Curve

When we want to determine the changed quantity of the wall voltage from a discharge, the wall voltage transfer curve between the two discharge electrodes can be used. This shows the changed quantity of the wall voltage according to the applied voltage. This, however, is insufficient when showing the firing voltage of the PDP discharge cell in a 3-electrode structure.

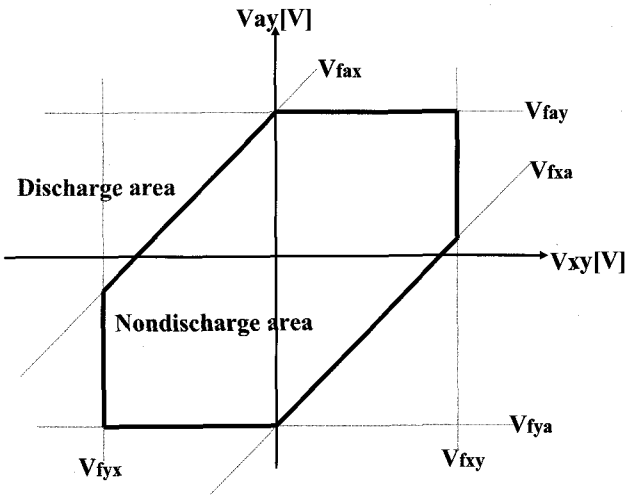


Fig. 3 Vt closed curve

The Vt close curve is presented to complement this fault and to analyze the firing voltage and discharge characteristics of the 3-electrode structure. This curve sets one (Y) of the three electrodes as the base electrode and can be expressed on a plane, as shown in Fig. 3. The x-

axis is the electric potential between the X and Y electrodes and the y-axis is the electric potential between the A and Y electrodes in this plane. A total of 6 firing voltages exist in the 3-electrode structure and these firing voltages occur between the X-Y, A-Y, and A-X electrodes and are expressed as Vfxy, Vfyx, Vfay, Vfya, Vfax, and Vfxa as the non-inverse or inverse voltage is applied. If these 6 types of firing voltages are indicated on this plane, they form a hexagon-shaped close curve. If an applied voltage corresponding to the inner close curve is applied to each of the three electrodes, the cell doesn't discharge. However, if an applied voltage, corresponding to the outer close curve, is applied to each of the three electrodes, the cell is discharged.

In the case of the PDP cell, control of the wall charge is significant. If the wall voltage can be controlled or measured easily, the discharge can be effortlessly controlled and analyzed. Measuring the wall voltage is impossible because the wall voltage can't be measured by using the external probe. Even if it can be used, the wall voltage cannot be measured because the wall charge disappears as soon as the probe interacts with the charge on the inner electrode.

An indirect method of measuring the wall voltage can be achieved by using the Vt close curve. If a cell does not have any wall charge, the cell will discharge when the applied voltage reaches the firing voltage. At that time, the applied voltage is the demarcation of the Vt curve, because the wall voltage is 0V. Assume that only the x-electrode of the inner cell has a wall charge and therefore has a wall voltage (Vwx). In this case, the least applied voltage (Vaax) needed to generate a discharge between the X and Y electrodes is expressed by Vfxy-Vwxy. Also, the wall voltage of the X electrode (Vwx) affects the cell voltage between the A and X electrode and the least applied voltage (Vaax), for the discharge between the A and X electrodes is expressed by Vfax-Vwax. On the other hand, this wall voltage doesn't affect the discharge between the A-Y electrodes. Therefore, the Vt curve is measured as a shifted Vt curve, as indicated in Fig. 3 since it displays the applied voltage when the discharge occurs.

When viewed from a different point of view, the existence of a wall voltage due to the wall charge is known if the shifted Vt curve is measured. Expressing the wall voltage on each electrode as an absolute value is impossible, and only the difference of the wall voltage between the electrodes can be determined, because discharge occurs due to the difference of the applied voltages on each electrode. We can satisfy the measurement of the difference of the wall voltage only. In order to measure the wall voltage, the wall voltage measurement system was made. It is used to measure the value and change of the Vt close curve and wall voltage.

3. Results and discussions

3.1 Measured Vt Close Curves without Wall Charges

The firing voltages between the electrodes on the 4-type panels with address electrode widths of 60, 100, 140, and 180μm were measured using the wall voltage measuring system, as indicated in Fig. 4.

The experiment considered the effects of the wall charge and gathered the measurements after self-erasing with a strong discharge. The experiment results showed that the surface firing voltage was constant and was not affected by the address electrode width, and the opposing firing voltage decreased as the address electrode width increased. Since the address electrode width is of no consequence to the surface discharge that occurs between the X and Y electrodes, the firing voltage was constant. For the opposing charge, it was found that the discharge could occur more readily as the address electrode width and the electrode surface area that had an effect on the discharge increased. From these results, we can expect that the minimum Vdata voltage of the address electrode width of 180μm is the lowest.

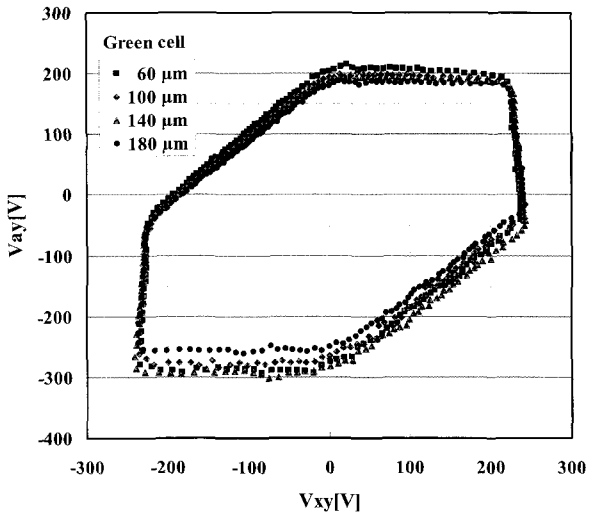


Fig. 4 The measured Vt close curves of the test panels

3.2 Selecting the Test Point (Ts) to Analyze the Address Discharge Characteristics

The number of the scan lines is limited by 40, in case of the 4-inch test panel. In order to analyze the address discharge characteristics using a small test panel, the starting point of the first scan pulse must become cleared. Analysis of the relationship between the barrier rib height of the PDP cell's structure and Vdata voltage margin was difficult, because if the Ts was short, then the address discharge was influenced by the priming particles. The Ts

was defined as the starting point of the first scan pulse after the ramp-reset period of the basic driving waveform, as displayed in Fig. 5.

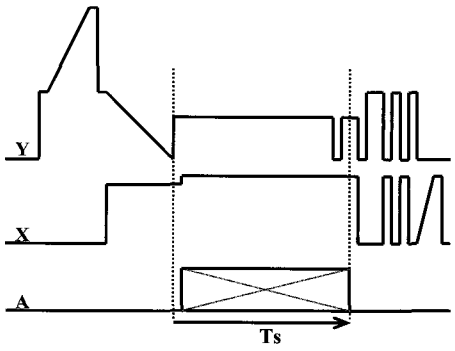


Fig. 5 Definition of the Ts

The Vdata voltage margins were measured as a function of the Ts, as shown in Fig. 6. The measured time ranged from 10μs to 840μs. In this experiment, the scan pulse width was 2.0μs and the Vramp voltage ranged from 130V to 240V. The minimum Vdata voltage increased rapidly before the Ts of 110μs, because the charged particles, which were generated by the reset discharges, were distributed in the vacuum space and decreased the firing voltages. After the Ts of 110μs, when the charged particles moved to each electrode by the electric fields, the priming effects disappeared. And therefore, the wall charges only affected the firing voltage. The charged particles in the vacuum space, as the PDP cells, decreased the vacuum resistor and the firing voltages between the electrodes. The minimum data voltage at the Ts of 10μs was 26.8V and the saturated minimum data voltage was about 40.0V at the Ts of 110μs. However, the maximum data voltage had constant value in spite of the increase of the Ts.

This experimental result means that the priming particles, which are generated by the weak reset discharges, almost completely disappear after 110μs, the minimum Vdata voltage can be decreased using the priming particles, and the high-speed addressing technique can be realized.

Fig. 7 indicates the measured dynamic Vdata voltage margin. The dynamic voltage margin decreased as the Ts. Especially, it rapidly decreased before the Ts of 110μs. And the Vdata margin increased as the Vramp voltage. The minimum Vdata voltages were about 47.4V at the Vramp of 210V and about 49.2V at the Vramp of 240V, after the saturation.

From these experimental results, we gather the fact that it was very important for the Ts to have been fixed, in order to analyze the address discharge characteristics using a 4-inch test panel. If the Ts was decided by the ending point of the reset period, the analysis of the address discharge characteristics could become difficult because of the priming effect of the charged particles. In this study, the Ts was decided on the 400μs.

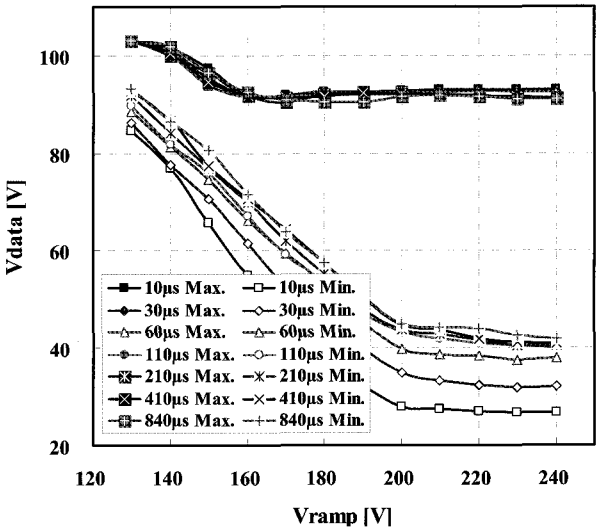


Fig. 6 The maximum and minimum data voltages according to the time after the ramp-reset period, when the address electrode width was 100μm

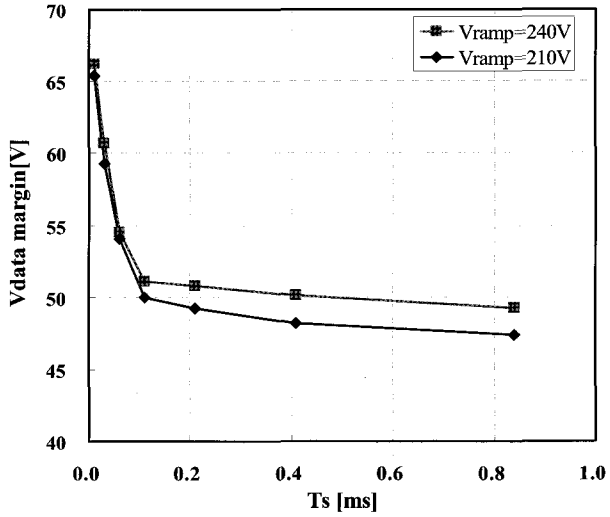


Fig. 7 The Vdata voltage margin according to the Ts

3.3 Dynamic Voltage Margins

Fig. 8 shows the measured results of the data voltage margin as the Vramp changed for the full-white, red, green and blue patterns when the address electrode width was 180μm and the scan pulse width was 2.0μs. In these experiments, the driving waveform was applied to a 4-inch test panel. The results indicated that the minimum and maximum data voltages decreased as the Vramp increased and these voltages were saturated when the Vramp voltage was over 180V. At the Vramp of 220V, the minimum and maximum Vdata voltages were 30.5V and 90.8V, respectively.

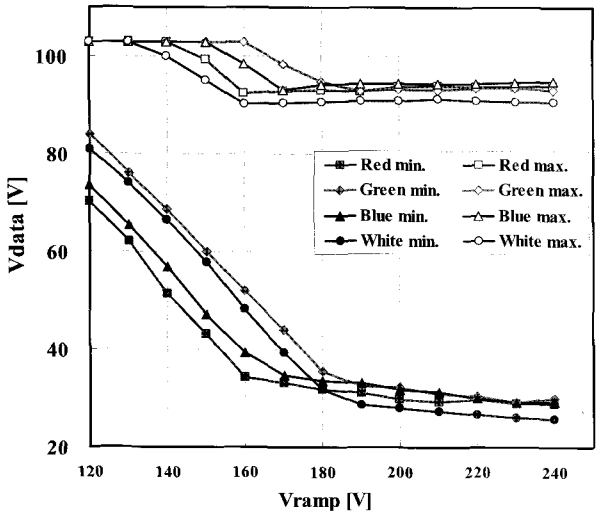
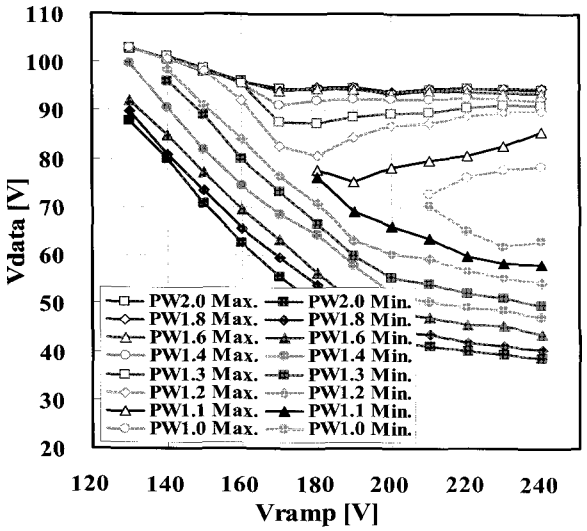
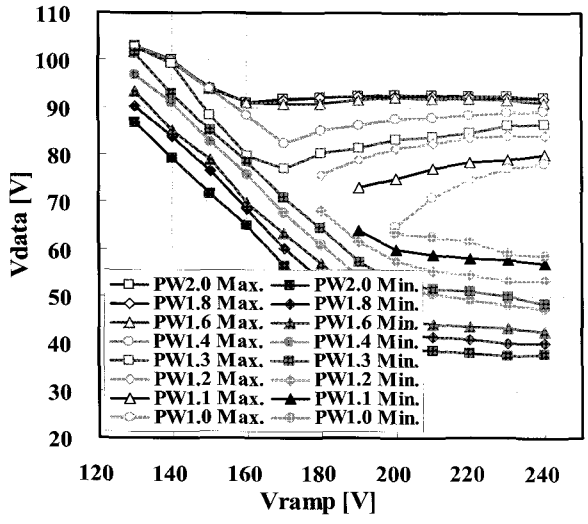


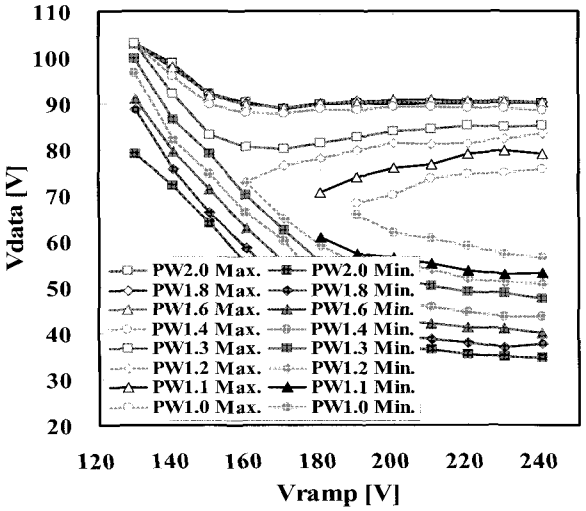
Fig. 8 The data voltage margins at a scan pulse width of 2.0μs when the address electrode width was 180μm



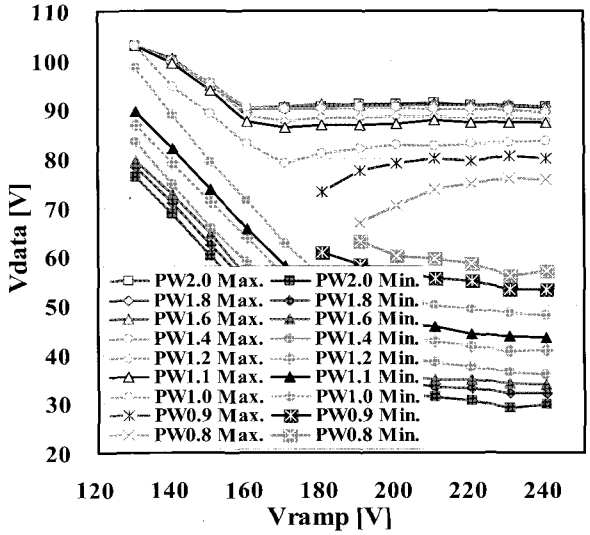
(a) With an address electrode width of 60μm



(b) With an address electrode width of 100μm



(c) With an address electrode width of 140μm



(d) With an address electrode width of 180μm

Fig. 9 The maximum and minimum Vdata voltages according to the scan pulse width.

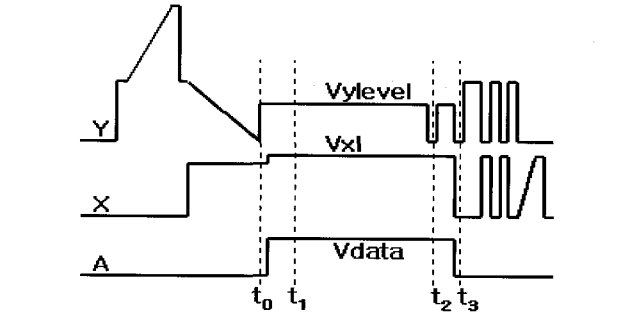
Fig. 9 presents the measurement results of the maximum and minimum Vdata voltages and dynamic Vdata voltage margins according to the scan pulse width when the address electrode widths were 60, 100, 140 and 180μm. In all cases, the maximum Vdata voltages decreased and the minimum Vdata voltages increased as the scan pulse width decreased. The maximum Vdata voltage decreased. The cell voltage is located at position B in Fig. 10(b), when the time is t_0. It is located at position A at time t_1.

If the Vdata voltage is high, a cell voltage that exceeds the firing voltage (Vfay at position A), which is the boundary of the Vt curve, is applied at time t_1, and then, a weak discharge may occur, as seen in Fig. 10(b). This is the discharge where the A-electrode is the anode and the Y-electrode is the cathode, and the negative and positive

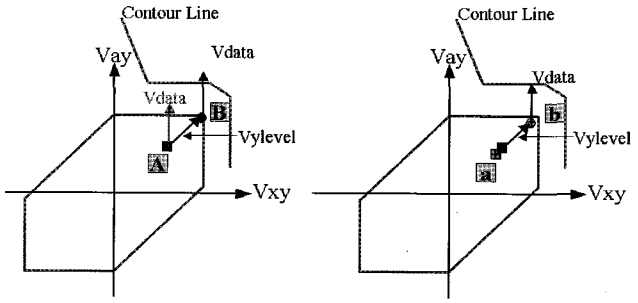
charged particles are accumulated on the A-electrode and Y-electrode, respectively, as the wall charges. Due to this discharge, it is brought to the change of the wall charge, which shifts the cell voltage from position A to a.

In this case, a continuous sustain discharge is not easily maintained in spite of the address discharge at time t_2, because the discharge delay time lags. Accordingly, if the scan pulse width is wide, this time delay does not affect the address discharge. However, the minimum Vdata voltage is a necessary higher voltage as the scan pulse width narrows.

When the Vramp voltage was 220V and the scan pulse width was 0.8μs, the panels, which had an address electrode width of 60μm, 100μm, or 140μm, did not have a margin. However, the minimum and maximum Vdata voltages of the panel, which had an electrode width of 180μm, were 59.5V and 74.9V, respectively and the dynamic voltage margin was 16.4V. This shows that a stable sustain discharge can be generated when the Vdata voltage is set at 70V. Therefore, it is confirmed that the address electrode width must be increased for high-speed addressing.



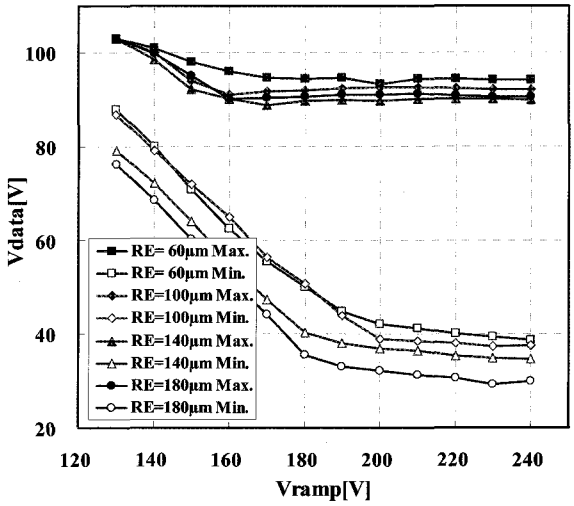
(a) Driving waveforms



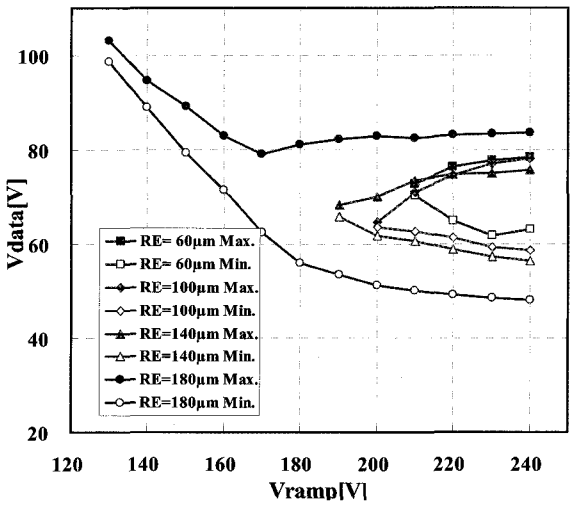
(b) The cell and wall voltages

Fig. 10 Analysis of the trends of the maximum Vdata margin according to the scan pulse width using Vt close curves.

Fig. 11 presents the dynamic margins of the Vdata voltage according to the address electrode width when the scan pulse widths were 2.0μs and 1.0μs. The results indicate that the minimum data voltage decreases and the range of the Vramp voltage widens according to the address electrode width. At the Vramp voltage of 220V, the scan pulse width of 2.0μs and the address electrode width of 60μm, the minimum data voltage was 40.1V. And at the address electrode width of 180μm, that voltage was 30.5V.



(a) At a scan pulse width of 2.0μs



(b) At a scan pulse width of 1.0μs

Fig. 11 The dynamic margins of the Vdata voltage according to the address electrode width

In particular, at the scan pulse width of 1.0μs and the address electrode width of 60μm, the minimum data voltage was 64.9V. And at the address electrode width of 180μm, that voltage was 49.2V, which shows a difference of 15.7V. These address discharge characteristics demonstrate that sustain discharges occur more readily, when the minimum data voltage is lower. The reason for this is that a stronger discharge can be generated if the applied voltage is high. If the same data voltage of 70V is applied, the panel with an electrode width of 180μm can generate a stronger discharge than the panel with an electrode width of 60μm.

Fig. 12 shows the measured results of the minimum Vdata voltage at the Vramp voltage of 210V. These experimental results indicate that the minimum Vdata voltages increase according to the increase of the address electrode width. The minimum Vdata voltage decreased according to the scan pulse width in case of all the test panel types. The minimum data voltages were 50.1V, 60.6V, 62.6V, and 72.6V in the case of the address electrode widths of 60μm, 100μm, 140μm, and 180μm, respectively, at the scan pulse width of 1.0μs. The minimum Vdata voltage of the test panel with the address electrode width of 180μm was 59.5V at the scan pulse width of 0.8μs. However, the minimum Vdata voltage could not be obtained in the case of the others, because the dynamic voltage margin could not be had.

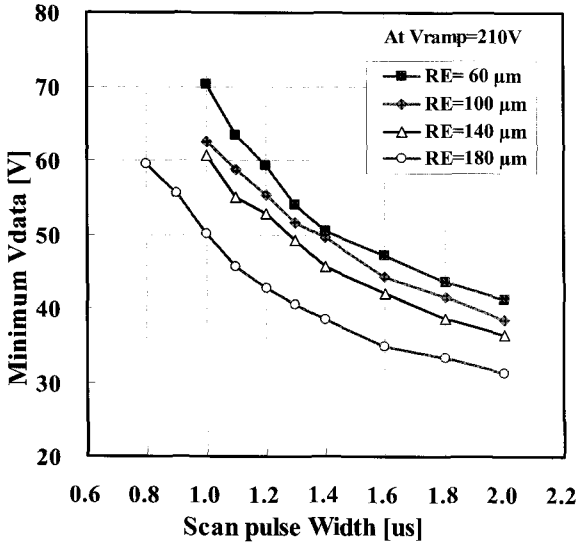


Fig. 12 The minimum Vdata voltage according to the width of the address electrode

These results can be explained from the experimental results of the Vt curve of Fig. 4. There was no significant difference in the surface firing voltage when the address electrode width increased, but the opposed firing voltage decreased greatly when the address electrode width was 180μm. Stable driving is possible even if the Vramp is low in the case of a panel with a wide address electrode width. This implies that a sufficiently stable wall charge can be generated although the Vramp voltage is low. It also means that if a higher Vramp voltage is applied, an even greater wall charge can be generated, and then a stronger discharge can occur because the discharge delay can be reduced.

Therefore, if a panel has a wide address electrode width, the scan pulse width can be reduced under conditions with the same applied voltage, and thus high-speed addressing is possible.

4. Conclusions

The address electrode width of the PDP structure has influence on the address discharge characteristics for the driving PDP. The 4-inch test panels, which had the different address electrode widths, were made in order to analyze the effects of the address electrode width to the address discharge characteristics, in particular, the high-speed addressing tendency. The Vt close curve was used and the Vdata voltage margin was measured to analyze the high-speed addressing tendency and address discharge characteristics according to the scan pulse width. A driving PDP was possible at a scan pulse width of 1.0μs at all of the address electrode widths within test panels. However, the driving Vdata margin of the panel, of which the address electrode width was 180μm, was the smallest having 50.1V at the Vramp voltage of 210V.

The results showed that the address discharge characteristics were better as the address electrode width increased and this panel's factor had to increase for the high-speed addressing.

Acknowledgements

This work was supported by the Engineering Research Center (ERC) and the Korea Science and Engineering Foundation (KOSEF). This work was also supported by project no. 10016632(2004) of MOCIE.

References

[1] A. Seguin, L. Tessier, H. Doyeux and S. Salavin, "Measurement of Addressing Speed in Plasma Display Devices," Proc. IDW99, Sendai, Japan, pp. 699-702, December 1999.

[2] Jae Sung Kim, Jin Ho Yang, Tae Jun Kim and Ki Woong Whang, "Comparison of Electric Field and Priming Particle Effects on Address Discharge Time Lag and Addressing Characteristics of High-Xe Content AC PDP," IEEE Trans. Plasma Science, vol. 31, no. 5, pp. 1083-1090, Oct. 2003.

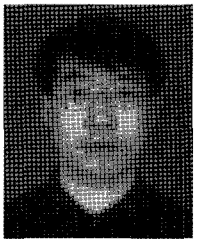
[3] Jae Sung Kim, Jin Ho Yang, and Ki Woong Whang, "A Driving Method for High-Speed Addressing in an AC PDP Using Priming Effect," IEEE Trans. Electron Devices, vol. 51, no. 4, pp. 548-553, Apr. 2004.

[4] K. Sakita, K. Takayama, K. Awamoto and Y. Hashimoto, "High-speed Address Driving Waveform Analysis Using Wall Voltage Transfer Function for Three Terminal and Vt Close Curve in Three-

Electrode Surface-Discharge AC-PDP's," SID2001 Tech. Dig., San Jose, USA, pp. 1022-1025, June 2001.

[5] S.K.Lee, W.J.Kim, Y.J.Lee, Y.D.Kim, M.S.Kim, S.J.Moon, Y.H.Kwon, S.J.Yoo and J.D.Kim, "Analysis of Priming Effect Using Vt Close Curve," Proc. IDW02, Hiroshima, Japan, pp.709-712, December, 2002.

[6] Y.D.Kim, W.J.Kim, Y.J.Lee, S.K.Lee, M.S.Kim, S.J.Moon, Y.H.Kwon, S.J.Yoo and J.D.Kim, "The Relation between Opposed Firing and Ramp Reset Voltage in AC-PDP Driving Waveform," Proc. IDW02, Hiroshima, Japan, pp. 717-720, December 2002.



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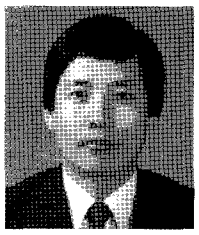

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