A Novel Zero-Voltage-Switching Push-Pull DC-DC Converter for High Input Voltage and High Power Applications

Saijun Mao*, Huizhen Wang* and Yangguang Yan*

Abstract - This paper proposes a novel zero-voltage-switching (ZVS) Push-pull DC-DC Converter for high input voltage and high power applications. This topology utilizes two switches in series to replace one switch in conventional push-pull converter, and two clamping diodes are introduced. The voltage stress of the switches is the input voltage, and the switches can realize ZVS with the use of the leakage inductance of the transformer. Furthermore, secondary full-wave rectifier with a clamping capacitor is used to eliminate the voltage oscillation and spike of the rectifier diodes due to the reverse recovery. Therefore, the electromagnetic interference is reduced effectively. The operation principle of the proposed converter is analyzed theoretically. The output characteristic, ZVS condition and design principle of the clamping capacitor are discussed. Experimental results obtained from a 270V input 2kW prototype with 95.8% high efficiency confirms the design.

Keywords: Converter, push-pull, zero-voltage-switching, clamping capacitor, high input voltage

1. Introduction

In industry applications, conventional push-pull converter is widely used in low input voltage and low power applications due to its simple topology structure [1-7]. However it suffers from the high turn-off voltage spike of the switches due to the transformer leakage inductance. In recent years, push-pull forward converter is attractive in voltage regulator module due to its good performance. The clamping capacitor can restrain the voltage spike of the switches, but the switches still suffer more than two times input voltage stress [8-10]. Two-transistor forward converter and full bridge converter are suitable in high input voltage and high power applications because the voltage stress of the switches is only the input voltage. The two-transistor forward converter is more reliable, however it has the drawback of hard switching and single quadrant operation of the transformer [11, 12]. Phase-shifted full-bridge converters can achieve soft-switching easily; however, this topology suffers from risk of direct shoot-through failures, as the switches are directly connected across the source [13, 14]. In recent years, three-level converter has received a lot of attention due to their suitability for applications with high input voltages. However, it needs two large volume divided capacitors to share the input voltage evenly, and the control strategy of the topology is complex [15, 16].

This paper proposes a novel zero-voltage-switching push-pull DC-DC converter for high input voltage and high power applications, as shown in Fig. 1. This topology utilizes two switches in series to replace one switch in conventional push-pull converter; moreover, two clamping diodes are introduced. The voltage stress of the switches is only the input voltage, and the switches can realize zero-voltage-switching with the use of the leakage inductance of the transformer and the parasitic capacitors of the switches. Furthermore, secondary full-wave rectifier with a clamping capacitor is used to eliminate the voltage oscillation and spike of the rectifier diodes due to the reverse recovery. The converter operates at a fixed duty cycle ratio near unity and all switches run at a duty cycle of around 50%, As a result the load current never has to come solely out of the output filter for any significant fraction of the switching period. The inductor in the customary inductor/capacitor output filter can therefore be removed.

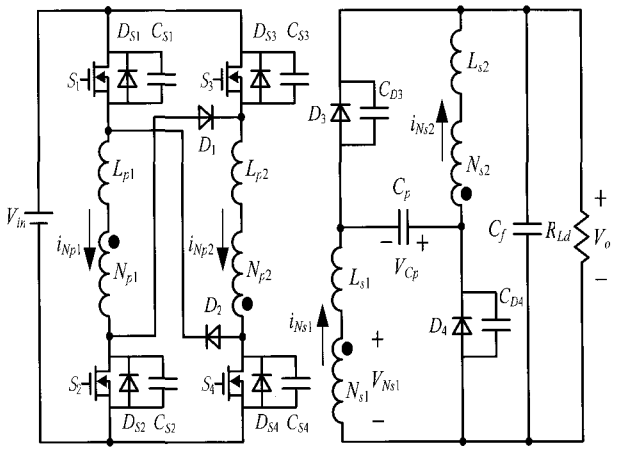

Fig. 1 Proposed Push-pull DC-DC converter

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2. Operation Principle of the Proposed Converter

Key waveforms and equivalent circuits of the switching modes in a half switching cycle are shown in Fig. 2 and Fig. 3, respectively. Half of the switching cycle of the proposed converter can be divided into five modes. The following assumptions are made to simplify the analysis of the proposed converter: 1) the circuit operates in steady-state; 2) MOSFETs are considered as ideal switches with their body diodes and parasitic capacitances. $C_{S1}=C_{S2}=C_{S3}=C_{S4}=C_S$. All diodes are considered as ideal except for the rectifier diode, which is equivalent to an ideal diode and a junction capacitor. $C_{D3}=C_{D4}=C_D$. 3) Turn ratio of the transformer is $n=N_s$: N_p, where $N_p=N_{p1}=N_{p2}$; $N_s=N_{s1}=N_{s2}$. Transformer's two primary windings and two secondary windings have leakage inductance $L_{p1}=L_{p2}=L_p$ and $L_{s1}=L_{s2}=L_s$ respectively. 4) The capacity of the clamping capacitor C_p is sufficiently large so that the voltage of C_p can be considered as a constant voltage source with a value equal to output voltage V_o.

1) Mode 1 [t_0, t_1] [Fig. 3 (a)]: Prior to t_0, S_1, S_2 conduct. Magnetizing current increases in a positive direction and power is transferred from the input source to the load through primary winding N_{p1}. At time t_0, S_1 and S_2 are simultaneously turned off with ZVS due to C_{S1} and C_{S2}. The capacitor C_{S1} and C_{S2} begin to charge and C_{S3} and C_{S4} begin to discharge linearly with time. Freewheeling diodes D_1 and D_2 keep conducting. This mode is ended when the voltage of S_1 and S_2 increases to V_{in} and the voltage of S_3 and S_4 decreases to zero.

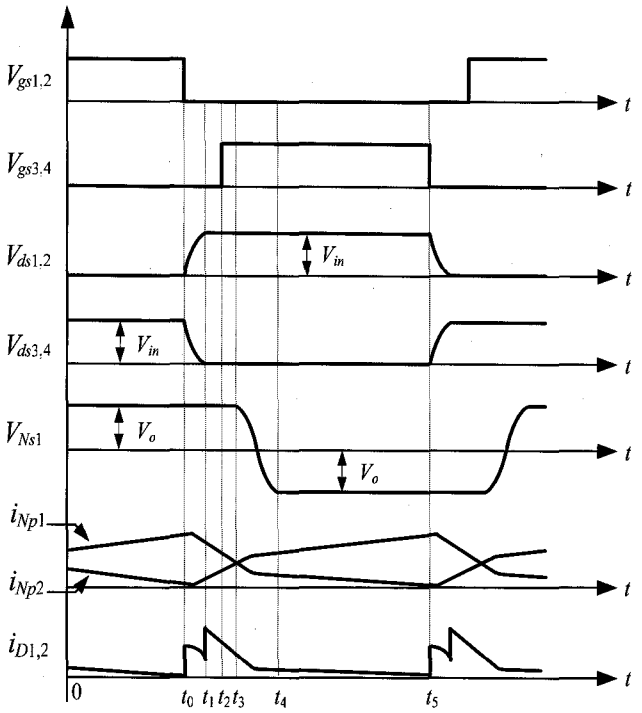
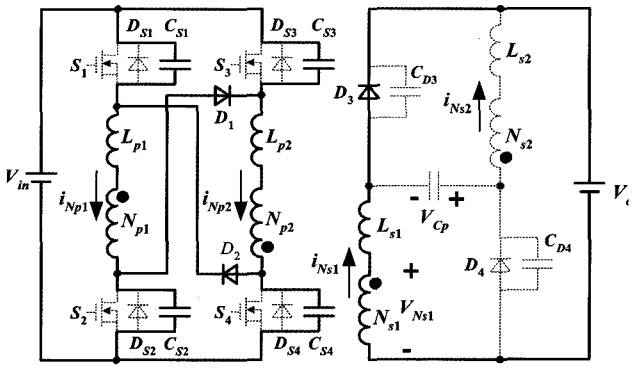
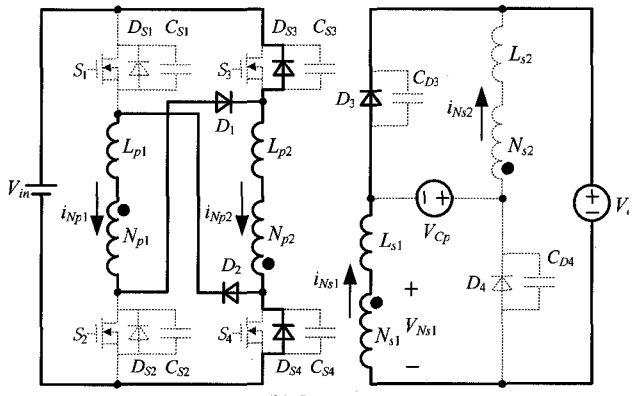


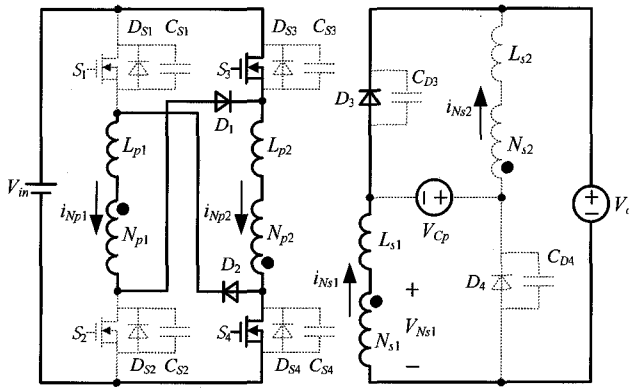
Fig. 2 Key waveforms of the proposed converter



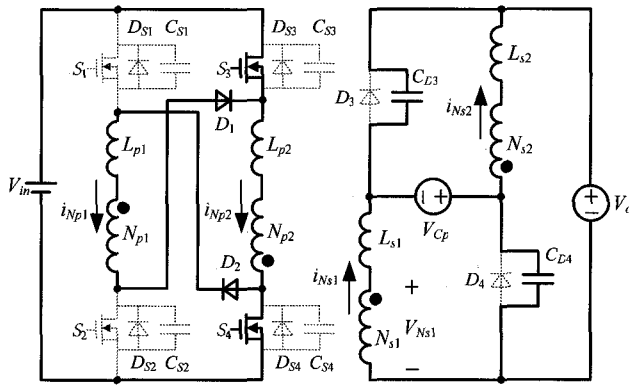
(a) [t_0, t_1]



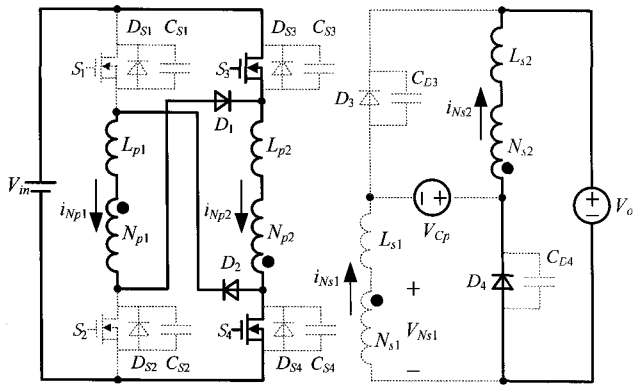
(b) [t_1, t_2]



(c) [t_2, t_3]



(d) [t_3, t_4]



(e) [t_4, t_5]

Fig. 3 Equivalent circuits of the switching modes

$$i_{Np1}(t)=\frac{I_p}{2}(1+\cos\omega_{r1}(t-t_0)) \tag{1}$$

$$i_{Np2}(t)=\frac{I_p}{2}(1-\cos\omega_{r1}(t-t_0)) \tag{2}$$

$$v_{ds1}(t)=v_{ds2}(t)=\frac{I_pZ_{r1}}{4}\sin\omega_{r1}(t-t_0) \tag{3}$$

$$v_{ds3}(t)=v_{ds4}(t)=V_{in}-\frac{I_pZ_{r1}}{4}\sin\omega_{r1}(t-t_0). \tag{4}$$

where I_p is the current of i_{Np1}at time t_0.

$$\omega_{r1}=\sqrt{\frac{2}{(L_p+L_s/n^2)C_S}},Z_{r1}=\sqrt{\frac{2(L_p+L_s/n^2)}{C_S}}.$$

2) Mode 2 [t_1, t_2] [Fig. 3 (b)]: At time t_1, D_{S3} and D_{S4} conduct. The voltage of S_1 and S_2 keep constant value of V_{in}. I_{Np1} decreases linearly and i_{Np2} increases linearly due to the effect of the input voltage and output voltage.

$$i_{Np1}(t)=i_{Np1}(t_1)-\frac{V_{in}+V_o/n}{L_p+L_s/n^2}(t-t_1) \tag{5}$$

$$i_{Np2}(t)=i_{Np2}(t_1)+\frac{V_{in}+V_o/n}{L_p+L_s/n^2}(t-t_1). \tag{6}$$

In this mode, the voltage of the S_1 and S_2 is sustained at V_{in} because of D_1 and D_2's clamping.

3) Mode 3 [t_2, t_3] [Fig. 3 (c)]: At time t_2, S_3 and S_4 can be turned on with ZVS at this time. When i_{Np1} equals to i_{Np2}, i_{Ns1} decreases to zero, and secondary rectifier diode D_3 turns off simultaneously.

4) Mode 4 [t_3, t_4] [Fig. 3 (d)]: At time t_3, D_3 turns off; the voltage of transformer winding begins to reverse. During this interval, L_{p1} and L_{s1} resonate with the junction capacitor of the rectifier diode D_3, C_{D3} is charged. Meanwhile, leakage inductance L_{p2} and L_{s2} resonate with the junction capacitor of the rectifier diode D_4, C_{D4} is discharged. This mode will be ended when C_{D4} is fully discharged, and D_4 begins to conduct. During this interval, the voltage of D_3 and D_4 is well clamped due to the clamping capacitor C_p and output capacitor C_f.

$$v_{CD3}(t)=2V_o(1-\cos\omega_{r2}(t-t_3)) \tag{7}$$

$$v_{CD4}(t)=2V_o\cos\omega_{r2}(t-t_3) \tag{8}$$

$$i_{Ns2}(t)=\frac{2V_o}{Z_{r2}}\sin\omega_{r2}(t-t_3)=I_S\sin\omega_{r2}(t-t_3) \tag{9}$$

where $\omega_{r2}=\frac{1}{\sqrt{(n^2L_p+L_s)C_D}},Z_{r2}=\sqrt{\frac{n^2L_p+L_s}{C_D}}$.

In the circuit loop of C_{D3}-V_o-C_{D4}-V_{Cp}, the voltage oscillation and spike of the rectifier diodes D_3 and D_4 is eliminated due to the clamping of V_o and V_{Cp}.

5) Mode 5 [t_4, t_5] [Fig. 3 (e)]: At time t_4, rectifier diode D_4 begins to conduct. Magnetizing current increases in a negative direction and power is transferred from the input source to the load through primary winding N_{p2}. i_{Np1} reduces and i_{Np2} increases linearly. This mode is finished when S_3 and S_4 are turned off at time t_5. The operation of the next half switching cycle is symmetrical with that of this half switching cycle.

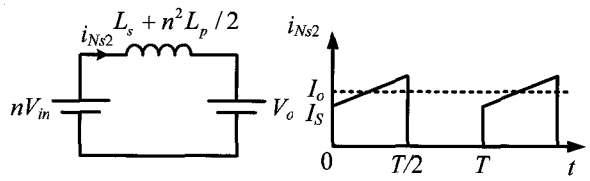
$$i_{Np1}(t)=i_{Np1}(t_3)-\frac{V_{in}-V_o/n}{L_p+L_s/n^2}(t-t_4) \tag{10}$$

$$i_{Np2}(t)=i_{Np2}(t_3)+\frac{V_{in}-V_o/n}{L_p+L_s/n^2}(t-t_4). \tag{11}$$

3. Theoretical Analysis

3.1 Output Characteristics

The switches of the proposed converter run at a duty cycle of around 50%. The output voltage is related to the loads and the input voltage. Considering the very short interval between t_0-t_3 in steady state, simplified equivalent circuit when S_3 and S_4 conduct and current waveform of secondary winding N_{s2} are illustrated in Fig. 4.



(a) (b)

Fig. 4 (a) Simplified equivalent circuit when S_3 and S_4 conduct; (b) current waveform of secondary winding N_{s2}

According to the equivalent circuit in Fig. 4. (a), we can get

$$V_o = nV_{in} - (n^2 L_p + 2L_s)\frac{I_o - I_s}{T/2}. \tag{12}$$

where I_o is the output current.

Substituting equation (7) into (12) yields

$$V_o = \frac{nV_{in} - 2f_s I_o (n^2 L_p + 2L_s)}{1 - 4f_s \sqrt{(n^2 L_p + 2L_s) C_D}}. \tag{13}$$

Fig. 5 illustrates the curve of the output voltage V_o which varies with transformer leakage inductances when the input voltage V_{in}=270V, output power P_o=2kW, turns ratio N_{p1}:N_{p2}:N_{s1}:N_{s2}=16:16:11:11, duty ratio is at 0.48.

We can obtain that the higher the leakage inductances, the more reduction of the output voltage.

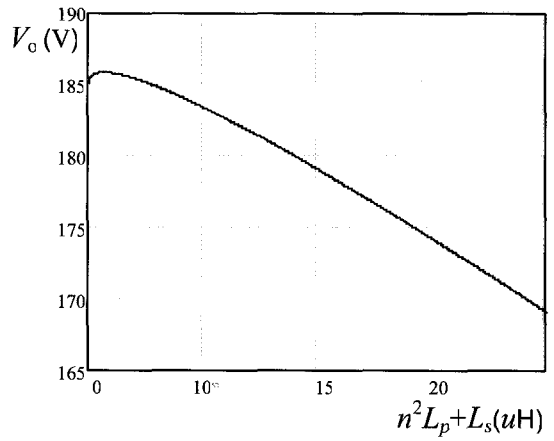


Fig. 5 The curve of output voltage versus leakage inductances

3.2 ZVS Condition of the Proposed Converter

The proposed converter can achieve ZVS operation on conditions:

1) The capacitor C_{S3} and C_{S4} must be discharged to zero in mode 2, from (4), we can derive

$$\frac{1}{4} I_p Z_{r1} \geq V_{in}. \tag{14}$$

From the current waveform of winding N_{s2} in Fig. 4. (b), we can get

$$I_p = n(2I_o - I_s) \tag{15}$$

Substituting (15) into (14), and combining (7) with them, we can get

$$n^2 L_p + L_s \geq \frac{2C_S V_{in}^2 + 4\sqrt{2C_D C_S} V_{in} V_o + C_D V_o^2}{I_o^2} \tag{16}$$

From (16), we can see that it is easy to achieve ZVS when output current I_o and leakage inductance are higher. However, increasing the value of leakage inductances will cause a decrease of the output voltage. In experiment, ZVS is achieved when the output current I_o is above 4A.

2) The dead time T_{off} when all switches are turned off must be given as

$$(t_1 - t_0) \leq T_{off} \leq (t_3 - t_0) \tag{17}$$

Combing (4),(7),(15) and (17) yields

$$T_{off} \geq t_1 - t_0 = \frac{1}{\omega_{r1}} \arcsin \frac{2V_{in}}{nZ_{r1}(I_o - V_o / Z_{r2})} \tag{18}$$

3.3 Design consideration for the clamping capacitor C_p

In steady-state operation, the clamping capacitor C_p resonates with the secondary leakage inductance L_{s1} and L_{s2}.The equivalent resonant circuit is illustrated in Fig. 6.

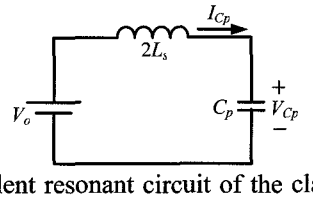


Fig. 6 Equivalent resonant circuit of the clamping capacitor and secondary leakage inductance

$$i_{Cp}(t) = I_{Cp}(t_0)\cos\omega_{r3}(t - t_0) + \frac{V_o - V_{Cp}(t_0)}{Z_{r3}} \sin\omega_{r3}(t - t_0) \tag{19}$$

$$v_{Cp}(t) = V_o - (V_o - V_{Cp}(t_0))\cos\omega_{r3}(t - t_0) + I_{Cp}(t_0) Z_{r3} \sin\omega_{r3}(t - t_0) \tag{20}$$

where $\omega_{r3} = \frac{1}{\sqrt{2L_s C_p}}, Z_{r3} = \sqrt{\frac{2L_s}{C_p}}$.

According to (19) and (20), we can obtain that increase of the capacitance of the clamping capacitor C_p will result in large resonate current, it will increase the conduction loss. Decrease of the capacitance of the clamping capacitor C_p will result in increase of the resonate frequency; the loss during the switching period will increase. Hence, the capacity of the clamping capacitor C_p will be synthetically considered. In experiment $1uF$ metalized polymer capacitor is adopted.

4. Experiment Results

In order to verify the operation principle of the proposed converter, a prototype is built in our lab with the following parameters:

- Input voltage: V_{in}=270V;
- Output voltage: V_o=180V;
- Rated output power: P_o=2kW;
- Switches S_1-S_4 : IXFK48N50;
- Rectifier diodes D_3 and D_4: DSEI60−10A;
- Freewheeling diodes D_1 and D_2: DSEI60−06A;
- Transformer core: dual EE55 ferrite core; turns ratio: N_{p1}:N_{p2}:N_{s1}:N_{s2}=16:16:11:11;
- Leakage inductance: Lp1=3.2uH; Lp2=3.1uH; Ls1=1.9uH; Ls2=1.7uH;
- Clamping capacitor: C_p=1uF;
- Output filter capacitor: C_f=470uF;
- Switching frequency: f_s=100kHz;
- Duty ratio is constant at 0.48.

Fig. 7 shows the experimental waveforms of the proposed converter under 2kW output condition. Fig. 7 (a) shows the gate drive signal V_{gs1} and drain to source voltage V_{ds1} of S_1. It can be seen from Fig. 7 (a) that the main switch $S_1$is turned on with ZVS. Fig. 7 (b) illustrates the gate drive signal of S_3, the current of primary winding N_{p2}. Fig. 7 (c) shows the gate drive waveform of S_1 and Voltage waveform of rectifier diode D_3, which illustrates that the voltage of the secondary winding is clamped by the output capacitor. Fig. 7 (d) gives the gate drive waveform of S_1 and voltage waveform of the clamping capacitor C_p. It can be seen from Fig. 7 (d) that the voltage of C_p fluctuates according to the output voltage V_o.

The efficiency curve of the proposed converter is shown in Fig. 8. It can be seen from Fig. 8 that the efficiency of the proposed converter at full load condition is about 95.8%.

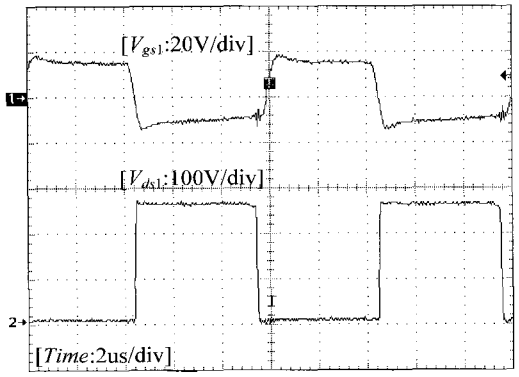


Fig. 7 (a) The gate drive waveform and the drain source voltage waveform of S_1

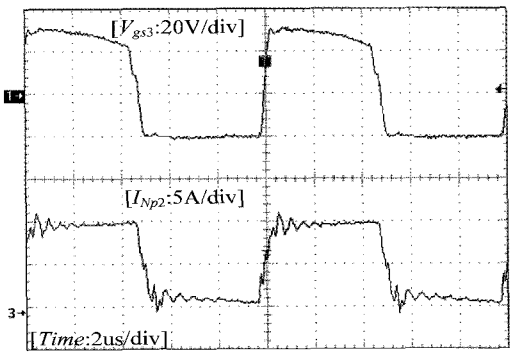


Fig. 7 (b) The gate drive waveform of S_3 and the current of primary winding N_{p2}

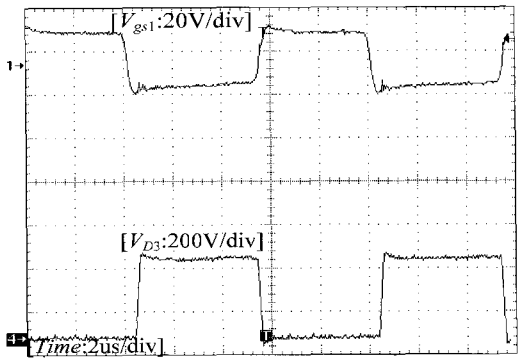


Fig. 7 (c) The gate drive waveform of S_1 and Voltage waveform of rectifier diode D_3

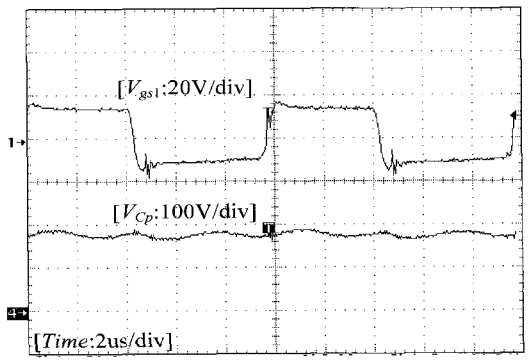


Fig. 7 (d) The gate drive waveform of S_1 and voltage waveform of the clamping capacitor C_p

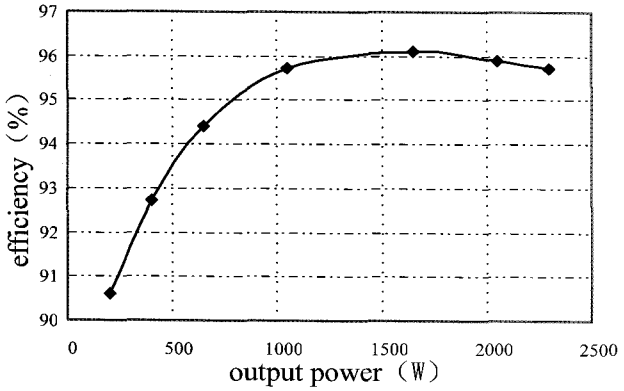


Fig. 8 The curve of relationship between efficiency and output power

5. Conclusion

A novel zero-voltage-switching push-pull DC-DC converter for high input voltage and high power applications is proposed in this paper. Analysis of the proposed converter, output characteristics, ZVS condition and design consideration for the clamping capacitor are discussed. Through experiments it is shown that the proposed converter has following characteristics:

1) The proposed converter can reduce the voltage stress of switches to the input voltage. The two clamping diodes eliminate the voltage spike of the switches.
2) All switches run at a duty cycle of around 50%, zero-voltage-switching of main switches are realized with function of transformer leakage inductance and the parasitic capacitors of the switches without using additional passive or active circuits. Therefore, high power density and high efficiency will be realized.
3) Secondary full-wave rectifier with a clamping capacitor is used to eliminate the voltage oscillation and spike of the rectifier diodes due to the reverse recovery. So the electromagnetic interference of the proposed converter is reduced effectively.
4) The proposed converter is very suitable for high input voltage and high power industrial applications.

References

[1] Shoyama, M., Harada, K, "Zero-voltage-switched push-pull DC-DC converter," *in Proc. IEEE PESC'91*, 1991, pp. 223–229.

[2] Shoyama, M., Harada, K, "Zero-voltage-switching realized by magnetizing current of transformer in push-pull current-fed DC-DC converter," *in Proc. IEEE PESC'93*, 1993, pp. 178–184.

[3] Jianping Ying, Qiuhua Zhu, Hua Lin, Zhigan Wu, "A zero-voltage-switching (ZVS) push-pull DC/DC converter for UPS," *in Proc. IEEE PEDS'03*, 2003, pp. 1495–1499.

[4] Yuancheng Ren, Ming Xu, Ching-Shan Leu, Fred. C.Lee. A family of high power density bus converters[C]. IEEE PESC, 2004: 527 – 532.

[5] G. Ivensky, A. Abramovitz, M. Gulko and S. Ben-Yaakov. A resonant DC-DC transformer[C]. IEEE APEC, 1992: 731 – 737.

[6] Ryan, M.J.; Brumsickle, W.E.; Divan, D.M.; Lorenz, R.D., "A new ZVS LCL-resonant push-pull DC-DC converter topology," IEEE Trans. Industry Applications, vol.34, no.5, pp. 1164–1174, Oct, 1998.

[7] Lin, F.-J.; Wai, R.-J.; Lee, C.-C. , "Fuzzy neural network position controller for ultrasonic motor drive using push-pull DC-DC converter," in *Proc. IEE Control Theory and Applications, 1999*, pp. 99–107.

[8] Fanghua Zhang, Haihong Qin, Huizhen Wang, Yangguang Yan, "Freewheeling current in push-pull forward converter," *in Proc. IEEE PESC'03*, 2003, pp. 353–358.

[9] Rong-Tai Chen, Yung-Yaw Chen, "A novel single stage push pull converter with integrated magnetics and ripple-free input current," *in Proc. IEEE PESC'04*, 2004, pp. 3848–3853.

[10] Peng Xu; Mao Ye; Lee, F.C. , *"Single magnetic push-pull forward converter featuring built-in input filter and coupled-inductor current doubler for 48 V VRM," in Proc. IEEE APEC'02*, 2002, pp. 754–759.

[11] Feng Han, Xu Dehong, Matsui, M., "A novel ZVT circuit for interleaving two-transistor forward converter, "Freewheeling current in push-pull forward converter," *in Proc. IEEE APEC'00*, 2000, pp. 843–849.

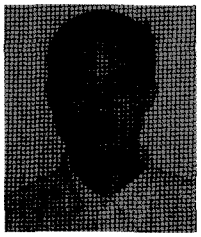
[12] Dharmraj V.Ghodke and K.Muralishnan,"A 1.5 KW two switch forward zczvs converter using primary side clamping," *in Proc. IEEE PESC'03*, 2003, pp.893-898;

[13] Redl, R., Balogh, L., Edwards, D.W., "Optimum ZVS full-bridge DC/DC converter with PWM phase-shift control: analysis, design considerations, and experimental results," *in Proc. IEEE APEC'94*, 1994, pp. 159–165.

[14] Xinbo Ruan, Yangguang Yan, "Soft-switching techniques for PWM full bridge converters," *in Proc. IEEE PSEC'00*, 2000, pp. 634–639.

[15] Pinheiro, J.R., Barbi, I., "The three-level ZVS-PWM DC-to-DC converter," IEEE Trans. Power Electron., vol.8, no.4, pp. 486–492, Oct, 1993.

[16] Canales, F., Barbosa, P., Lee, F.C. , "A zero-voltage and zero-current switching three-level DC/DC converter," IEEE Trans. Power Electron., vol.17, no.6, pp. 898–904, Nov, 2002.



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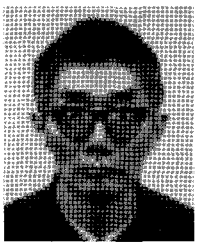

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