더블게이트 MOSFET의 동적 특성

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Dynamic characteristics for Double Gate MOSFET

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이 논문은 2002년도 군산대학교 두뇌한국21사업에 의하여 일부 지원되었음

요 약

본 논문에서는 메인게이트와 사이드게이트를 갖는 더블게이트 구조의 동작 온도에 따른 전기적 특성들을 조사하였다. 실온(300K)에서 뿐만 아니라 극저온(77K)에서도 전류-전압특성이 우수함을 알 수 있었다. 또한 우수한 DG MOSFET의 동적 특성들을 얻기 위한 최적의 조건들은 메인게이트 길이가 50㎚이고 사이드게이트 길이가 70㎚, 그리고 드레인 전압이 2V이상 인가되어야 함을 알 수 있었다. 실온에서 문턱전압은 약 0.358V, 77K에서는 약 0.513V를 얻을 수 있었다. 또한 온-오프 특성이 우수하여 디지털 소자로서 유용하게 사용될 수 있을 것이다.

ABSTRACT

In this paper, we have investigated electrical characteristics by action temperature of double gate structure that have main gate and side gate. Could know current-voltage characteristic is superior in ultra low temperature (77 K) as well as in room temperature (300 K). Also, conditions of most suitable for get superior DG MOSFET's dynamic characteristics are main gate length of 50㎚ and side gate length of 70㎚ and could know that should be approved more than voltage 2V. Also, this DG MOSFET usefully use may as digital device because on-off characteristic is superior.

키워드

double gate, main gate, side gate, temperature-dependent, on-off characteristic

Ⅰ. INTRODUCTION

Outstanding improvements in the speed and performance of CMOS technology continue to be made[1]. Due to the considerable progress of CMOS technology over the last two decades, scaling technology and device dimensions are approaching the fundamental physical limitation of nanometer regime[2-3]. As the gate lengths of MOSFET are scaled down to a sub-100nm regime, there are key issues to be considered in device

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design.[4] As scaling down of MOSFET proceeds, extremely shallow source and drain (S/D) junctions are required in order to suppress the short channel effects(SCE) and the formation of these ultra shallow S/D junctions with low resistances is one of the most important technologies[5-6].

In this paper, we investigate double-gate(DG) MOSFET structure, which has main gate(MG) and side gates(SG), to solve SCE problems. We investigate optimum side gate voltage for side gate length in order to analyze characteristics of device and the variety of threshold voltage for each side gate length.

Also, we investigate the frequency characteristics and digital applications using the DG MOSFETs. The single most important measurement in MOSFET work is a plot of the capacitance of a MOSFET structure as a function of its dc gate bias. Then, we investigated a C-V (capacitance-voltage) plot. We have simulated using ISE-TCAD tool for characteristics analysis of device.

Ⅱ. DEVECE STRUCTURE AND SIMULATION

Fig. 1 shows the cross sectional view of the DG MOSFET. The gate oxide thickness of main gate and side gate is 3nm and 4nm, respectively. A long side gate results in performance degradation due to increased resistance. Under

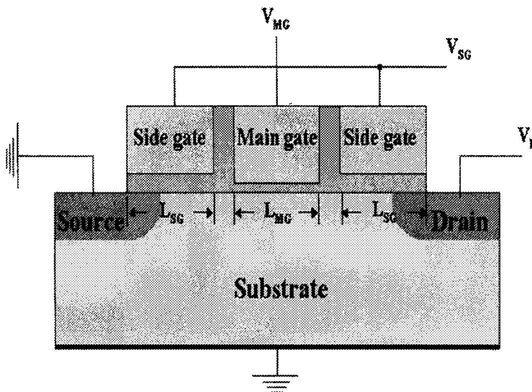

Fig. 1. The structure of DG MOSFET

the main gate region, the local threshold voltage implantation has the merit of reducing parasitic junction capacitance and the side gate can easily induce the inversion layer due to the lower threshold voltage. We have extracted threshold voltage for each side gate length using INSPECT in the ISE-TCAD tool.

We have compared with threshold voltages to obtain optimum value for each side gate length and each side gate voltage. The main gate length is scaled down from 90nm to 40nm and side gate length is scaled down from 90nm to 40nm to investigate optimum side gate length for each gate length. Also, both of side gates for each gate length are biased from 5V to 1V. We have investigated threshold voltage for characteristics analysis of DG MOSFET. To extract threshold voltage, drain voltage and side gate voltage are biased with 1.5V and 3.0V, respectively.

Ⅲ. RESULTS AND DISCUSSION

The calculated current-voltage relations are shown in Fig. 2.

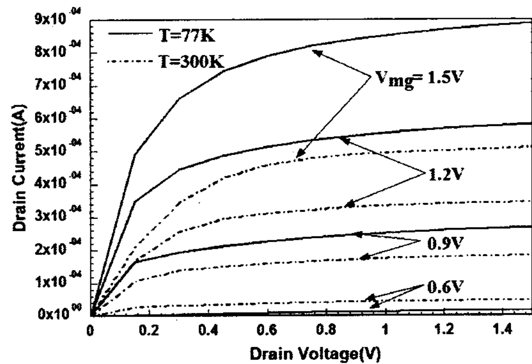

Fig. 2. Comparison of temperature-dependent current-voltage relation

In the graph of current-voltage characteristic we show temperature-dependant current-voltage relation for DG MOSFET when the main gate length and side gate length is 50nm and 70nm. We have investigated the temperature-dependent charac-teristics of current-voltage, and drain

voltage is changed from 0V to 1.5V at V_{MG}=1.5V and V_{SG}=3.0V. We have obtained very good current-voltage curves for 77K.

Fig. 3 shows temperature-dependent threshold voltage characteristics. DG MOSFET has the main gate length of 50nm and the side gate length of 70nm. It shows that device threshold voltage decreases with higher temperature regardless of side gate voltage. When side gate voltage is 3V, threshold voltage of DG MOSFET is about 0.358V at 300K, about 0.513V at 77K.

We have investigated the variety of threshold voltage for side gate voltage according to change of side gate length. Then, drain voltage is 0.05V and side gate voltage is biased from 1V to 5V.

Fig. 4 shows threshold voltage roll-off characteristics for side gate voltage in the DG MOSFET with main gate length of 50nm. When side gate voltage is 5V, threshold voltage of

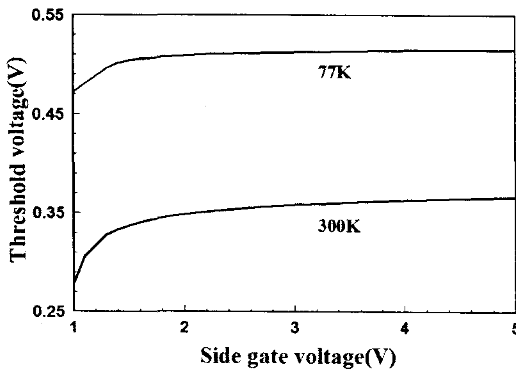

Fig. 3. Comparison of temperature-dependent threshold voltage

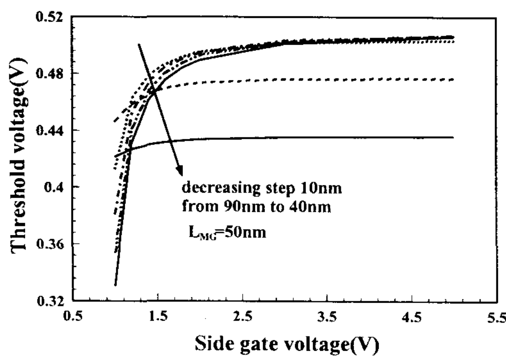

Fig. 4. Various threshold voltages for side gate voltage

DG MOSFET with side gate length of 90nm is about 0.504V.

As side gate voltage is 2V, threshold voltage is about 0.496V. We know that deviation of threshold voltage is about 14mV and very small. But if side gate voltage is 2V below, the deviation of threshold voltage becomes larger. We know that if side gate voltage is 2V above, threshold voltage for side gate voltage hardly changes regardless of side gate length. The results show that after strong inversion layer is formed, additional side gate bias is not necessary.

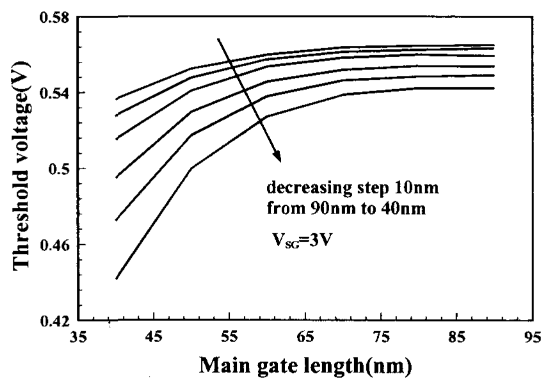

Fig. 5. The threshold voltages for main gate length

Fig. 5 shows threshold voltage roll-off characteristics for main gate length of simulated device. As main gate length is decreasing, we know threshold voltage is lower. As main gate length is reducing from 90nm to 40nm, the deviation of threshold voltage for DG MOSFET with side gate length of 70nm is about 27mV. As a result, we know that DG MOSFETs maintain minimum roll-off characteristics with side gate bias of 3V and side gate length of 70nm above. As shown in Fig. 4 and 5, we know that optimum side gate length is 70nm and optimum side gate voltage is 2V above.

Fig. 6 shows the on-off state characteristics of DG MOSFET with 50nm main gate. When side gate voltage and side gate length are 2V and 70nm above, respectively, we have obtained excellent on-off state for DG MOSFET. Therefore, this DG MOSFET may be applied usefully in digital devices.

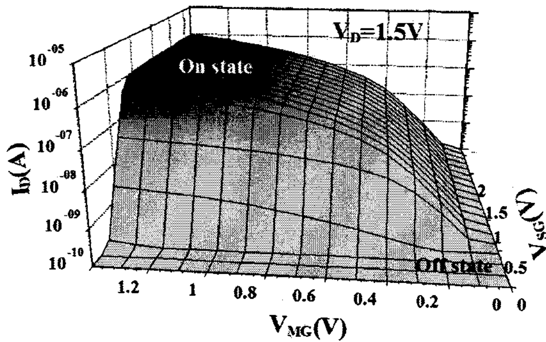

Fig. 6. On-off state of double gate MOSFET with 50nm main gate

Fig. 7 shows capacitance-voltage and transconductance characteristics of DG MOSFETs when the side gate lengths are 40nm, 70nm, respectively.

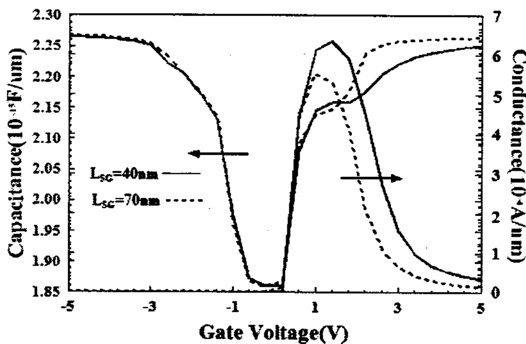

Fig. 7. Capacitance-voltage and trans-conductance curves of DG MOSFETs

The bias conditions of DG MOSFET are V_{SG}=3.0V and V_D=2.0V. We have changed the main gate voltage from 5.0V to 5.0V. Here, cut-off frequency is 41.4GHz in L_{SG}=70nm. The capacitance-voltage plot has accumulation, depletion and inversion layer. The capacitance starts out at a maximum in accumulation layer and drops in depletion layer. However, when the inversion condition is appeared, the inversion layer can actually change its charge at the same rate as the ac signal. It should be pointed the threshold voltage is about 0.59V. The total capacitance increases again to the maximum.

When the side gate voltage is 3V, we know that capacitance-voltage curves are bending at near the main gate voltage of 1.8V as shown in Fig.7. This phenomenon does not appeared when the side gate voltage is below 2V. We know that this phenomenon appeared due to the interactive capacitance between main gate and side gate. That is, we can ignore the depletion capacitance after strong inversion is occurred, but we can't ignore the interactive capacitance due to the oxide layer between main gate and side gate. Therefore, we think that this phenomenon is occurred in the capacitance-voltage curve. We know that two capacitance-voltage curves for side gate length are distinguished after occurring of this phenomenon. As the side gate lengths are increased, the transconductance is reduced and picked at about 1.8V when the side gate length is 40nm.

Ⅳ. CONCLUSION

We have investigated DG MOSFET, which has main gate and side gates. Side gates are used to suppress SCE. That is, when side gate voltage and side gate length are 2V and 70nm above, respectively, we have obtained the minimum SCE for DG MOSFET. We know that optimum side gate voltage for each side gate length is about 2V in the main gate 50nm. We have obtained a very good characteristic of current-voltage for 77K. The cut-off frequency is 41.4GHz in L_{SG}=70nm in this device. Therefore, we have obtained excellent electrical characteristics and very high cut-off frequency for DG MOSFET. We know this structure has many advantages when it is applied to multi-input NAND gate. Finally, the simulated results in this study, we think, can be used for the basis data of DG MOSFET in the ICs fabrication.

Ⅴ. ACKNOWLEDGMENTS

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