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Fabrication of a (100) Silicon Master Using Anisotropic Wet Etching for Embossing

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ABSTRACT

To fabricate a (100) silicon hard master, we used anisotropic wet etching for the embossing. The etching chemical for the silicon wafer was a TMAH 25% solution. The anisotropic wet etching produces a smooth sidewall surface inclined at 54.7°, and the surface roughness of the fabricated master is about 1 nm. After spin coating an organic-inorganic sol-gel hybrid resin on a silicon substrate, we used the fabricated master to form patterns on the silicon substrate. Thus, we successfully obtained patterns via the hot embossing technique with the (100) silicon hard master. Moreover, by using a single hydrophobic surface treatment of the master, we succeeded in achieving uniform surface roughness of the embossed patterns for more than ten embossments.

Key words*: *Silicon master, Anisotropic wet etching, Embossing, Surface roughness

1. Introduction

The demand for optical waveguides in short-distance telecommunications will increase rapidly in the near future because of the need to transfer optical signals between computers and chips.[1] The type of optical fiber that has been widely used for long-distance telecommunications is too costly to be used for the waveguides in short-distance telecommunications.[2,3] Recently, an inexpensive embossing technique was developed to fabricate low-cost waveguides for short-distance telecommunications.[4-8] In the embossing technique, a patterned plate called a master is used to fabricate the planar optical waveguide, and patterns are formed by pressing the patterned master on a substrate and curing it.[9] The patterns embossed on the substrate should be well duplicated from the patterns on the master. In order to produce the well duplicated patterns, the surface of the master should be very smooth for easy separation between the pattern and the master. In particular, the sidewall roughness of the master is critical for the easy separation.

Several materials, such as nickel, silica, and silicon, have been used to fabricate masters with various advantages. A master fabricated with nickel has a long life-span but the fabrication procedure is expensive because it requires a process called *lithographie galvanoformung abformung*. In addition, when fabricated with this process, the nickel master has a high level of roughness. Masters can also be fabricated with silicon by means of deep Reactive Ion Etching (RIE), and this method is popular because of the wide availability of the microelectromechanical system. Deep RIE, however, produces a scallop structure on the silicon sidewall, and an experienced operator is needed to control the structure.

To fabricate a (100) silicon hard master, we used anisotropic wet etching. With this method, we obtained an atomically smooth etched surface because the anisotropic wet etching utilizes the varied bonding strengths of different crystal planes. Moreover, by using a single hydrophobic surface treatment of the master, we successfully repeated the embossing process more than ten times on organic-inorganic hybrid resin without any defaults.

2. Experimental Procedure

To fabricate the silicon masters, we used 4" (100) p-type silicon wafers. As shown in Fig. 1, the silicon wafers were oxidized in an electric furnace to form a 500 nm silicon oxide film on the wafers as a protection layer for silicon etching. Next, with the aid of a standard semiconductor photolithographic process, we used a photomask (Microimage) to transfer patterns onto the oxidized silicon wafers. We then selectively removed the silicon oxide film on the substrate with Buffered Oxide Etching (BOE) solution (J. T. Baker Chemical Company) for 30 min after the photolithographic process. To remove the residual photoresist (Clariant), we used REMOVE100 (Clariant) at 60°C.

Anisotropic wet etching with a TMAH 25% (Nepes) solution was used to etch the silicon surface. First, we heated the TMAH 25% solution to 80°C. We then put the silicon wafer with oxide patterns into the TMAH 25% solution and shook the solution to detach any H_2 bubbles from the silicon

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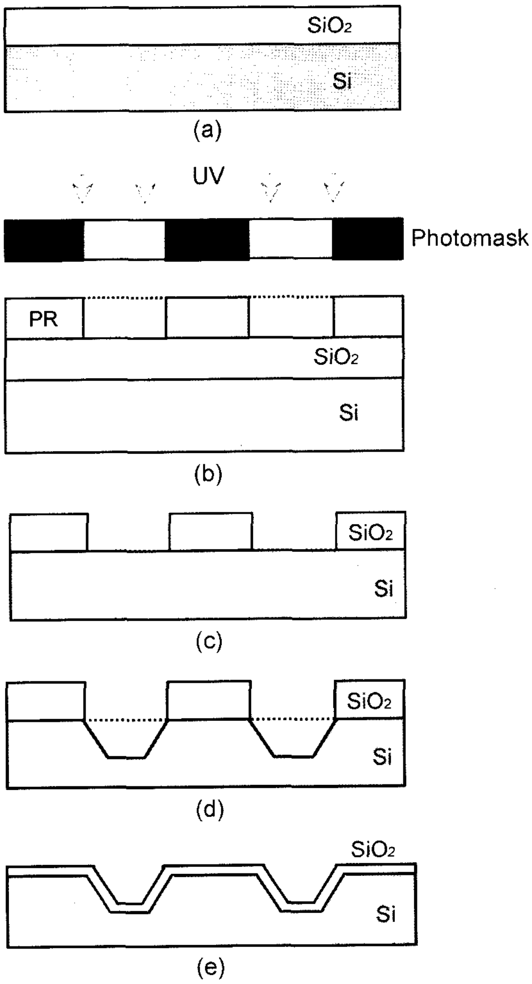

Fig. 1. Fabrication process of a silicon hard master: (a) SiO_2 growth, (b) photolithography, (c) SiO_2 removal, (d) Si etching, and (e) SiO_2 growth and surface treatment.

surface. The last step was necessary because undetached bubbles may hinder the etching of the silicon, resulting in an unevenly etched silicon surface. Finally, we used the BOE solution to remove any residual silicon oxide film from the substrate.

The surface of the fabricated silicon master should have a hydrophobic characteristic to ensure that the master can be separated smoothly from the formed patterns. To increase the hydrophobicity of the etched silicon surface, we oxidized the surface again to form the silicon oxide film and we coated the oxide surface with perfluoroalkylsilane (PFAS) film.

We also used deep RIE to fabricate a silicon master and we compared its surface roughness with that of the silicon master fabricated with anisotropic wet etching.

By using the hot embossing technique at a low pressure and temperature, we successfully formed patterns with the aid of the fabricated silicon masters. First, we spin coated an organic-inorganic sol-gel hybrid resin, which was synthesized by alkoxylation of diphenylsilanediol and 3 methacryloxy-propyltrimethoxysilane, onto a silicon substrate. We

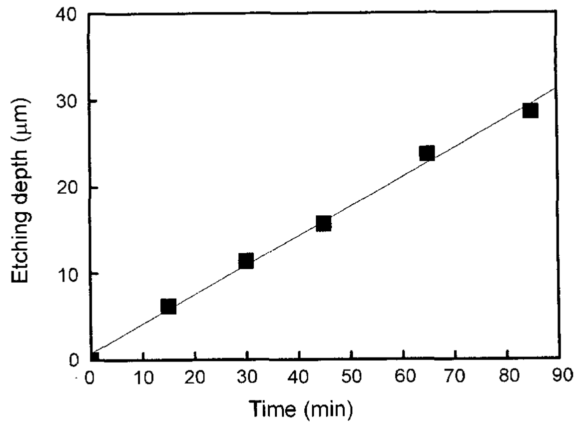

Fig. 2. Etching depth of a p-type (100) silicon wafer in a TMAH 25% solution as a function of the etching time at 80°C.

then added the thermal initiator, benzoyl peroxide, to the resin to ensure the resin hardened when heated. After placing the silicon master, which we fabricated as described in the previous paragraph, on the spin-coated hybrid resin, we applied pressure in the range of 1 kg/cm^3 to 3 kg/cm^3 and heat at 100°C for 10 min in order to transfer the master patterns onto the hybrid resin on the substrate. We then separated the silicon master from the hybrid resin spin-coated substrate. Finally, we analyzed the shape and surface roughness of the formed patterns by using an optical microscope, a Scanning Electron Microscope (SEM), and a Scanning Probe Microscope (SPM).

3. Results and Discussion

By varying the temperature of the TAMH 25% solution from 60°C to 90°C, we determined that the optimum operating temperature for the etching rate of the silicon and the evaporation rate of the solution was 80°C. Fig. 2 shows the etching depth of the p-type (100) silicon surface as a function of etching time at 80°C, and, from the slope, we can determine that the etching rate was 0.33 μm/min.

Fig. 3 shows optical images of cross-sectioned silicon masters fabricated by (a) deep RIE and (b) anisotropic wet etching. As shown in Fig. 3(a), deep RIE, which is the combination of polymer deposition for a sidewall protection and anisotropic etching, produces a scallop structure on the silicon sidewall. This scallop structure increases the surface roughness of the sidewall surface of the silicon master and therefore complicates the separation of the master from the embossed patterns during the final stage of the embossing process. On the other hand, as shown in Fig. 3(b), anisotropic wet etching, which utilizes the variation in atomic bonding strengths among the different crystal planes of silicon single crystal, produces a smooth sidewall surface inclined at 54.7°. Thus, as a result of the anisotropic wet etching, the inclined sidewall surface of the patterns on the silicon master is (111), and this inclined sidewall surface facilitates the

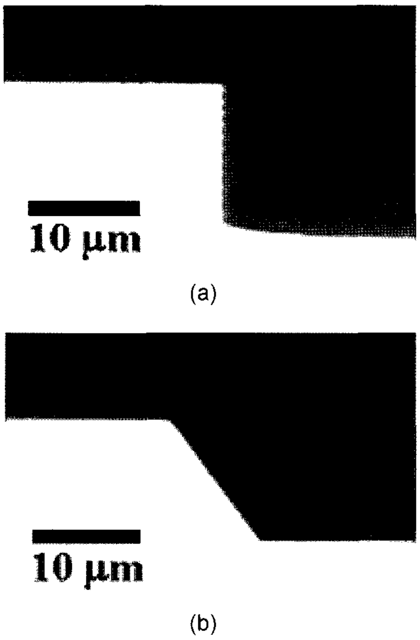

Fig. 3. Shape of the sidewalls fabricated by (a) deep RIE and (b) anisotropic wet etching.

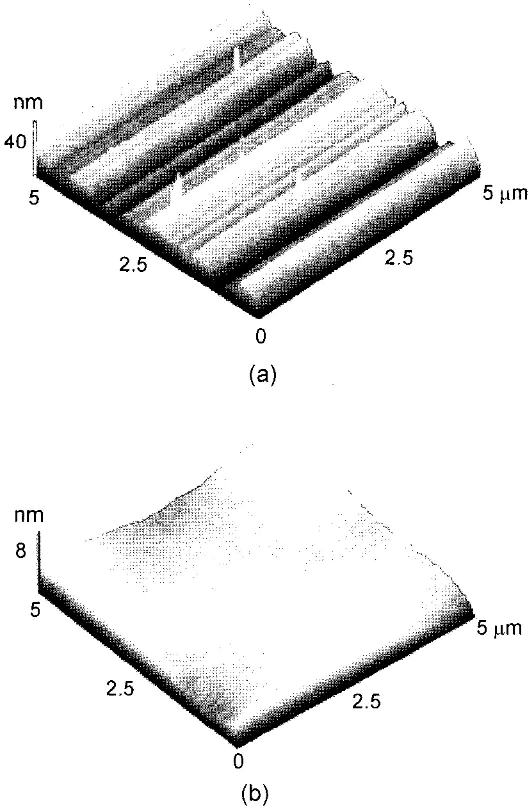

Fig. 4. SPM images of the sidewall surfaces of masters fabricated by (a) deep RIE and (b) anisotropic wet etching.

separation of the master from the embossed patterns due to the open geometry at the top of the master surface.

Fig. 4 shows SPM images of the sidewall surfaces of the masters fabricated by (a) deep RIE and (b) anisotropic wet etching. The sidewall roughness of the masters was measured at 17 nm and 1 nm, respectively. This result shows that anisotropic wet etching is superior to deep RIE with respect to obtaining smooth surfaces.

Fig. 5 shows SEM images of (a) the patterns on the silicon master (50 × 30 μm) and (b) the embossed patterns made by

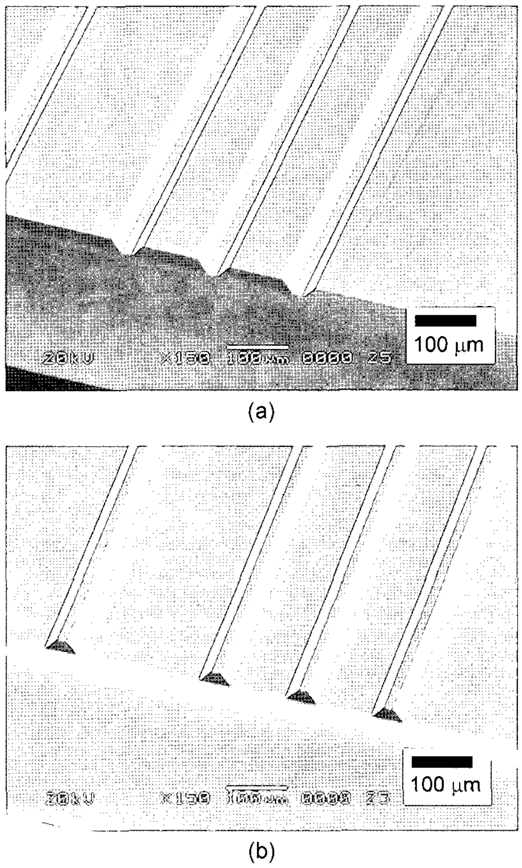

Fig. 5. SEM images of (a) the patterns of the silicon master and (b) the embossed patterns on the silicon substrate.

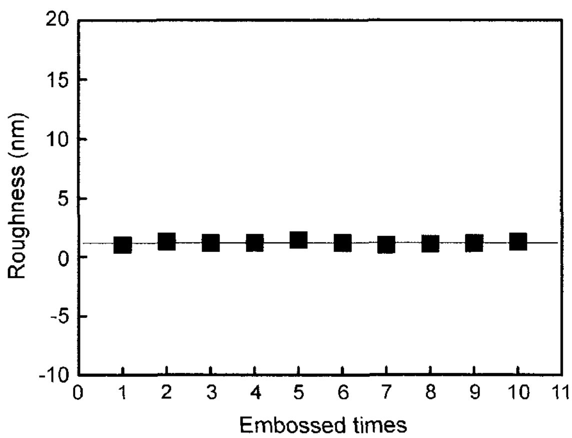

Fig. 6. Roughness variation of the embossed patterns as a function of the embossment frequency.

the hybrid resin, which was spin-coated on a silicon substrate. The embossed patterns on the substrate shown in Fig. 5(b) are well duplicated from the patterns on the master shown in Fig. 5(a). The easy separation of the master from the substrate is the result of the oxidation and the PFAS treatment of the master, which increases the hydrophobicity of the master surface. The inclined sidewall structure also facilitates the separation.

Fig. 6 shows the variation in the roughness of the embossed surface as a function of the embossment frequency. The surface roughness of the embossed patterns was about 1 nm, and it was uniform for more than ten embossment processes with a single surface treatment of the silicon master.

4. Conclusion

By using anisotropic wet etching and a TMAH 25% solution, we fabricated a (100) silicon hard master, and we analyzed its surface property with the aid of an SEM and SPM. We then used PFAS to enhance the hydrophobicity of the master surface for easy separation. In addition, we used a hot embossing technique at a low pressure and temperature to form hybrid resin patterns with the fabricated silicon master. As a result, the formed patterns were shaped almost the same as those of the silicon master, and the surface roughness of the embossed patterns was uniform, at about 1 nm. Moreover, the hybrid resin patterns can be fabricated for more than ten times with a single surface treatment of the silicon master.

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