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Strained SGOI n-MOSFET에서의 phonon-limited 전자이동도의 Si 두께 의존성

(Dependency of Phonon-limited Electron Mobility on Si Thickness in Strained SGOI (Silicon Germanium on Insulator) n-MOSFET)

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요 약

60 nm C-MOSFET 기술 분기점 이상의 고성능, 저전력 트랜지스터를 구현 시키기 위해 SiGe/SiO2/Si위에 성장된 strained Si의 두께가 전자 이동도에 미치는 영향을 두 가지 관점에서 조사 연구하였다. 첫째, inter-valley phonon 산란 모델의 매개변수들을 최적화하였고 둘째, strained Si 반전층의 2-fold와 4-fold의 전자상태, 에너지 밴드 다이어그램, 전자 점유도, 전자농도, phonon 산란율과 phonon-limited 전자이동도를 이론적으로 계산하였다. SGOI n-MOSFET의 전자이동도는 고찰된 SOI 구조의 Si 두께 모든 영역에서 일반적인 SOI n-MOSFET보다 1.5~1.7배가 높음이 관찰 되었다. 이러한 경향은 실험 결과와 상당히 일치한다. 특히 strained Si의 두께가 10 nm 이하일 때 Si 채널 두께가 6 nm 보다 작은 SGOI n-MOSFET에서의 phonon-limited 전자 이동도는 일반 SOI n-MOSFET과 크게 달랐다. 우리는 이러한 차이가 전자들이 strained SGOI n-MOSFET의 반전층에서 SiGe층으로 터널링 했기 때문이고, 반면에 일반 SOI n-MOSFET에서는 캐리어 confinement 현상이 발생했기 때문인 것으로 해석하였다. 또한 우리는 10 nm와 3 nm 사이의 Si 두께에서는 SGOI n-MOSFET의 phonon-limited 전자 이동도가 inter-valley phonon 산란율에 영향을 받는 다는 것을 확인하였으며, 이러한 결과는 더욱 높은 드레인 전류를 얻기 위해서 15 nm 미만의 채널길이를 가진 완전공핍 C-MOSFET는 strained Si SGOI 구조로 제작하여야 함을 확인 했다

Abstract

To make high-performance, low-power transistors beyond the technology node of 60 nm complementary metal-oxide-semiconductor field-effect transistors(C-MOSFETs) possible, the effect of electron mobility of the thickness of strained Si grown on a relaxed SiGe/SiO2/Si was investigated from the viewpoint of mobility enhancement via two approaches. First, the parameters for the inter-valley phonon scattering model were optimized. Second, theoretical calculation of the electronic states of the two-fold and four-fold valleys in the strained Si inversion layer were performed, including such characteristics as the energy band diagrams, electron populations, electron concentrations, phonon scattering rate, and phonon-limited electron mobility. The electron mobility in an silicon germanium on insulator(SGOI) n-MOSFET was observed to be about 1.5 to 1.7 times higher than that of a conventional silicon on insulator(SOI) n-MOSFET over the whole range of Si thickness in the SOI structure. This trend was good consistent with our experimental results. In particular, it was observed that, when the strained Si thickness was decreased below 10 nm, the phonon-limited electron mobility in an SGOI n-MOSFET with a Si channel thickness of less than 6 nm differed significantly from that of the conventional SOI n-MOSFET. It can be attributed this difference that some electrons in the strained SGOI n-MOSFET inversion layer tunnelled into the SiGe layer, whereas carrier confinement occurred in the conventional SOI n-MOSFET. In addition, we confirmed that in the Si thickness range of from 10 nm to 3 nm, the phonon-limited electron mobility in an SGOI n-MOSFET was governed by the inter-valley phonon scattering rate. This result indicates that a fully depleted C-MOSFET with a channel length of less than 15 nm should be fabricated on an strained Si SGOI structure in order to obtain a higher drain current.

Keywords: SGOI, phonon-limited mobility, strained Si, mobility, simulation

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Ⅰ. Introduction

As the gate channel length of complementary metal-oxide-semiconductor field-effect transistors (C-MOSFETs) shrinks below 90 nm, transport enhanced field-effect transistors, which are classified as non classical C-MOSFETs, will inevitably become necessary. Such transistors are beyond the capabilities of a conventional bulk silicon structure. In addition, as the channel length of C-MOSFETs becomes less than 70 nm, the device structure will require ultra-thin-body silicon-on-insulator C-MOS FETs(UTB SOI C-MOSFETs) for system LSI circuits. The UTB SOI C-MOSFET requires an SOI thickness of less than 25 nm, which degrades both the electron mobility and the hole mobility, because of carrier confinement in the quantum well as a result of the nano-scale SOI thickness (i.e., a quantum-mechanical effect).

This degradation of the electrical characteristics can be overcome by utilizing strained silicon on a relaxed silicon-germanium-on-insulator(SGOI) structure, forming an SGOI C-MOSFET[1]. Such C-MOSFETs are thus being considered as a promising device structure[1~2]. The SGOI C-MOS FET enhances both the electron mobility and the hole mobility by reducing carrier scattering. This happens because the biaxial tensile strain increases the difference in sub-band energy between the two-fold (Δ_2) valleys and four-fold(Δ_4) valleys in the conduction band, thus enhancing the electron occupancy of the two-fold valleys. Our group previously reported the effect on electron-mobility of utilizing nano-scale strained Si grown on SGOI, showing that the ratio of electron-mobility enhancement in the resulting n-MOSFETs is 1.6 times higher than that in conventional SOI MOSFETs[3]. In addition, our group experimentally demonstrated that the electron mobility in strained SGOI is influenced by the Si thickness in the SGOI structure, as well as by the Ge concentrations in the SiGe layer[4].

To simulate the electronic states in the nano-scale thickness of Si in an SGOI n-MOSFET, it is most important to employ an accurate scattering model. Although many papers based on theoretical work have been published[5, 6, 7~12], a definite mobility model for a strained Si MOSFET has not yet been published. Thus, our simulation required modifying and optimizing the parameters of the mobility model based on a bulk Si MOSFET.

The aim of this report is to investigate the dependency of the phonon limited electron mobility in an inversion layer on the thickness of nano-scale strained Si grown for SGOI MOSFETs. An additional goal is to study the electrical phenomena of SGOI MOSFETs through theoretical simulation using a quantum-mechanical model for the electronic states of both the two- and four-fold valleys, including such characteristics as the energy band diagram, electron occupancy, electron concentration, phonon scattering rate, and phonon-limited electron mobility.

Ⅱ. Simulation Model

1. Sub-band calculation

In general, the conduction band of unstrained bulk Si has six equivalent valleys along the <100> direction of the Brillouin zone. These six valleys in the inversion layer on the (100) surface are classified into two degenerate valleys with an effective mass of $0.916m_0$, and four degenerate valleys with an effective mass of $0.19m_0$. When a tensile strain is applied by inserting a relaxed SiGe layer, in contrast to an unstrained Si layer, the energy of the conduction band minima of the four-valleys on the in plain <100> axes rises with respect to the energy of the two-valleys on the <100> axes perpendicular to the plane[13~14]. The splitting energy band gap, ΔE_{strain}, between the two lowered and the four raised degenerate valleys is given by

$$\Delta E_{strain} = 0.67\ x\ \text{eV},$$

where x is the Ge concentration of the relaxed $Si_{1-x}Ge_x$ layer[15].

To simulate the electrical characteristics of a MOSFET accurately, it is most important to extract the transverse electric field correctly by using an appropriate model. In our simulation, the transverse electric field was extracted by applying a two-dimensional(2D) quantum-mechanical(QM) model based on a self-consistent solution of the Poisson-Schrödinger equations with different conduction effective masses in the two-fold and four-fold valleys. In addition, the surface carrier concentrations occupying each sub-band in the strained Si were calculated by using the following equations:

$$\frac{1}{N_i} = \frac{2m_{d2}k_BT}{\pi\eta^2} F_0\left(\frac{E_f - E_i}{k_BT}\right) \tag{1}$$

$$\frac{1}{N'_i} = \frac{4m_{d4}k_BT}{\pi\eta^2} F_0\left(\frac{E_f - E_{i'} - E_{strain}}{k_BT}\right) \tag{2}$$

where N_i and N'_i are the carrier concentrations of the ith sub-band of the two- and four-fold valleys, respectively. $F_0(x) = \ln[1 + \exp(x)]$, and E_f is the Fermi potential.

2. Scattering model

The inversion layer mobility in a Si MOSFET is determined by three scattering mechanisms, i.e., coulomb scattering, phonon scattering, and surface roughness scattering. Since both the biaxial strains induced by inserting a SiGe layer and the wave-function modulation caused by the thin Si mainly affect phonon scattering in the effective field range of 0.05~0.5 MV/cm[5], we assumed that the surface roughness scattering was negligible. We also did not consider the coulomb scattering mobility, since an undoped channel is suitable for an ultra-thin top Si thickness of less than 20 nm in order to avoid mobility degradation[16]. By this reasoning, we mainly considered the phonon-limited electron mobility and simulated it by applying the relaxation time approximation (RTA) method[17~18] with a 1.5 V gate bias. The f-type, g-type, and inter- and intra-valley phonon scattering were all calculated so as to determine the phonon limited electron mobility by using following equations.

First, the momentum relaxation rate[17~18] (E) for deformation potential scattering by intra-valley acoustic phonons from the ith sub-band to the jth sub-band, is given by the following equations:

$$\frac{1}{\tau_{ac2}^{i,j}} = \frac{n_{v2}^{ac} m_d D_{ac}^{\ 2} k_B T}{\eta^3 \rho s_l^{\ 2}} \frac{1}{W_{i,j}} \tag{3}$$

$$W_{i,j} = \{\int \xi_i^{\ 2}(z)\xi_j^{\ 2}(z)dz\}^{-1} \tag{4}$$

$$\frac{1}{\tau_{ac4}^{i,j}} = \frac{n_{v4}^{ac} m_d D_{ac}^2 k_B T}{\eta^3 \rho s_l^2} \frac{1}{W'_{i,j}} \tag{5}$$

$$W'_{i,j} = \{\int \xi'_i{}^2(z)\xi'_j{}^2(z)dz\}^{-1} \tag{6}$$

where n_{v2}^{ac} is the degeneracy of the valley with respect to intra-valley scattering, m_d is the density of state mass in each valley, D_{ac} is the deformation potential due to acoustic phonons, ρ is the crystal density, and S_l is the sound velocity. $W_{i,j}$ is interpreted as the effective thickness of the wave function of the ith sub band with respect to z[6].

Second, the inter-valley phonon scattering can be obtained from the following four equations. The momentum relaxation rate(E), for inter-valley phonon scattering from the ith sub-band to the jth sub-band is given by

$$\frac{1}{\tau_{inter2}^{i,j}} = \sum_k^{\{f\}} \frac{n_{v2\to4}^f m_{d4} D_k^{\ 2}}{\eta\rho E_k} \frac{1}{V_{i,j}} (N_k + \frac{1}{2} \pm \frac{1}{2})(\frac{1 - f(E \mu E_k)}{1 - f(E)}) \tag{7}$$

$$\frac{1}{\tau^{i,j}_{\text{inter4}}} = \sum_{k}^{\{f\}} \frac{n^{f}_{v4\to4} m_{d4} D_k^{\,2}}{\eta\rho E_k} \frac{1}{W'_{i,j}} (N_k + \frac{1}{2} \pm \frac{1}{2})(\frac{1-f(E \mu E_k)}{1-f(E)}) \quad (8)$$

$$\frac{1}{\tau^{i,j}_{\text{inter4}}} = \sum_{k}^{\{g\}} \frac{n^{g}_{v4\to4} m_{d4} D_k^{\,2}}{\eta\rho E_k} \frac{1}{W'_{i,j}} (N_k + \frac{1}{2} \pm \frac{1}{2})(\frac{1-f(E \mu E_k)}{1-f(E)}) \quad (9)$$

$$\frac{1}{\tau^{i,j}_{\text{inter4}}} = \sum_{k}^{\{f\}} \frac{n^{f}_{v4\to2} m_{d2} D_k^{\,2}}{\eta\rho E_k} \frac{1}{V'_{i,j}} (N_k + \frac{1}{2} \pm \frac{1}{2})(\frac{1-f(E \mu E_k)}{1-f(E)}) \quad (10)$$

where $n^{f}_{v4\to4}(=4)$ is the degeneracy of the valley into which the electrons are scattered; D_k and E_k are the deformation potential and energy of the kth inter-valley phonon, respectively; N_k is the occupation number of the kth inter-valley phonon; the plus and minus signs in the expression $\left(N_k + \frac{1}{2} \pm \frac{1}{2}\right)$ correspond to phonon emission and phonon absorption, respectively; and $f(E)$ is the Fermi-Dirac distribution function. $n^{f}_{v2\to4}$, $n^{g}_{v4\to4}$, and $n^{f}_{v4\to2}$ are the degeneracies of the valleys into which the electrons are scattered, and are taken as 2, 1, and 2, respectively. To provide the parameters for the inter-valley phonon scattering model, the Ferry model[19] was applied in the present work. We considered equivalent inter-valley scattering, i.e., from X valley to X valley, not from X valley to L valley. In addition, although we recognize that the big momentum conservation involving optical phonon scattering could be changed by strain, we did not take into account the phenomena because it has not yet been published quantitatively and explicitly so far.

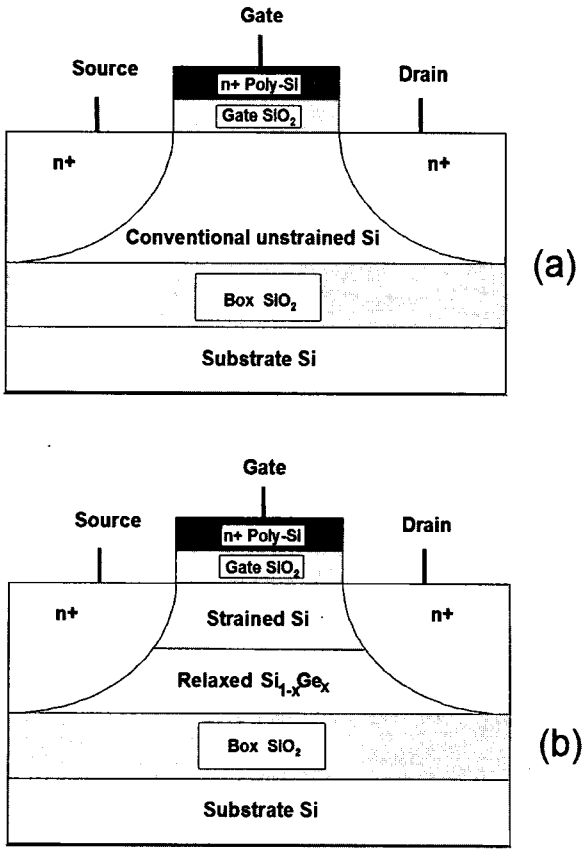

그림 1. 도식적 다이어그램 구조 (a) unstrained SOI n-MOSFET (b) strained SGOI n-MOSFET

Fig. 1. Schematic diagram illustrating the structure of (a) an unstrained SOI n-MOSFET and (b) a strained SGOI n-MOSFET.

3. Mobility calculation

The total relaxation times, $\tau_2^i(E)$ and $\tau_4^i(E)$, for electrons with energy E in the ith sub-band of the two- and four-fold valleys, respectively, are given by

$$\frac{1}{\tau_2^i}(E) = \frac{1}{\tau_{ac2}^i}(E) + \frac{1}{\tau_{\text{inter2}}^i}, \quad (11)$$

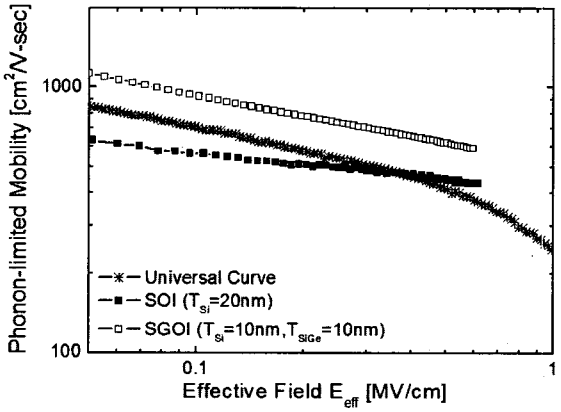

그림 2. 수정된 산란변수를 사용한 본 논문의 phonon-limited 이동도와 참고문헌 22의 실험값과의 비교

Fig. 2. Phonon-limited mobility calculated using the scattering parameter modified in this work and compared with experimental data obtained from reference [22].

$$\frac{1}{\tau_4^i}(E)=\frac{1}{\tau_{ac4}^i}(E)+\frac{1}{\tau_{inter4}^i} \tag{12}$$

By using Matthiessen's equation, the carrier effective mobility μ_{eff} in a longitudinal field can be described approximately as the sum of three scattering terms[20~21]

$$\frac{1}{\mu_{eff}}=\frac{1}{\mu_c}+\frac{1}{\mu_{ph}}+\frac{1}{\mu_{sr}} \tag{13}$$

where μ_c is the coulomb scattering mobility, μ_{ph} is the phonon limited mobility, μ_{sr} is the surface roughness mobility, and μ_{eff} is the effective mobility. Among the three mobility components, we only considered the phonon limited electron mobility for the conventional SOI and SGOI structures as described above.

The electron mobilities in the ith sub-band of the two-fold and four-fold valleys are given by the following equations:

$$\mu_2^i=\frac{e\int_{E_i}^{\infty}(E-E_i)\tau_2^i(E)(-\partial f/\partial E)dE}{m_{c2}\int_{E_i}^{\infty}(E-E_i)(-\partial f/\partial E)dE} \tag{14}$$

$$\mu_4^i=\frac{e\int_{E_{i'}}^{\infty}(E-E_i')\tau_4^i(E)(-\partial f/\partial E)dE}{m_{c4}\int_{E_{i'}}^{\infty}(E-E_i')(-\partial f/\partial E)dE} \tag{15}$$

where m_{c2} and m_{c4} are the conductivity masses of the two- and four-fold valleys, respectively. The total electron mobility is given by

$$\mu=\left(\sum_i \mu_2^i N_i+\sum_{i'}\mu_4^{i'}N_{i'}\right)(N_s)^{-1} \tag{16}$$

where N_S is the total surface carrier concentration in the inversion layer.

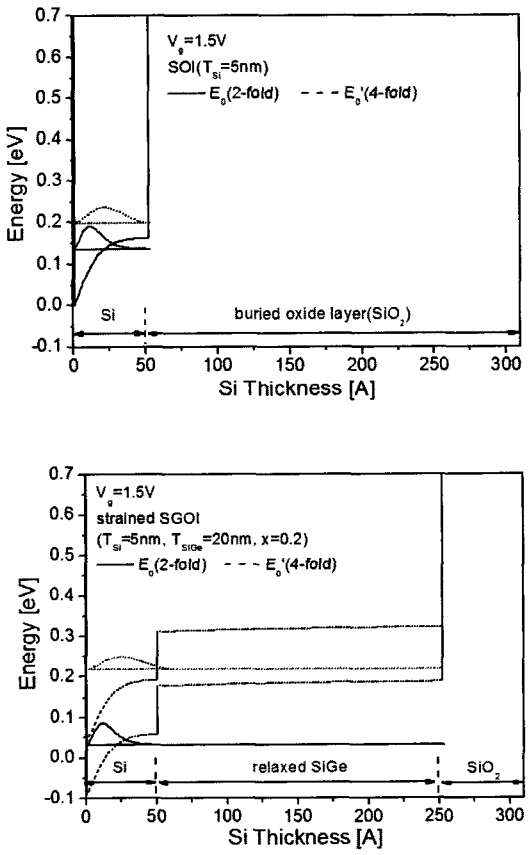

그림 3. 1.5 V 게이트 전압 인가시 기저 상태의 전자확률밀도와 에너지 준위 (a) 5 nm 일반 SOI n-MOSFET (b) 20 at% Ge농도를 갖는 20 nm SiGe 층 위의 5 nm strained Si

Fig. 3. Electron probability and the energy level of the ground state under a 1.5 V gate bias condition, for (a) a 5 nm thick conventional SOI n-MOSFET and (b) a 5 nm strained Si layer on a 20 nm SiGe layer with 20 at% Ge concentration.

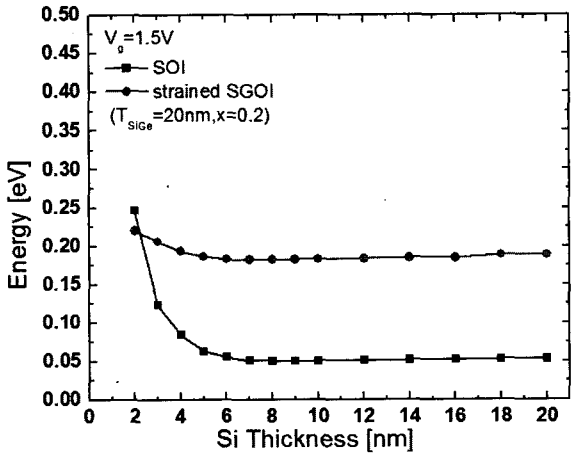

그림 4. Si 두께의 함수로 나타낸 2-fold(E0)와 4-fold(E0') 기저 상태간의 에너지 차(ΔE)

Fig. 4. Energy difference (ΔE) between the ground states of the two-fold(E0) and four-fold valleys(E0') as a function of the Si thickness.

To investigate the dependency of the phonon-limited electron mobility on the strained inversion layer thickness, we varied the strained Si thickness (T_{Si}) on the relaxed SiGe layer, which had a Ge concentration of 20 at%, as depicted in Fig. 1 the doping concentration of the strained p-type(100) Si layer was 1.5×10^{15} cm^{-3}, and the SiGe layer was simulated under an undoped condition.

Ⅲ. Result and discussion

Utilizing a numerical simulator coded in the C-language, we extracted the phonon limited electron mobility curve as a function of the transverse effective electric field in an inversion layer, and we compared the resulting curve with experimental results.

Figure 2 shows the phonon limited mobility calculated by using the scattering parameter modified in this work, along with experimental data obtained from ref[23]. As illustrated in the figure, the calculated mobility shows a good agreement with the measured data at the middle range of the effective electric fields(Eeff). The results also confirm that the mobility in the strained Si MOSFET is 1.5~1.7 times higher than that in the unstrained Si MOSFET over the whole range of Eeff. The differences between the simulated and experimental results could be due to the fact that the Ge concentration in the SiGe layer was different from that for the reference data.

Figure 3 presents the electron probability and the energy level of the ground state under a 1.5 V gate bias condition, for (a) a 5 nm thickness of Si in a conventional SOI n-MOSFET and (b) a 5 nm thickness of strained Si on a 20 nm SiGe layer with a Ge concentration of 20 at%. The energy value of the ground state in the strained Si SGOI n-MOSFET is lower than that of the conventional SOI n-MOSFET. This is because a tensile strain splits the conduction band valleys, with the two-fold valleys being lowered in energy and the four-fold valleys being raised, thus indicating that volume inversion occurs earlier in the strained Si SGOI n-MOSFET than in the conventional SOI n-MOSFET and the electron confinement occurs more easily.

Figure 4 exhibits the energy difference(ΔE) of the ground state between the two-fold(E0) and four-fold

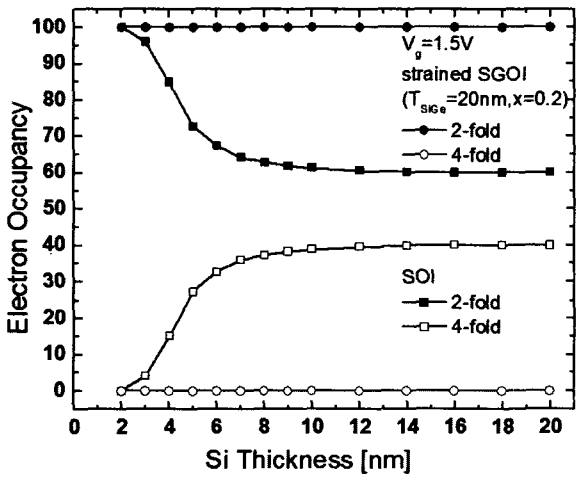

그림 5. Si 두께의 함수로 나타낸 strained Si SGOI n-MOSFET과 일반 SOI n-MOSFET의 전자 점유도

Fig. 5. Electron occupancy in a strained Si SGOI n-MOS FET and in a conventional SOI n-MOSFET as a function of the Si thickness.

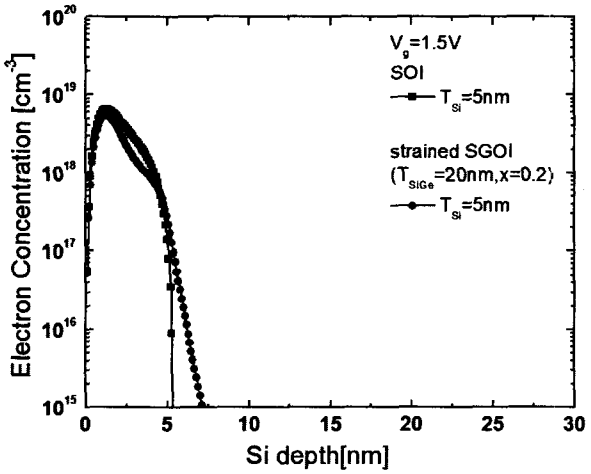

그림 6. Si 표면으로부터의 깊이함수로 나타낸 1.5 V 게이트 전압 인가시 반전층 전자농도

Fig. 6. Electron concentration in the inversion layer as a function of depth from the Si surface under a 1.5 V gate bias condition.

valleys(E0') as a function of the Si thickness. The results indicates that as the Si thickness decreases below 6 nm, the electron energy in the SGOI n-MOSFET increases moderately, while that in the conventional SOI n-MOSFET increases abruptly because of quantum-mechanical effects.

Figure 5 shows the electron occupancy in the strained Si SGOI n-MOSFET and in the conventional SOI n-MOSFET as a function of the Si thickness. For the strained Si SGOI n-MOSFET, most of the electrons are populated in the two-fold valleys and the electron population shows no thickness dependency. Note that ΔE(E0-E0') in the strained Si SGOI n-MOSFET is much larger than that in the conventional SOI n-MOSFET, because of the split conduction band valleys. On the other hand, the electron population of two-fold valleys in the conventional SOI n-MOSFET increased with decreasing Si thickness below 10 nm; this is called the size modulation effect.

Figure 6 presents the electron concentration in the inversion layer as a function of depth from the Si surface under a 1.5 V gate bias condition. The results demonstrate that some electrons in the inversion layer of the strained Si SGOI n-MOSFET tunneled into the SiGe layer, indicating less carrier confinement than in the conventional SOI n-MOSFET.

Figure 7 shows the simulated phonon scattering rate of both the SGOI n-MOSFET and the conventional SOI n-MOSFET, including (a) the total phonon scattering rates, (b) the inter-valley scattering rate, and (c) the intra-valley scattering rate. The figures indicate much less total scattering rate in the SGOI n-MOSFET than in the conventional SOI n-MOSFET. This is because the inter-valley phonon scattering rate of the SGOI n-MOSFET was much lower than that of the conventional SOI n-MOSFET, as shown in Fig. 7(b). In particular, although the intra-valley scattering rate in the SGOI n-MOSFET is not so much different

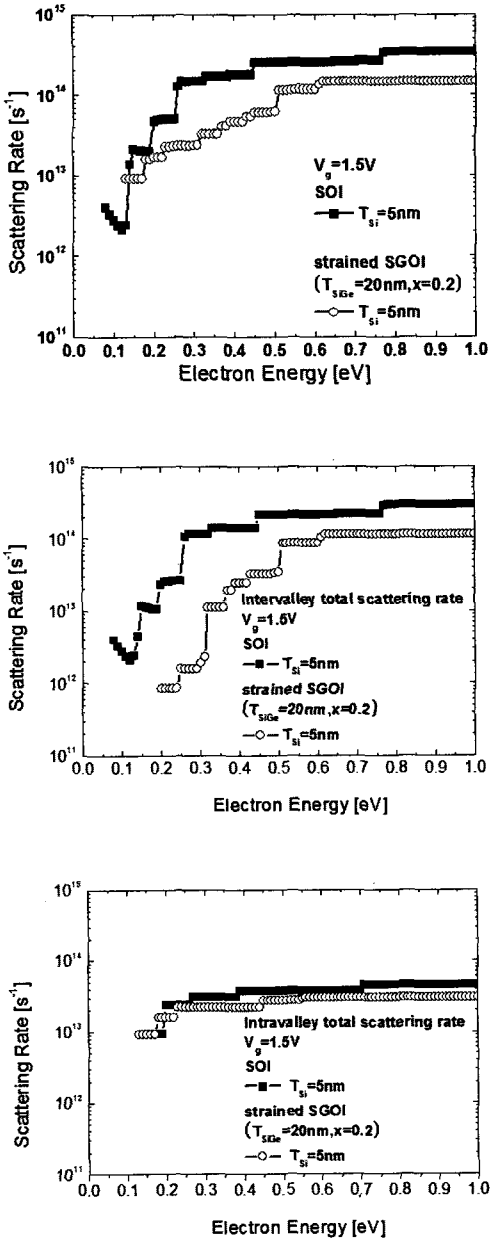

그림 7. 전산모사된 phonon 산란율: (a) 전체 산란율 (b) inter-valley phonon 산란율 (c) intra-valley phonon 산란율

Fig. 7. Simulated phonon scattering rates: (a) the total scattering rate, (b) the inter-valley phonon scattering rate and (c) the intra-valley phonon scattering rate.

from that in the conventional SOI n-MOSFET as shown in Fig. 7(c), the total phonon scattering rates in the SGOI n-MOSFET shows higher than that in the conventional SOI n-MOSFET as shown in Fig. 7(a). This means that the intra-valley phonon

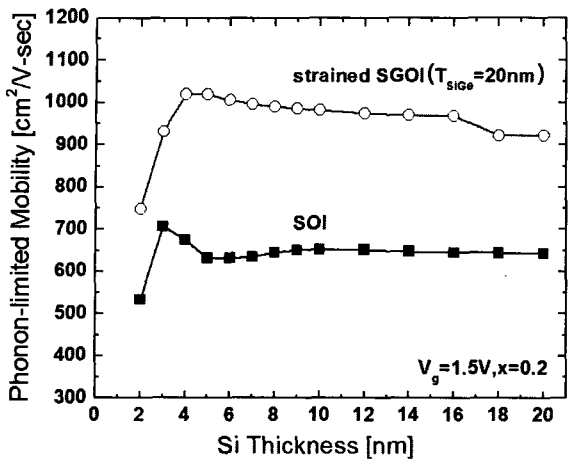

그림 8. SGOI n-MOSFET의 strained Si 두께에 의존성을 갖는 phonon-limited 전자 이동도

Fig. 8. Phonon-limited electron mobility dependency on the strained Si thickness in an SGOI n-MOSFET.

scattering rate did not significantly affect the total phonon scattering rate.

Finally, figure 8 presents the phonon limited electron mobility as a function of the Si thickness. The result shows that the SGOI n-MOSFET has about 1.5 to 1.7 times higher mobility as compared to the conventional SOI n-MOSFET over the whole range of Si thickness; this result is well agreed with many experimental results. Note here that the enhancement of the phonon limited electron mobility was mainly caused by the reduction in the inter-valley phonon scattering rate for the two-fold valleys as shown in Fig. 7(b). In addition, It is observed that in the thickness range from 5 to 10 nm, the phonon-limited electron mobility in the SGOI n-MOSFET as a function of Si thickness is different from that in the conventional SOI n-MOSFET, i.e., for SGOI n-MOS case, it is increased with reducing a Si thickness in , while, it is decreased with reducing a Si thickness in conventional SOI case. It can be attributed this that less occurrence of electron confinement induced by the reduction in the Si thickness happened in the SGOI n-MOSFET case, and electrons in the inversion layer of the SGOI n-MOSFET tunnelled into the SiGe layer as the Si thickness was decreased. Furthermore, it should be noted that the mobility is abruptly dropped at the Si thickness of 2 nm in both structures. This is because all electrons populated at two fold valley, and intra-valley scattering lessened the mobility.

Ⅳ. Conclusion

In this paper, we have investigated the phonon-limited electron mobility as a function of Si thickness by solving the coupled Poisson and Schrödinger equations. We have also studied a mechanism accounting for the mobility enhancement in a strained SGOI n-MOSFET, as well as the Si thickness dependency of the electron mobility. We observed that the phonon limited mobility in a strained Si SGOI n-MOSFET was about 1.5 to 1.7 times higher than that in a conventional n-MOSFET, which is well agreed with many experimental results. In addition, we showed that the mobility enhancement in the strained Si SGOI n-MOSFET was associated more with the reduced inter-valley scattering rate between two-fold and four-fold valleys than with the SOI structure. In particular, we confirmed that in the Si thickness range from 10 nm down to 3 nm, the phonon limited electron mobility in the SGOI n-MOSFET is governed by the inter-valley phonon scattering rate. This result indicates that a fully depleted C-MOSFET with a channel length of less than 15 nm should be fabricated on a SGOI structure in order to obtain a higher drain current.

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