Single-Scan Plasma Display Panel(PDP)를 위한 고속 어드레스 에너지 회수 기법

論 文
54B-9-8

A High Speed Address Recovery Technique for Single-Scan Plasma Display Panel(PDP)

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Abstract - A high speed address recovery technique for AC plasma display panel(PDP) is proposed. Replacing GND switch by clamping diode, the recovery speed can be increased by saving GND hold-time and switching loss due to GND switch also becomes to be reduced. The proposed method is able to perform load-adaptive operation by controlling the voltage level of energy recovery capacitor, which prevents increasing inefficient power consumption caused by circuit loss during recovery operation. Test results with 50″ HD single-scan PDP(resolution = 1366×768) show that less than 350ns of recovery time is successfully accomplished and about 54% of the maximum power consumption can be reduced, tracing minimum power consumption curves.

Key Words : PDP, Energy Recovery, Addressing

I. Introduction

Thanks to the attractive merits such as wide view angle, large screen, high brightness, and thinness, PDP is expected to widen its market share in the digital display market[1]. Fig. 1 shows the simplified PDP structure with three electrodes and matrix cell structure. The PDP cell structure naturally forms capacitances among three electrodes and it causes heat dissipation problem of address drive ICs. To solve this problem, the half-resonant method that is similar to sustain driver suggested by L.F. Webber et. al. and quarter-resonant method have been adopted by PDP makers. Power consumption is successfully reduced with the help of these methods but they cannot be applicable to PDPs requiring a high speed addressing such as large size and high resolution PDPs or single-scan PDPs, due to their slow recovery speed and circuit loss. Another simple method to reduce heat stress is proposed by Y. Sano et. al[2]. It is very simple structure using only resistor but excessive heat dissipated from resistor cannot be accommodated by larger size PDPs.

In this paper, a new address energy recovery technique with fast recovery operation for AC PDP is proposed. This method has load-adaptive power saving characteristic using charge-pumping operation, which enables to consume the minimum address powers according to various images by controlling the voltage level of recovery capacitor. Prototype circuit has been designed and experimented for 50″HD single-scan PDP to show the validity of the proposed circuit.

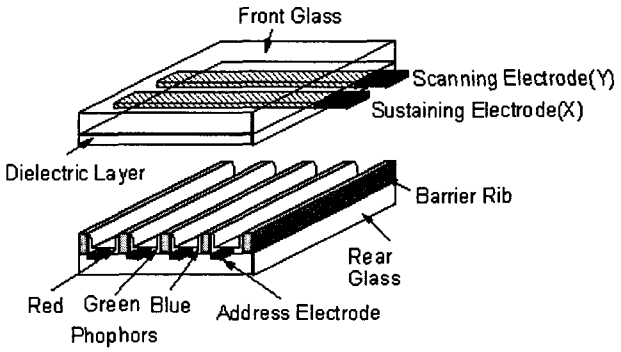

Fig 1. Simplified PDP cell structure

II. Mode analysis

Fig. 2 is the proposed fast address energy recovery circuit(AERC) with address drive IC model at a heavy data switching image. GND switch is replaced by diode only for GND clamping to save GND hold-time. At white dot on/off image that requires severe address power consumption, the address data-switching occurs at each scan line and all capacitances existing among three

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接受日字 : 2005年 5月 18日
最終完了 : 2005年 8月 16日

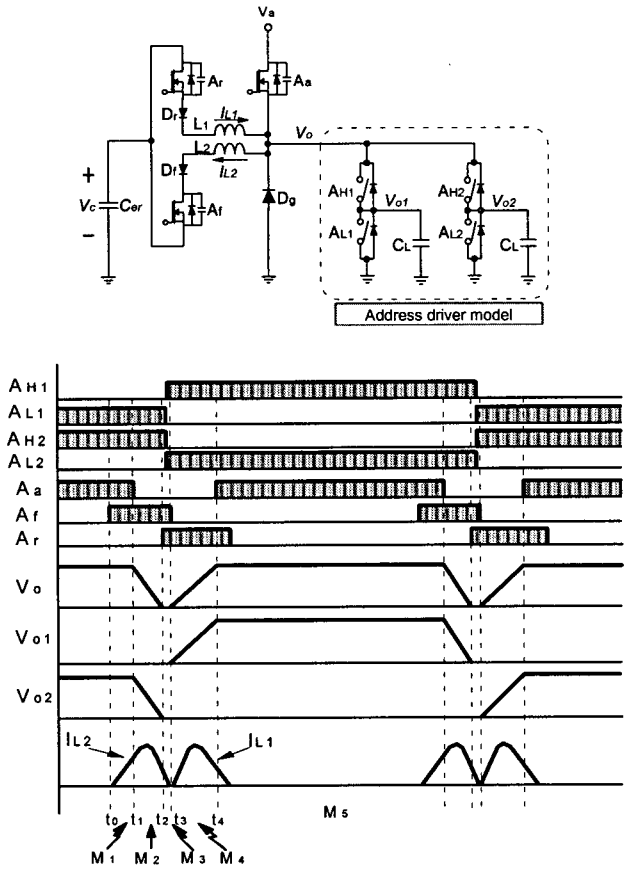

Fig. 2 Proposed method with address IC model

electrodes are applied. In this case, address drive ICs can be modeled by four switches of A_{H1}, A_{L1}, A_{H2}, and A_{L2}, and the load capacitance C_L can be written as

$$C_L = \frac{N_d}{N_M}\left(\frac{1}{2}C_{b,line} + \frac{1}{3}C_{a,line}\right) \quad (1)$$

where N_M : number of recovery circuit blocks,
N_d : number of data lines
$C_{a,line}$: capacitance between address electrodes
$C_{b,line}$: sum of capacitances between one address electrode and each bus electrodes.

Before the analysis, it is assumed that L_1 and L_2 have a same value of L and Parasitic components are ignored.

Mode 1 ($t_0 \le t < t_1$) : Mode 1 begins at t_o when A_f is turned on. Because A_a is already maintained as conducting state, there forms current path including A_a, L_2, D_f and A_f in sequence. Accordingly, I_{L2} linearly is increased with the slope of $(V_a - V_c)/L$ to store the magnetic energy in L_2. The current is expressed as

$$I_{L2} = \frac{V_a - V_c}{L}(t - t_0) \cdot \quad (2)$$

The current built up before the energy charged in panel capacitances is recovered helps to reduce transition time from V_a to zero, which minimizes the shrinkage of address pulse width that is necessary for address discharge. In addition, since this build-up current can be used for the voltage level control of recovery capacitor, the recovery operation becomes different according to load condition.

Mode 2 ($t_1 \le t < t_2$) : When A_a is turned off, the resonant current caused by panel capacitance starts to flow through C_L, L_2, D_f, and A_f and the terminal voltage V_o goes down from V_a to zero. During this mode, the expressions of I_{L2} and V_y are written as:

$$I_{L2} = I_{L2}(t_1)\cos w_c(t - t_1) + \frac{V_a - V_c}{Z}\sin w_c(t - t_1) \quad (3)$$

$$V_o = V_c + (V_a - V_c)\cos w_c(t - t_1) - ZI_{L2}(t_1)\sin w_c(t - t_1) \quad (4)$$

where $Z = \sqrt{L/C_L}$ and $w_c = 1/\sqrt{LC_L}$.

Mode 3 ($t_2 \le t < t_3$) : After mode 2, the diodes of D_g is turned on and V_o is clamped by GND level. Accordingly, the current I_{L2} starts to flow through D_g, D_f, L_2, and A_f. I_{L2} is ramped down to zero with the slope of V_o/L and it can be written as follows:

$$I_{L1} = I_{L1}(t_2) - \frac{V_c}{L}(t - t_2). \quad (5)$$

If data-switching happens during V_o is maintained as around GND level, switching losses of data drive ICs can be reduced.

Mode 4 ($t_3 \le t < t_4$) : After I_{L2} is reduced to zero, the current starts to flow to C_L immediately through A_r, D_r, L_1, and A_{H1} because A_r is already turned on during mode 3. The terminal voltage V_o goes up from zero to V_a. Similar to eqs. (3) and (4) in mode 2, I_{L1} and V_o can be written as

$$I_{L2} = \frac{V_c}{Z}\sin w_c(t - t_3) \quad (6)$$

$$V_o = V_c(1 - \cos w_c(t - t_3)). \quad (7)$$

Mode 5 ($t_4 \le t < t_5$) : After V_o increases to V_a, the rest of magnetic energy of L_1 starts to be recovered toward address voltage source through A_r, D_r, L_1, and the body diode of A_a, which makes the ZVS condition of A_a and A_g. During this mode, I_{L1} decreases to zero with the slope of $(V_c - V_a)/L$, which is expressed as

$$I_{L1} = I_{L1}(t_4) + \frac{V_c - V_a}{L}(t - t_4). \quad (8)$$

Address discharge is induced during A_a is conducting.

III. Operational characteristics

To realize images, all channels of address drive IC generate data and their switching-numbers may be changed from zero to the number of scan lines. The energy recovery capacitor voltage level V_c is important factor to control recovery operation. It is controlled by the build-up current explained in mode 1, which would make V_c tend to maintain a higher voltage level than $V_a/2$ while address recovery circuit comes into no address

data condition, there exits only build-up current flowing into energy recovery capacitor. In this case, V_c eventually increases to V_a and the recovery operation

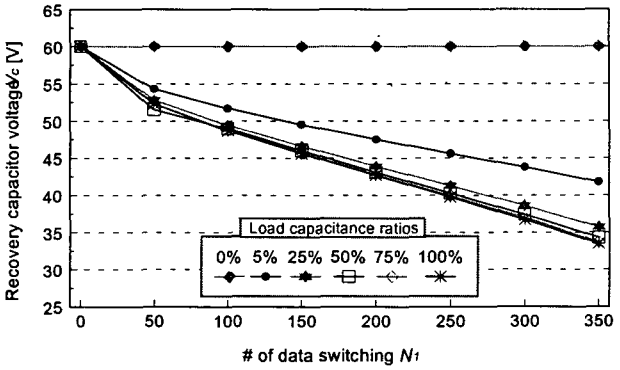

Fig. 3 Vc changes according to CL and N1 at Va = 60V

cannot be performed anymore. As data gets increased, discharge current from energy recovery capacitor becomes increased and it makes V_c lower to some voltage level. Accordingly, the energy stored in panel capacitor starts to be recovered by address recovery circuit. At small data-switching images, recovery operation may not give a help to save power consumption because the inefficient power consumption caused by circulating current for recovery operation is larger than that caused by data-switching. Therefore, this load-dependant recovery operation is desirable characteristic to minimize address power consumption. The expression of V_c can be determined by power-balancing condition of recovery capacitor during recovery operation, which is written as

$$\int (i_{charge} \times v_c)\, dt = \int (i_{discharge} \times v_c)\, dt. \qquad (9)$$

Using this concept, the expression of V_c can be obtained as

$$V_c = \left(1 - \sqrt{\frac{(N_s - N_1)\, C_L}{N_s T_b^2/2L + N_1 C_L\left(1 + \sqrt{1 + (T_b/\sqrt{LC_L})^2}\right)}}\right) V_a \qquad (10)$$

where N_s is the number of total scan electrodes and N_1 is the number of scan electrodes that address data exist on. The current build-up time T_b is defined as t_1-t_0. Calculated V_c with eq. (10) is plotted in Fig. 3 according to C_L and N_1. As C_L and N_1 are decreased, V_c level becomes lowered because the recovery capacitor charging current gets larger than discharging current due to the build-up current. That is to say that the recovery operation can be minimized in case of small data switching images at which power consumption caused by recovery operation is larger than data switching.

IV. Address recovery time TR

Address recovery time T_R is the sum of falling-transition time T_f and rising-transition time T_r.

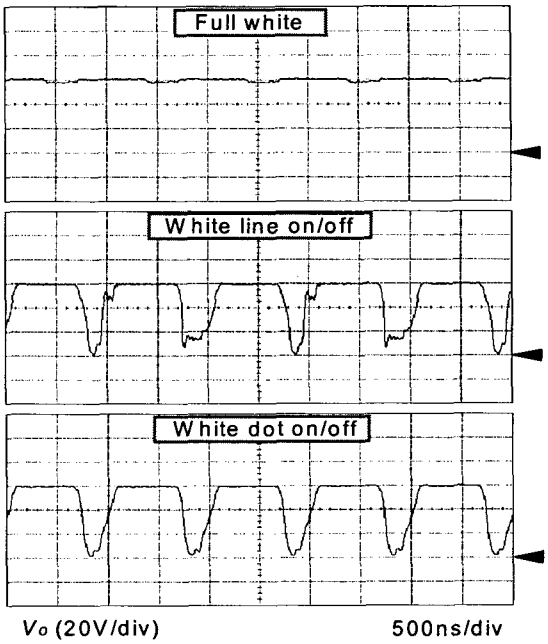

Fig. 4 Measured terminal voltages

The falling-transition time defined by t_2-t_1 is obtained from eq. (4) by replacing V_o with zero. This definition can not be applicable to all load conditions because V_o may not go down to zero according to load conditions. Fortunately, t_2-t_1 is nearly equal to t_3-t_1 which is the time that I_L takes to do down to zero and it can be used for all load conditions. Therefore, using eq. (3), T_f can be approximately expressed as follows:

$$T_f = \sqrt{LC_L}\left(\pi - \tan^{-1}\left(\frac{ZI_{Lo}}{V_a - V_c}\right)\right) \qquad (11)$$

where $I_{Lo} = (V_a - V_c)T_b/L$. Assuming that the circuit does not contain any parasitic components, the rising-transition time T_r is same as eq. (11). Since the transition time of this proposed method is the function of T_b as well as L, the transition time can be shortened by adjusting T_b. It helps to reduce the degradation of discharge margin due to address recovery operation.

V. Experimental results

A prototype circuit of the proposed method has been designed for 50" HD single-scan PDP with specifications of address voltage V_a=60V, total recovery time T_R=350ns, and maximum load capacitance per one circuit block C_L=28nF. Key parameters of L=0.1 μH and

T_b=20ns has been chosen under considering that too small values of L is not difficult to design and too large build-up time may cause a power loss of circuit due to large circulating current. Measured terminal voltages according to data switching are shown in Fig. 4 and less than 350ns of recovery time is successfully accomplished. Full white image which has no data-switching makes the

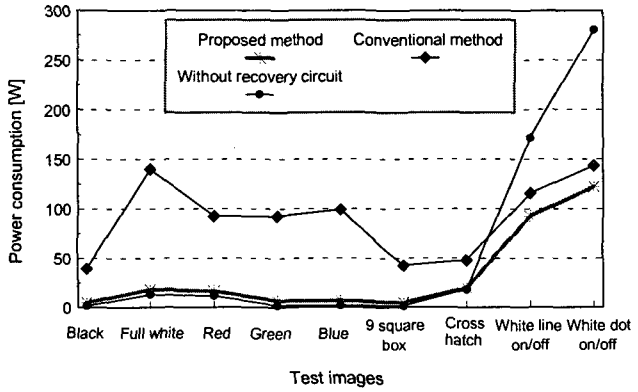

Fig. 5 Address power consumption comparisons

recovery operation stop automatically and heavy data-switching images such as white line on/off and white dot on/off images lower the energy recovery capacitor voltage so that the energy charged in panel capacitance can be recovered. Fig. 5 shows the power consumption comparisons according to address energy recovery methods. It shows that conventional series LC resonant type reduces address power successfully at heavy data-switching images but shows inefficient power dissipation caused by circulating current at small data-switching images. On the other hand, the proposed method can trace the minimum power consumption curve owing to load-adaptive operation. The measured data shows that above 54% of address power can be reduced.

VI. Conclusions

In this paper, a high speed address recovery technique for AC plasma display panel is proposed. By controlling the voltage level of energy recovery capacitor, the proposed method performs load-adaptive operation that shows minimum address power consumption according to displayed images. In addition, recovery speed can be increased by saving the GND hold-time because this method does not use GND switch. Prototype circuit has been implemented for 50" HD single-scan PDP and six blocks was designed to drive overall panel. Test results show that less than 350ns of recovery time is successfully accomplished and the maximum power consumption can be reduced from 280W to 130W.

References

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