A 2-D Model for the Potential Distribution and Threshold Voltage of Fully Depleted Short-Channel Ion - Implanted Silicon MESFET's

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***Abstract*—A new two dimensional (2-D) model for the potential distribution of fully depleted short-channel ion-implanted silicon MESFET's has been presented in this paper. The solution of the 2-D Poisson's equation has been considered as the superposition of the solutions of 1-D Poisson's equation in the lateral direction and the 2-D homogeneous Laplace equation with suitable boundary conditions. The minimum bottom potential at the interface of the depletion region due to the metal-semiconductor junction at the Schottky gate and depletion region due to the substrate-channel junction has been used to investigate the drain-induced barrier lowering (DIBL) and its effects on the threshold voltage of the device. Numerical results have been presented for the potential distribution and threshold voltage for different parameters such as the channel length, drain-source voltage, and implanted-dose and silicon film thickness.**

***Index Terms*—Bottom Potential, drain induced barrier lowering (DIBL), ion-implanted Si-MESFET's, threshold voltage**

I. INTRODUCTION

Silicon MESFET has drawn considerable attention in recent times as a potential device for the future VLSI/ ULSI applications due to the absence of oxide related problems such as radiation/ plasma damages and hot-carrier effects at the gate as in the case of conventional MOS devices and availability of a possible C-MESFET (i.e. complementary MESFET) structure [1-9]. Besides, the channel in the latter device is formed by the inversion layer at the gate oxide-silicon interface and thus the carriers suffer from high normal fields and serious roughness scattering, leading to drastic reduction in effective mobility and transconductance [8]. However, the channel in MESFET is formed in bulk region which is near to the bottom of the active layer and thus carrier mobility is less degraded. This is one of the advantages of MESFET's over the MOS devices. Further, MESFET's have smaller built-in potentials (~0.2V) at the source-channel and channel-drain junctions than that of MOSFET's (~0.9V) [8]. Therefore, MESFET devices do not need to concern much about the punch-though phenomenon which is very common in the latter devices. Since the gate of a MESFET is a Schottky contact, its voltage swing is limited within a small range that depends on the Schottky barrier height of the device. Hence, MESFET is also a good candidate for the low-power applications [8]. However, as the device dimensions shrink to submicrometer region, the short channel effects start to degrade the performance of all kinds of FET devices. The short-channel effect includes the drain induced barrier lowering (DIBL) which is the most pervasive effect in such devices. It is mainly caused by the two dimensional (2-D) electric field distributions in the channel region of the device. In this case, the 2-D potential function is obtained by solving the 2-D Poisson's equation with suitable boundary conditions. Most of the work done so far on the short-channel behavior of the FET devices have been on Si-MOSFET's [10-11] which is the most

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successful and most common transistor currently in use in VLSI. However, despite the possibility of becoming a good contender to MOS devices in the VLSI arena, only a little attention has been given so far for the submicrometer characterization of the Si-MESFET's. Thus, it may be of great interest to analytically model the potential distribution and threshold voltage behavior of the submicrometer Si-MESFET's to get a clear physical understand-ing of the device.

Marshal et. al. [5] have reported a 2-D model for the study of short-channel effects of silicon MESFET's with a uniform doping concentration. However, they have not shown the dependence of threshold voltage on various device parameters of such devices. Recently, a 2-D model has been reported in ref.[6] for the potential distribution and threshold voltage of Si-SOI-MESFET's for both the uniform and Gaussian doping profiles. Since ion implantation has become a widely used process for doping the active channel and source/drain regions of a short-gate length MESFET [7] a suitable 2-D model is also essential for the characterization of short-channel ion implanted MESFET's in the subthreshold region of operations.

The potential distribution of short-channel effects of FET's are modeled analytically by solving the 2-D Poisson's equation. The Green's function technique has been used to solve the Poisson's equation by several authors [8-10] for the modeling of potential distribution and threshold voltage of Si-SOI-MESFET's, and MOSFET's. Although, it is the best method to obtain an accurate solution of the 2-D Poisson's equation, but the involved mathematical complexity makes it difficult to understand the operation and application of the device. Another simple method is the parabolic approximation technique in which the solution of the 2-D Poisson's equation is assumed as a second order polynomial of y with coefficients as arbitrary functions of 'x' which are determined from the boundary conditions [6,11]. Here x and y denotes the longitudinal and transverse directions of the active channel of the device. Since it is an approximation of the actual solution, its accuracy is worse than the Green's function technique. The mostly used method to solve the 2-D Poisson's equation is the superposition technique in which the 2-D Poisson's equation is divided into a 2-D Laplace equation to include the 2-D electric field effects and a 1-D ordinary differential equation used for the modeling of long-channel conventional FET's [5,12,13]. This method may be considered as an optimum technique in terms of its simplicity to understand the device physics and application of the short-channel FET devices.

In this paper, a new 2-D model has been presented for the potential distribution and threshold voltage of fully depleted short-channel ion implanted silicon MESFET's with a Gaussian doping profile. It has been assumed that Gaussian distribution of initial implantation is retained throughout the process and higher moments of implant distribution are neglected in the analysis. The 2-D Poisson's equation has been solved using the superposition principle as in ref. [5,12]. The minimum potential at the edge of the gate-depletion region has been used to show the DIBL effect of the device. The dependence of threshold voltage on channel length, dose and channel width has also been investigated.

II. Theoretical Model

The schematic structure of an ion-implanted fully depleted Si-MESFET under consideration is shown in Fig. 1. The doping profile in the channel may be given by

$$N_d(y) = \frac{Q}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(y-R_p)^2}{2\sigma^2}\right) \tag{1}$$

where Q, σ, R_p are the dose, straggle and range parameters respectively. To obtain the potential distribution function, the 2-D Poisson's equation given by

$$\frac{\partial^2\psi}{\partial x^2} + \frac{\partial^2\psi}{\partial y^2} = -\frac{qN(y)}{\varepsilon_{si}} \tag{2}$$

has to be solved in the marked region of Fig. 1, where $N(y)=N_d(y)$ for $0 < y < a$ (i.e. doping profile in the active channel region), $N(y)=-N_a$ for $a < y < a+w_{dp}$ (i.e. the constant doping profile in the Si substrate region), ψ represents the 2-D electron potential distribution function, a is the thickness of the active layer and ε_{si} is the permittivity of the silicon. Due to the complexity involved in solving eqn.(2), it may be separated into the following equations using the superposition principle as in ref. [13]

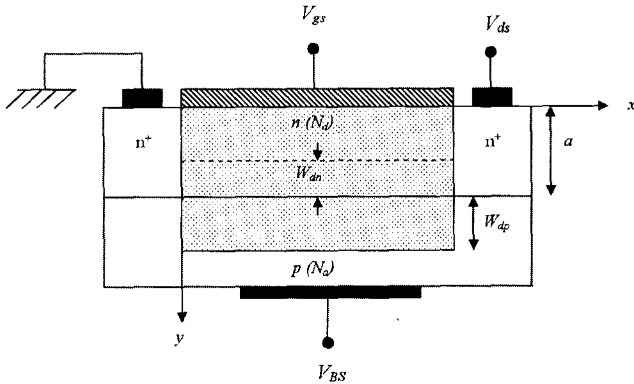


Fig. 1. Schematic structure of a Si-MESFET where marked section denotes the depletion region in which 2-D Poisson's equation is to be solved to obtain the potential distribution function.

$$\frac{\partial^2 U}{\partial y^2} = -\frac{qN(y)}{\varepsilon_{si}} \tag{3}$$

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} = 0 \tag{4}$$

The solution of Eqn.(2) may be written as the summation of the 1-D potential function $U(y)$ obtained by solving Eqn.(3) and 2-D potential function $\phi(x, y)$ obtained by solving Eqn.(4) as considered in ref. [5]. Thus, the solution of Eqn.(2) may be written as

$$\psi(x, y) = \phi(x, y) + U(y) \tag{5}$$

Using the boundary conditions $U(y)\big|_{y=a-w_{dn}} = \phi_c$ and $\left.\frac{dU}{dy}\right|_{y=a-w_{dn}} = 0$ in Eqn.(3) [5], $U(y)$ may be written as

$$U(y) = \begin{cases} \phi_c + \frac{-Qq}{2\varepsilon_{si}}\left[y\, erf\left(\frac{y-R_p}{\sqrt{2}\sigma}\right) + \frac{\sigma}{\sqrt{2\pi}} \exp\left(-\left(\frac{y-R_p}{\sqrt{2}\sigma}\right)^2\right) - y\, erf\left(\frac{a-w_{dn}-R_p}{\sqrt{2}\sigma}\right) \right. \\ \left. -R_p\, erf\left(\frac{y-R_p}{\sqrt{2}\sigma}\right) + R_p\, erf\left(\frac{a-w_{dn}-R_p}{\sqrt{2}\sigma}\right) - \frac{\sqrt{2}\sigma}{\sqrt{\pi}} \exp\left(-\frac{(a-w_{dn}-R_p)^2}{2\sigma^2}\right)\right]; \quad 0<y<a \\ \frac{qN_a}{2\varepsilon_{si}}\left[y-(a+w_{dp})\right]^2 ; \quad a<y<a+w_{dp} \end{cases} \tag{6}$$

where

$$erf(X) = \frac{2}{\sqrt{\pi}} \int_0^X \exp(-z^2)\, dz \tag{7}$$

is the error function, w_{dn} and w_{dp} are the depletion widths in the channel-side and substrate-side due to the channel-substrate interface respectively. ϕ_c in Eqn.(6) is a potential at $y=a-w_{dn}$[5] which may be determined from the continuity condition of $U(y)$ at $y=a$

Let $\Delta\phi_s$, $\Delta\phi_n$, and $\Delta\phi_p$ be the potential difference from surface (*i..e.* $y=0$) to channel (*i..e.* $y=a-w_{dn}$), channel to p-n junction interface (*i..e.* $y=a$), and junction interface to substrate (*i..e.* $y=a-w_{dp}$) respectively. Applying the Kirchoff's voltage law to sum the potentials along the path from the metal Fermi level to the substrate Fermi level, we may write [5]

$$V_{GS} - \Phi_B + \Delta\phi_s + \Delta\phi_n + \Delta\phi_p + (E_g - \xi_p) = V_{BS} \tag{8}$$

where V_{GS} and V_{BS} are the externally applied gate-source and substrate-source voltages, Φ_B is Shottky barrier height, E_g is the bandgap energy of the silicon and ξ_p is the difference between the Fermi energy and the valence band edge in the undepleted substrate, all expressed in units of electrostatic potential. Now $\Delta\phi_s$, $\Delta\phi_n$, and $\Delta\phi_p$, may be given by

$$\Delta\phi_s = \frac{q}{\varepsilon_{si}} \int_0^{a-w_{dn}} \int_0^y N_d(y)\, dy\, dy \tag{9}$$

$$\Delta\phi_n = -\frac{q}{\varepsilon_{si}} \int_{a-w_{dn}}^{a} \int_0^y N_d(y)\, dy\, dy \tag{10}$$

and

$$\Delta\phi_p = -\frac{qN_a}{2\varepsilon_{si}} w_{dp}^2 \tag{11}$$

respectively.

Applying the charge neutrality condition for the depletion region due to the channel-substrate junction, we may write

$$\int_{a-w_{dn}}^{a} N(y)dy = N_a w_{dp} \tag{12}$$

From the energy band diagram, the potential at may be given by

$$\phi_c = -(\Delta\phi_n + \Delta\phi_p) \tag{13}$$

Thus using Eqns. (9)-(11) in Eqn. (8), the resultant equation and Eqn.(12) may be solved to obtain w_{dn} and w_{dp}. Once the values of w_{dn} and w_{dp} are known, ϕ_c may be determined by using Eqns.(10) and (11) in Eqn.(13).

Now the Eqn.(4) may be solved to obtain the expression for with the following boundary conditions [5]:

$$\psi(x,0)=U(0) \Rightarrow \phi(x,0)=0 \quad (14)$$

$$\psi(x,a+w_{dp})=U(a+w_{dp})=0 \Rightarrow \phi(x,a+w_{dp})=0 \quad (15)$$

$$\psi(0,y)=P_S(y) \Rightarrow \phi(0,y)=P_S(y)-U(y) \quad (16)$$

$$\psi(L,y)=P_D(y) \Rightarrow \phi(L,y)=P_D(y)-U(y) \quad (17)$$

where $P_S(y)$ and $P_D(y)$ are the side wall potentials at $x=0$ and $x=L$ respectively, which may be given as [5].

$$P_S(y)=\begin{cases}\phi_{pn+}-V_{BS}; & 0\le y\le a\\ \dfrac{qN_a}{2\varepsilon_{si}}[y-(a+w_s)]^2; & a<y\le a+w_{dp}\end{cases} \quad (18)$$

$$P_D(y)=\begin{cases}\phi_{pn+}+V_{DS}-V_{BS}; & 0\le y\le a\\ \dfrac{qN_a}{2\varepsilon_{si}}[y-(a+w_d)]^2; & a<y\le a+w_{dp}\end{cases} \quad (19)$$

where ϕ_{pn+} is the built-in potential of the substrate-n^+ junctions at the source and drain sides which may be given by

$$\phi_{pn+}=E_g-\xi_p=E_g-\frac{kT}{q}\ln\left(\frac{N_V}{N_a}\right) \quad (20)$$

where N_V is the valence band effective density of states and V_{BS} is substrate bias voltage. W_s and W_d are the depletion widths below the n^+ source and drain regions respectively, which may be given as

$$w_s=\sqrt{\frac{2\varepsilon_{si}(\phi_{pn+}-V_{BS})}{qN_a}} \quad (21)$$

$$w_d=\sqrt{\frac{2\varepsilon_{si}(\phi_{pn+}+V_{DS}-V_{BS})}{qN_a}} \quad (22)$$

Applying the separation of variables technique [5, 12, 13] and using the boundary conditions described by Eqns. (14) and (15), the expression for $\phi(x,y)$ may be described as

$$\phi(x,y)=\sum_{n=1}^{\infty}\sin\left(\frac{n\pi y}{a+w_{dp}}\right)\left[A_n\cosh\left(\frac{n\pi x}{a+w_{dp}}\right)+D_n\sinh\left(\frac{n\pi x}{a+w_{dp}}\right)\right] \quad (23)$$

Using the boundary condition described by Eqn.(16) in Eqn.(23), we may write

$$f_1(y)=P_S(y)-U(y)=\sum_{n=1}^{\infty}A_n\sin\left(\frac{n\pi y}{a+w_{dp}}\right) \quad (24)$$

From Eqn.(24), we may observe that $f_1(y)$ has been expressed as a half-sine series. Thus from the property of the Fourier series, we may write

$$A_n=\frac{2}{(a+w_{dp})}\int_0^{a+w_{dp}}f_1(y)\sin\left(\frac{n\pi y}{a+w_{dp}}\right)dy \quad (25)$$

Similarly, using the boundary condition described by Eqn.(17) in Eqn.(23), we get

$$B_n=\left[A_n\cosh\left(\frac{n\pi L}{a+w_{dp}}\right)+D_n\sinh\left(\frac{n\pi L}{a+w_{dp}}\right)\right]$$

$$=\frac{2}{(a+w_{dp})}\int_0^{a+w_{dp}}\{P_D(y)-U(y)\}\sin\left(\frac{n\pi y}{a+w_{dp}}\right)dy \quad (26)$$

From Eqns.(25) and (26), we may get

$$D_n=\frac{B_n-A_n\cosh\left(\dfrac{n\pi L}{a+w_{dp}}\right)}{\sinh\left(\dfrac{n\pi L}{a+w_{dp}}\right)} \quad (27)$$

Thus, the resultant expression for 2-D potential function of ion implanted MESFET's may be put in the similar form as described in ref.[5] for the uniform doping profile and may be written as

$$\psi(x,y)=U(y)+\sum_{n=1}^{\infty}\frac{\sin\left(\dfrac{n\pi y}{a+w_{dp}}\right)}{\sinh\left(\dfrac{n\pi L}{a+w_{dp}}\right)}\left[A_n\sinh\left(\frac{n\pi(L-x)}{a+w_{dp}}\right)+B_n\sinh\left(\frac{n\pi x}{a+w_{dp}}\right)\right] \quad (28)$$

where A_n, B_n are the Fourier coefficients described by Eqns.(25) and (26) respectively. Note that we can't get the closed form expressions for A_n and B_n of Eqn.(28). However, we have solved the Eqns.(25) and (26) numerically using MATLAB to obtain the values of a and B_n for different device parameters.

The subthreshold characteristics are often expressed in terms of the minimum bottom channel potential $\Psi_{min}=\Psi(x_{min}, a-w_{dn})$where x_{min} is the distance from the source at which the bottom potential $\Psi_{bp}(x)=\Psi(x, a-w_{dn})$ has the minimum value. Thus, the expression for the may be obtained by solving the x_{min} following equation:

$$\left.\frac{\partial\Psi(x, a-w_{dn})}{\partial x}\right|_{x=x_{min}}=0 \quad (29)$$

From Eqns.(28) and (29), we may observe that the closed form expression of x_{min} is not possible to achieve for all the possible values of n. However, from our numerical calculations, it has been observed that A_n and B_n in Eqn.(28) for $n\geq 2$ are very small as compared to A_1 and B_1. Further, for a moderately short-channel device, we may use the following approximations in Eqn.(28) to obtain a simplified expression for $\Psi(x, a-w_{db})$:

$$\sinh\left(\frac{\pi (L-x)}{a+w_{dp}}\right)\approx \exp\left(\frac{\pi (L-x)}{a+w_{dp}}\right) \quad (30)$$

$$\sinh\left(\frac{\pi x}{a+w_{dp}}\right)\approx \exp\left(\frac{\pi x}{a+w_{dp}}\right) \quad (31)$$

$$\sinh\left(\frac{\pi L}{a+w_{dp}}\right)\approx \exp\left(\frac{\pi L}{a+w_{dp}}\right) \quad (32)$$

Thus, neglecting the Fourier coefficients A_n and B_n for $n\geq 2$, and using the approximations described through Eqns.(30)-(32), we may write

$$\psi(x,a-w_{dn})=\phi_c+\sin\left(\frac{\pi (a-w_{dn})}{a+w_{dp}}\right)\left[A_1\exp\left(\frac{-\pi x}{a+w_{dp}}\right)+B_1\exp\left(-\frac{\pi(L-x)}{a+w_{dp}}\right)\right] \quad (33)$$

Using Eqn.(29) and (33), x_{min} may be approximately given by

$$x_{min}\approx\frac{L}{2}-\frac{a+w_{dp}}{2\pi}\ln\left(\frac{B_1}{A_1}\right) \quad (34)$$

Since A_1 and B_1 differ only because of the applied V_{DS}, thus for $V_{DS}=0$, $A_1=B_1$ which results in $x_{min}=\frac{L}{2}$. From Eqns.(25) and (26), it may be observed that as V_{DS} is increased, B_1 is also increased while A_1 remains unchanged. Hence, the second term in the right side of Eqn.(34) is increased with the increase in V_{DS}, and thus x_{min} is decreased. In other words, we may say that the position of the minimum channel potential at $y=a-w_{dn}$, moves toward the source with the increase in the drain bias voltage. This is called the drain induced barrier lowering (DIBL) effect in the short-channel FET devices.

The threshold voltage V_{th} may be defined as the gate voltage below which the channel remains under fully depleted condition. In other words, there is no channel opening and thus the channel does not start to conduct if $V_{gs}\leq V_{th}$. The threshold voltage may V_{th} be obtained by solving the following equation [8]:

$$\psi(x_{min}, a-w_{dn})\big|_{V_{gs}=V_{th}}-\phi_{pn+}=\phi_b^c \quad (35)$$

where ϕ_b^c is the minimum channel barrier to define the threshold voltage [9]. Note that using Eqns.(20), (33) and (34) in Eqn.(35), it is not possible to obtain a closed form expression for the threshold voltage. However, we have solved the Eqn.(34) numerically to calculate the threshold voltage for different device parameters.

III. Results And Discussions

In this section we have presented some numerical results to demonstrate the effects of various parameters on the bottom channel potential to demonstrate the DIBL and threshold voltage of short-channel Si-MESFET's. The variation of bottom potential $\Psi_{bp}(x)=\Psi(x, a-w_{dn})$ as a function of the normalized position (x/L) along the channel has been shown in Fig. 2 for different drain voltages. From the figure it is observed that for a fixed gate length, as the drain -source voltage V_{DS} is increased, the value of the

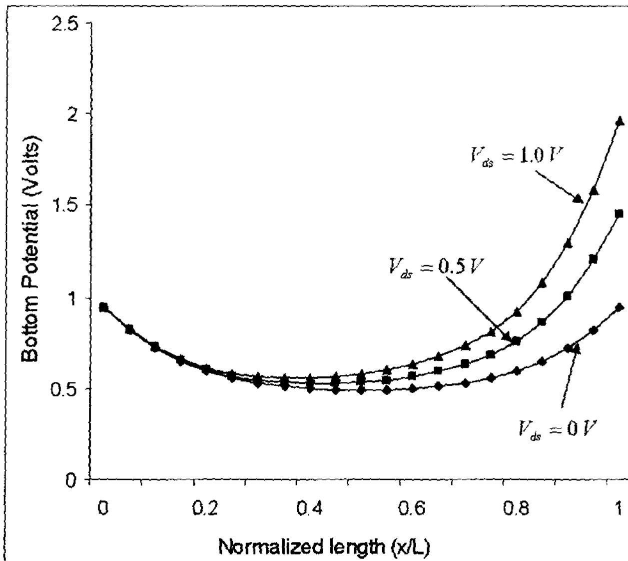


Fig. 2. Plot of bottom potential $\Psi_{bp}(x)=\Psi(x, a\text{-}w_{dn})$in the channel as a function of normalized channel length (x/L) for L=0.5μm at V_{GS}=-0.3*Volts* for V_D=0V, 0.5V and 1.0 V, a=0.1μm, Dose (Q) =1X10[13]/cm^2, R_p=0.0, σ=0.1μm, N_a=5X10[15]cm^{-3}, N_v=1.04X10[19]/cm^3, Φ_B=0.7V and V_{BS}=0V.

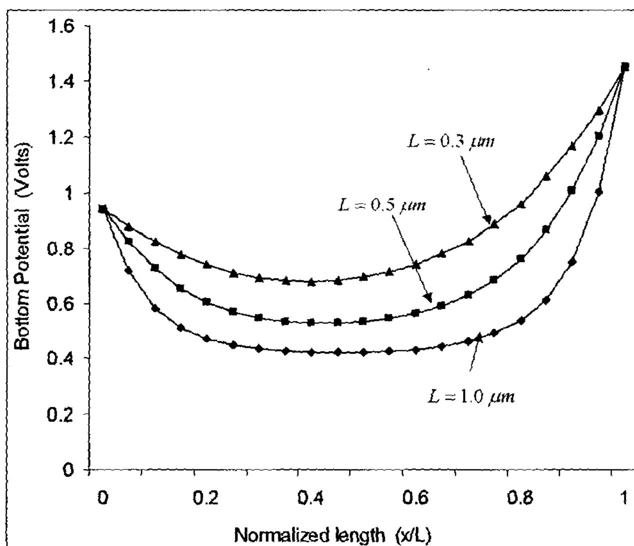


Fig. 3. Plot of bottom potential as a function of normalized channel length for gate lengths 1.0, 0.5, 0.3μm, with V_{GS}=-0.3V, V_{DS}=0.5V, a=0.1μm, Dose (Q) =1X10[13]/cm^2, R_p=0.0, σ=0.1μm, N_a=5X10[15]cm^{-3}, N_v=1.04X10[19]/cm^3, Φ_B=0.7V and V_{BS}=0V.

minimum bottom potential is also increased which results in the considerable reduction in the channel barrier. Thus the potential difference between the channel and the source is reduced due to the increase in the drain-source voltages in the subthreshold region of operation of the MESFET's. This phenomenon is commonly known as DIBL in short-channel FET devices. It may also be observed that the

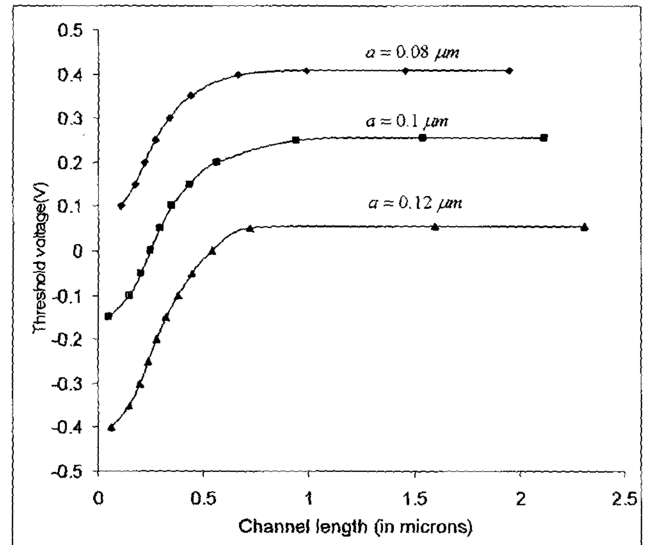


Fig. 4. Plot of threshold voltage versus channel length (L) for different channel thickness. Parameter used for calculation: Dose (Q) =1X10[13]/cm^2, R_p=0.0, σ=0.1μm, N_a=5X10[15]cm^{-3}, ϕ_S^c=-0.1V, N_v=1.04X10[19]/cm^3, Φ_B=0.7V and V_{BS}=0V.

position of the minimum bottom potential is shifted towards the source as the drain bias is increased. The variation of the bottom potential as a function of the normalized distance is shown in Fig. 3 for different gate-lengths and a fixed value of the V_{DS}. It is observed that the minimum bottom potential is increased with the decrease in gate-length. The position of the minimum bottom potential is also shifted in this case towards the source with the decrease in L. From Fig. 2 and 3, we may observe that DIBL effect is more dominant for L=0.3μm than that for L=0.3μm and 1.0μm which indicates that DIBL is the most pervasive effect in the submicrometer regime of operation of the MESFET's.

The effect of active layer thickness 'a' on the threshold voltage has been presented in Fig. 4. It is observed that for a fixed value of 'a', the threshold voltage is degraded as the gate-length is decreased and becomes constant for larger gate-length. For a fixed gate-length, the threshold voltage is increased as the channel thickness is reduced. This implies that the short-channel effects due to the reduction of the gate-length may be minimized by reducing the channel thickness. This suggests that the degradation of threshold voltage due to the short gate-length may be minimized by reducing the active channel thickness. The threshold voltage against the channel length L has been plotted in Fig. 5 for different values of the drain-source bias V_{DS}. It is

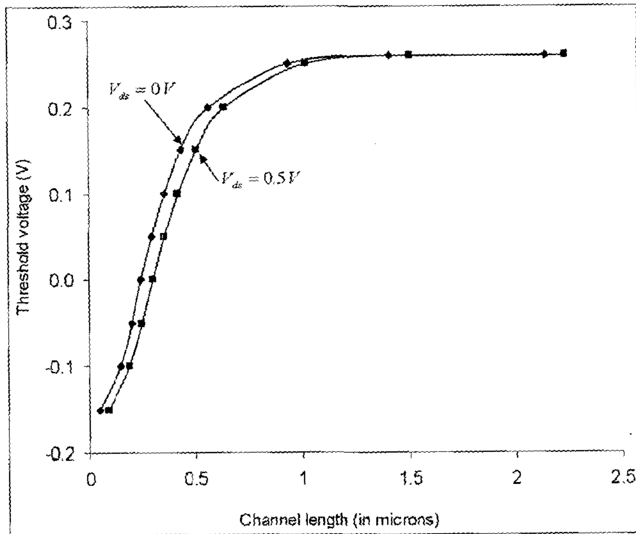


Fig. 5. Variation of threshold voltage with channel length (L) for different drain-source voltages. Parameters used for calculation: a=,0.1μm, Dose (Q)=1×10^{13}/cm^2, R_p=0.0, σ=0.1μm, N_a=5×10^{15}cm^{-3}, ϕ_b=-0.1V, N_v=1.04×10^{19}/cm^3, Φ_B=0.7V and V_{BS}=0V.

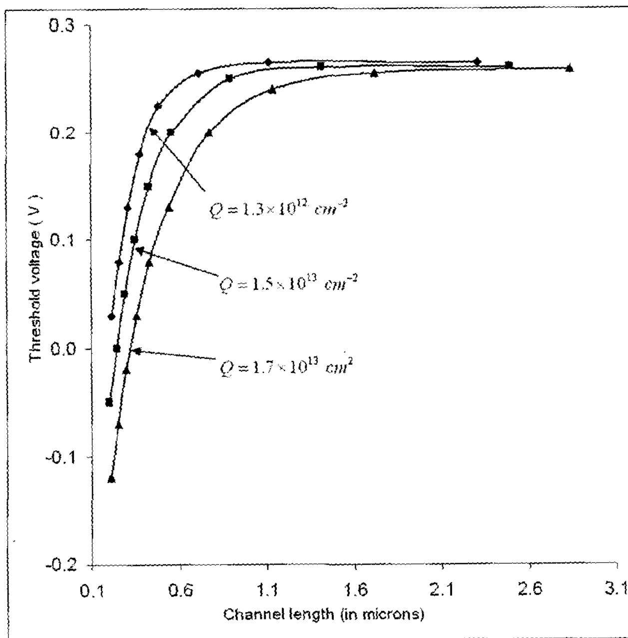


Fig. 6. Plot of threshold voltage versus channel length (L) for different doses (Q). Parameters used for calculation: a=,0.1μm, R_p=0.0, σ=0.1μm, N_a=5×10^{15}cm^{-3}, ϕ_b^c=-0.1V, N_v=1.04×10^{19}/cm^3, Φ_B=0.7V, V_{DS}=0.0V and V_{BS}=0V.

observed that as the gate-length is below some certain value, the threshold voltage is degraded due to the increase in the drain-source voltage in the subthreshold region of operation of the MESFET. The dependence of the threshold voltage on the implanted dose (Q) has been shown as a function of the gate-length in Fig. 6. It is observed that as the gate-length is decreased below a certain value, the threshold voltage is degraded due to the increase in the value of the implanted dose with all other device parameters remaining unchanged. However, it almost remains unaffected for higher gate-length devices.

It may be observed by comparing the figures from Fig. 4 to Fig. 6 that as the gate-length reduces below some certain value, the threshold voltage changes from a positive to a negative value. This shows that the normally-off device behaves as a normally-on device if the gate-length is lower than some specified value which is not desirable at all.

It may be mentioned that the major disadvantage of a Si-MESFET over a Si-MOSFET is that gate leakage current increases much rapidly due to the decrease in the channel length in the former device than that in the latter device. However, the basic purpose of the present study is to present a 2-D model for the ion-implanted Si-MESFET but not to present any comparative study of MESFET and MOSFET devices in the subthreshold region of operations.

It may be mentioned that the results presented in this paper are mostly for channel length greater than 0.1μm which is slightly larger than that used in current CMOS based VLSI/ULSI technology. This is due to the fact that the rate of increase in the gate leakage current with the decrease in channel length is much higher in MESFET's than the MOSFET devices. This may be treated as the major limitation for the MESFET based VLSI/ULSI technology. However, the purpose of the present paper is only to report an analytical model for the ion-implanted short-channel Si-MESFET's to get the physical insight regarding the potential distribution and threshold voltage behavior of the device in the submicrometer region of operation. Further study may be carried out to make a detailed quantitative comparison between the performances of MESFET's and MOSFET's in their deep submicrometer regions of operations.

IV. CONCLUSIONS

A 2-D model for the potential distribution and threshold voltage of fully depleted short-channel ion-implanted Si-MESFET's has been presented in this paper.

The channel potential function has been derived by solving the 2-D Poisson's equation in the depletion region of the MESFET. The DIBL effect has been demonstrated by presenting numerical results. It has been observed that as the channel length is reduced, the channel potential shifts towards the source. Similar effects have also been observed by increasing the values of drain-source voltages. The effect of different device parameters on the threshold voltage is also presented for short-channel Si-MESFET's. It has been observed that the normally-off device behaves as a normally-on device if the gate-length is less than some specified value.

REFERENCES

[1] K. P. MacWilliams, and J. D. Plummer, "Device physics and technology of complementary silicon MESFET's for VLSI applications," *IEEE Trans. Electron Devices*, vol. 38, no. 12, pp. 2619-2631, Dec. 1991.

[2] J. Mendl, "Theoretical, practical, and analogical limits in ULSI, "*IEDM Tech. Dig.*, p.8, 1983.

[3] J. Nulman and J.P. Krusius, "2-GHz 150 μW self-aligned Si-MESFET logic," *IEEE Electron Device Lett.*, vol. EDL-5, p. 169, 1984.

[4] J. D. Marshal and J. D. Mendl, "A sub- and near threshold current model for silicon MESFET's," *IEEE Trans. Electron Devices*, vol. 35, p. 388, March 1988.

[5] J. D. Marshall and J. D. Meindl, "An analytical two-dimensional model for silicon MESFET's," *IEEE Trans. Electron Devices*, vol. 35, p. 373, March 1988.

[6] P. Pandey, B. B. Pal and S. Jit, "A new 2-D model for the potential distribution and threshold voltage of fully depleted short-channel Si-SOI-MESFETs," *IEEE Trans. Electron Devices*, vol. 51, p. 246, Feb. 2004.

[7] R. Anholt and T. W. Sigmon, "Ion implantation effects on GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. 36, p. 250, 1989.

[8] C. S. Hou and C. Y. Wu, "A 2-D analytic for the threshold-voltage of fully depleted short gate-length Si-SOI-MESFET's," *IEEE Trans. Electron Devices*, vol. 42, p. 2156, Dec 1995.

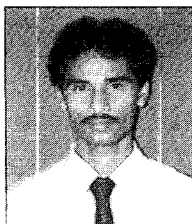
[9] S.-P. Chin, and C.-Y. Wu, "A new two-dimensional model for the potential distribution of short-gate-length MESFET's and its applications," *IEEE Trans. Electron Devices*, vol. 39, p. 1928, Aug. 1992.

[10] P. S. Lin and C- Y. Wu, "A new approach to analytically solving the two-dimensional Poisson's equation and its application in short-channel MOSFET modeling," *IEEE Trans. Electron Devices*, vol. ED-34, p. 1947, 1987.

[11] K. K. Young, "Short-channel effects in fully depleted SOI-MOSFET's," *IEEE Trans. Electron Devices*, vol. 36, p. 399, Feb. 1989.

[12] T. K. Chiang, Y. H. Wang, and M. P. Houng, "Modeling of threshold voltage and subthreshold swing of short-channel SOI-MESFET's," *Solid-State Electron*, vol.-43, p.123, 1999.

[13] K. N. Ratnakumar and J. D. Meindl, "Short channel MOST threshold voltage model," *IEEE J. Solid State Circuits*, vol.SC-17, p. 937, Oct.1982.



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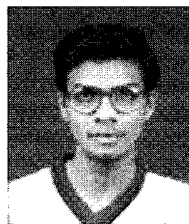

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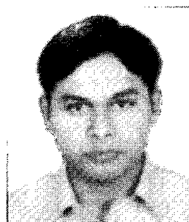

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