# Physics-based Algorithm Implementation for Characterization of Gate-dielectric Engineered MOSFETs including Quantization Effects

Tina Mangla*, Amit Sehgal**, Manoj Saxena***, Subhasis Haldar****, Mridula Gupta*, and R. S. Gupta*

*Abstract*—**Quantization effects (QEs), which manifests when the device dimensions are comparable to the de Brogile wavelength, are becoming common physical phenomena in the present micro-/nanometer technology era. While most novel devices take advantage of QEs to achieve fast switching speed, miniature size and extremely small power consumption, the mainstream CMOS devices (with the exception of EEPROMs) are generally suffering in performance from these effects. In this paper, an analytical model accounting for the QEs and poly-depletion effects (PDEs) at the silicon (*Si*)/dielectric interface describing the capacitance-voltage (C-V) and current-voltage (I-V) characteristics of MOS devices with thin oxides is developed. It is also applicable to multi-layer gate-stack structures, since a general procedure is used for calculating the quantum inversion charge density. Using this inversion charge density, device characteristics are obtained. Also solutions for C-V can be quickly obtained without computational burden of solving over a physical grid. We conclude with comparison of the results obtained with our model and those obtained by self-consistent solution of the Schrödinger and Poisson equations and simulations reported previously in the literature. A good agreement was observed between them.**

*Index Terms*—**Quantization effects, poly-depletion effects, gate stack architecture, gate capacitance, transconductance**

Manuscript received March 20, 2005; revised September 9, 2005.
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## I. INTRODUCTION

To fulfill the scaling scenario as projected in the International Technology Roadmap for Semiconductors (ITRS), it is widely believed that a high-*k* (high permittivity) dielectric is needed to replace silicon-dioxide ($SiO_2$) as the CMOS gate dielectric, to reduce significantly the gate leakage current [1]. High-*k* gate dielectrics are seen as a potential solution for the low-leakage technologies, as these materials allow for physically thicker films still having a small electrical thickness and thus maintaining same gate capacitance. After extensive research efforts by numerous groups, several high-*k* dielectrics have shown promising results [2]. However, there are still many challenges that occur due to downscaling of device dimensions. One of the well known fact is that the electrons in metal-oxide-semiconductor field-effect-transistor (MOSFET) inversion layer is actually two-dimensional electron gas (2-DEG) with sub-bands each of which corresponds to a quantized energy level for motion perpendicular to the $Si/SiO_2$ interface [3, 4], which is quite different from that in the semi-classical case. The quantization effects (QEs) on the characteristics of MOSFET become more significant with the scaling down of modern MOSFETs [5-9]. It has been observed that among other effects, the quantization of the carrier energy results in an increase in threshold voltage [5], decrease in gate capacitance [6, 7] and decrease in transconductance [8, 9]. These effects are associated with the increased average distance of the carriers from the $Si/SiO_2$ interface due to the quantization of carrier states. In order to estimate various QEs, it is necessary to solve Schrödinger and Poisson equations self-consistently [3, 4], which is

very time consuming. So, it is important to develop simple and convenient model to predict QEs on MOSFET characteristics. Several works have proposed either physically rigorous or simplified treatments [10, 11] of the QEs of an inverted MOS structure. The former is known to give an accurate and physically rigorous, accounts of the system behaviour, where as the latter propose an approximate treatment. Generally the accuracy is traded-off for speed. Nevertheless, there are relatively few works addressing the QEs through high-*k* dielectric structures [12] via fully self-consistent approach. Although a self-consistent approach, essentially based on the numerical solution of coupled Schrödinger and Poisson equations would be conceptually similar to that of a MOS structure with a single dielectric layer, simplified models particularly exploiting the stacked structure of the multilayer dielectrics have not been widely addressed. The triangular potential well (TPW) approximation holds good to decouple Schrödinger and Poisson equations and could well predict the carrier density reduction due to QEs in strong inversion of gate-stacked structures [13]. The extracted surface-potential is used to evaluate capacitance-voltage (C-V) characteristics of the device for both classical and quantum mechanical approach. A newly developed iteration method with high efficiency and robust stability is adopted in this model. Surface potential as well as carrier sheet density of high precision can be achieved simultaneously within two or more iteration loops. The model is then applied to analyze QEs on device characteristics. The paper thus presents a complete analytical model accounting for both QE and poly-depletion effect (PDE) in MOS inversion layer for both single dielectric and stacked dielectric structures. Comparison with more sophisticated numerical [9, 12] and simulated results [7] demonstrates the accuracy of the model and is found to be less time consuming.

## II. Model Formulation and Algorithm Computation

MOS inversion layer carrier density and then the gate capacitance are key parameters for MOSFET characterization and modeling. To avoid the computational complexity of the fully self consistent solution of Schrödinger and Poisson equations, in an inverted MOS structure, an alternative is to use an approximate treatment that takes into account the quantization effect occurring at the $Si/SiO_2$ interface. In spite of simplifying assumptions and "first-order" precision of the results, this approach proved to be a valuable tool for quick assessment of the QEs in MOS structures. In this section we briefly explain the general algorithm implemented in our model to obtain the $C_G$ - $V_G$ and $I_D$ - $V_G$ characteristics of the transistor. Fig. 1 shows the four different dielectric configurations analyzed for MOSFET and Fig. 2 shows a flowchart where we represented the three iterations procedures ; labeled A, B and C respectively used to : (A) extract the surface potential, (B) calculate the drain current and transconductance and (C) evaluate the gate capacitance with respect to source. The symbols/notations used in the computational flowchart are described as: $\phi_S$ is the surface potential, $\varepsilon_{Si}$ is the silicon permittivity, $q$ is the electronic charge, $\eta$ is the reduced Planck constant, $k_B$ is the Boltzmann's constant, $T$ is the temperature, $N_A$ is the substrate doping, $m_i$ is the effective mass perpendicular to the surface, $n_{vi}$ is the degeneracy of the energy subbands, $m_{di}$ is the density-of-states mass per valley, $E_{ij}$ is the energy state of $i^{th}$ valley and $j^{th}$ subband, $E_F$ is the Fermi energy and $V_{fb}$ is the flat-band voltage. The poly-depletion effect is included in the computation by incorporating the additional potential drop $\phi_P$ [14] in the gate-bias acting on

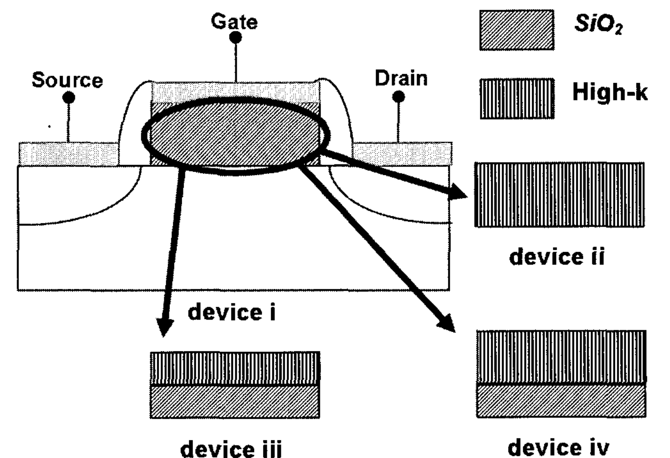


**Fig. 1.** Schematic diagram for silicon MOSFET structures. *device i*: conventional $SiO_2$. *device ii*: high-k gate dielectric (k=10) with physical thickness of device i. *device iii*: Gate-stack structure with upper dielectric (k=10) and lower dielectric $SiO_2$ (k=3.9) physical thickness equal to device i. *device iv*: Gate-stack structure same as device iii but with an electrical thickness equal to device i.

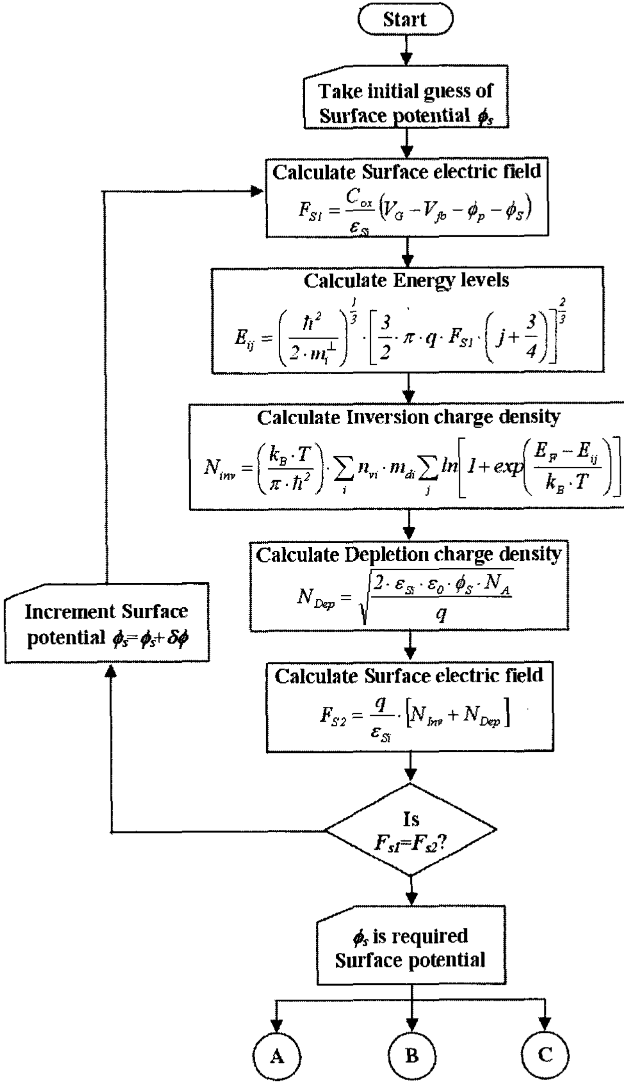


Fig. 2a. Flowchart/algorithm for the extraction of surface potential, $\phi_s$ with quantization effects.

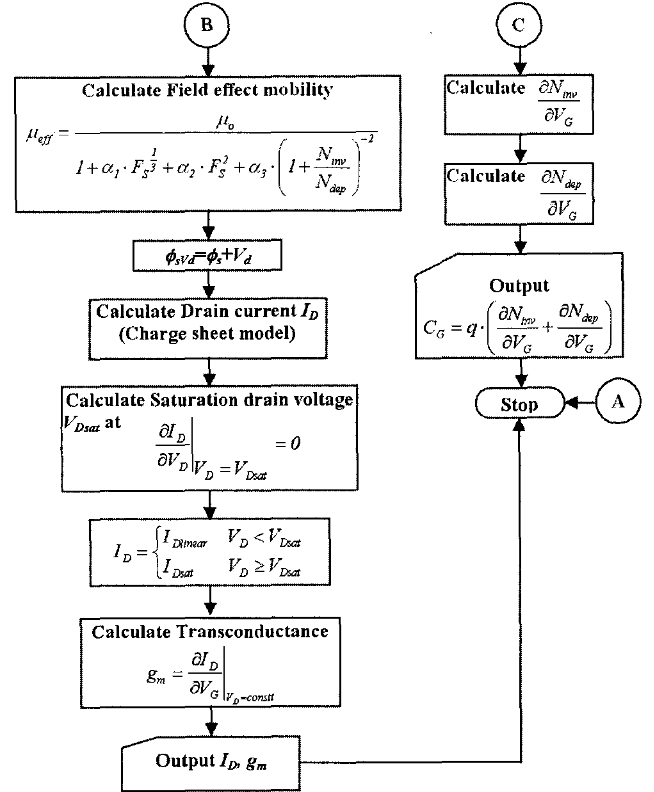


Fig. 2b. Flowchart/algorithm for the extraction of transfer characteristics and gate capacitance using surface potential, $\phi_s$.

silicon, calculated by solving Poisson equation in poly-*Si*, and is given by:

$$\phi_P = \begin{cases} 0 & for \quad V_G \le V_{fb} \\ \left(\sqrt{V_G - V_{fb} - \phi_S + \dfrac{\gamma_P^2}{4}} - \dfrac{\gamma_P}{2}\right)^2 & for \quad V_G > V_{fb} \end{cases} \tag{1}$$

where $\gamma_P$ is the body effect coefficient of the poly-silicon gate and equals to $\gamma_p = \sqrt{2 \cdot q \cdot \varepsilon_{Si} \cdot N_P}/C_{ox}$ with $N_P$ the poly-silicon doping and $C_{ox}$ the oxide capacitance per unit area. The drain current is calculated using charge sheet model [15]. In the context of a charge sheet model, it has an advantage that a single continuous equation yields the drain current for the device operation range, and the computation of charges is straightforward. Note that the mobility model used in our analysis is described as:

$$\mu_{eff} = \frac{\mu_o}{1 + \alpha_1 \cdot F_S^{\frac{1}{3}} + \alpha_2 \cdot F_S^2 + \alpha_3 \cdot \left(1 + \dfrac{N_{inv}}{N_{dep}}\right)^{-2}} \tag{2}$$

where $\mu_o$ is the low-field mobility [16], and $\alpha_1$, $\alpha_2$, $\alpha_3$ are the technology dependent fitting parameters, where $\alpha_1$ = 1.1-1.5 (x$10^{-3}$) $(m/V)^{1/3}$, $\alpha_2$ = 4.2-5.8 (x$10^{-17}$) $(m/V)^2$ and $\alpha_3$ = 1.2-8.2 .

The gate capacitance $C_G$ evaluated with respect to source, which determines the MOSFET's cut-off frequency as well as the magnitude of the inversion charge density in the channel, is defined as:

$$C_G = \frac{dQ_G}{dV_G} = \frac{q \cdot d(N_{inv} + N_{dep})}{dV_G} \tag{3}$$

where $dQ_G$ is the change of the gate charge due to a $dV_G$ gate voltage change, $N_{inv}$ is the inversion charge density

and $N_{dep}$ is the depletion charge density. The corresponding gate voltage derivatives of inversion charge and depletion charge are calculated as:

$$\frac{dN_{inv}}{dV_G} = \left(\frac{k_B \cdot T}{\pi \cdot \hbar^2}\right) \cdot \sum_i n_{vi} \cdot m_{di} \cdot \sum_j \left\{ \frac{-\exp\left(\frac{E_F - E_{ij}}{k_B \cdot T}\right)}{1 + \exp\left(\frac{E_F - E_{ij}}{k_B \cdot T}\right)} \cdot \frac{1}{k_B \cdot T} \times \right.$$

$$\left. \left[ \left(\frac{\hbar^2}{2 \cdot m_i^{\perp}}\right)^{\frac{1}{3}} \cdot \left[\frac{3}{2} \cdot \pi \cdot q \cdot \left(j + \frac{3}{4}\right)\right]^{\frac{2}{3}} \cdot \frac{2}{3} \cdot F_S^{\frac{-1}{3}} \cdot \frac{C_{ox}}{\varepsilon_{Si}} \left(1 - \frac{d\phi_P}{dV_G} - \frac{d\phi_S}{dV_G}\right) - q \cdot \frac{d\phi_S}{dV_G} \right] \right\} \tag{3A}$$

$$\frac{dN_{dep}}{dV_G} = \sqrt{\frac{\varepsilon_{Si} \cdot \varepsilon_0 \cdot N_A}{2 \cdot \phi_S}} \cdot \frac{d\phi_S}{dV_G} \tag{3B}$$

The sub-100 nm MOSFETs face a scaling limit, when a $SiO_2$ gate dielectric is used, and requires gate dielectric engineering to be done. An alternative gate-dielectric material with higher permittivity and greater physical thickness prevents tunneling of carriers. But, use of high-*k* gate material may result in dielectric thickness comparable to the device gate length, resulting in increased fringing fields [17] from the gate to the source/drain regions and compromised short-channel performance. Thus, the need of gate-stack architecture arises, which allows one to use physically thicker films thereby reducing the tunneling current while maintaining the same gate capacitance needed for scaled device operation. In order to model gate-stack structure, $C_{ox}$ is replaced by the effective dielectric capacitance $C_{eff}$ in the equation of surface electric field and is given by:

$$C_{eff} = \frac{k_1 \cdot k_2}{k_1 \cdot t_{ox2} + k_2 \cdot t_{ox1}} \tag{4}$$

where $k_1(t_{ox1})$ and $k_2(t_{ox2})$ is the dielectric permittivity (dielectric thickness) of upper and lower dielectric respectively.

Finally, it is also important to address that closed boundary conditions are used in our model, which assumes that the wave-function is zero at the $Si/SiO_2$ interface, and the wave-penetration effects into the gate-dielectric are neglected. Consequently, for a given electrical thickness, the calculated gate capacitance becomes independent of the gate-dielectric material [12]. Also the problems arising due to defects both at the interface and within the dielectric layer are not considered in the analysis. These issues will require more detailed analysis to identify the material properties of the dielectric together with the understanding of atomic nature of defects, to study their role in device reliability prediction. The modeling of the above mentioned effects is however beyond the scope of this paper. For the latter, the reader is referred to [2, 18] and references therein.

## III. Results and Discussions

The results of our surface potential based analytical model for n-MOS devices are presented in this section. Calculations are performed at room temperature and values of various parameters for <100> silicon are the same as those used by Stern [3] .The calculated surface potentials of the present model are in good agreement with available self-consistent results [9] as shown in Fig. 3. As the potential barrier at the interface is assumed to be infinitely large, the wavefunction vanishes at the interface and thus the probability of finding an electron there is

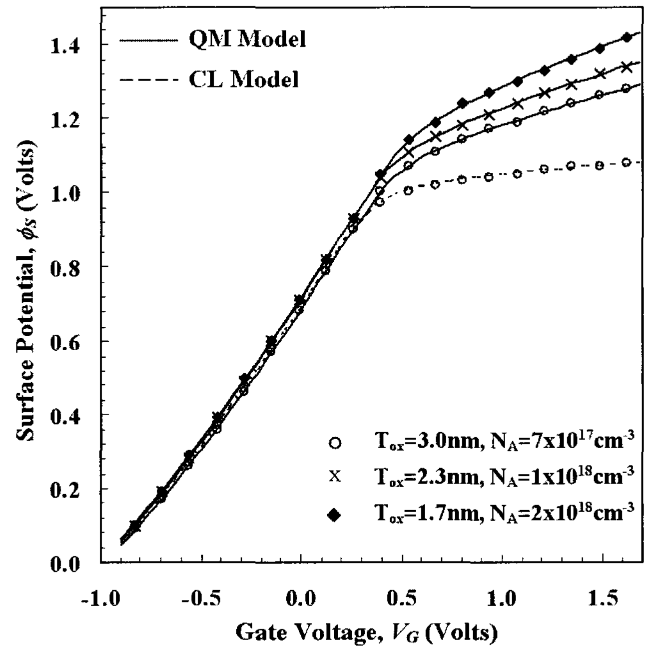


**Fig. 3.** Variation of surface potential with gate voltage for different dielectric thicknesses and substrate doping concentrations for device i. Symbols represent the F. Pregaldiny et. al [9] results.

nearly zero. Hence, the electron concentration peaks below the interface, which is in contrast to the classical model in which the electron concentration peaks at the surface. As a result, it takes a higher gate voltage drive or in other words gives rise to a higher value of surface potential to produce a given level of inversion charge density and it can be interpreted from the curves that a raise in surface potential occurs on comparison of classical and quantum approach. Also, surface potentials for quantum approach for different set of parameters are drawn to study the impact of reduction in dielectric thickness and increase in substrate doping which are necessary for better gate controllability. The difference in the scheme of curves drawn is noticeable and shows the necessity of incorporation of quantization effect analysis while scaling down MOS devices.

Another important issue with respect to MOS transistor is the gate capacitance. Since the device scaling rules demand thinner gate valleys, with the effective mass acting in the direction perpendicular to the $Si/SiO_2$ interface, degradation of the total gate capacitance is expected to have an important consequence on device performance. Fig. 4 shows the comparison of n-MOS gate-capacitance for device i with gate-source voltage ($C_G$-$V_G$ characteristics) between the modeled and available simulated results [7]. The gate capacitance of the device reduces with respect to the $C_{ox}$ as $T_{ox}$ ($t_{ox1}$ + $t_{ox2}$) is increased, due to the larger effective oxide thickness consequent to the displacement of the inversion charge from the device interface. Figure 4 shows the computed gate capacitance according to classical (CL) approach, quantum model with substrate quantization (without PDE) and full quantum model including both substrate and poly-silicon depletion. The effect of poly-silicon depletion on the gate capacitance can be noted effectively in strong inversion, as CL distribution in the poly-silicon is eventually recovered and widens the depletion layer thus enhances the effective oxide thickness, and the gate capacitance further degrades for full quantum approach. These observations imply that, even though the space quantization effect considerably reduces the magnitude of $C_G$, the dominant degradation mechanism for the total gate capacitance is the depletion of the poly-silicon gates.

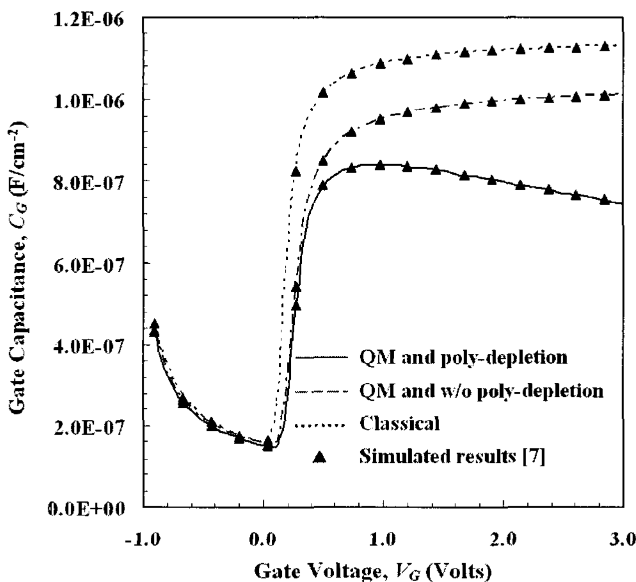


**Fig. 4.** Gate-capacitance per unit area with gate voltage for device i. $T_{ox}$=3nm, $N_A$=3x10$^{17}$cm-3 and $N_P$=5x10$^{19}$cm$^{-3}$.

Table I proves the validity of our approach adopted for analyzing stacked structures (Fig.1). It shows the values of gate-capacitance obtained at different gate source voltages for QM approach together with available self-consistent results [12]. Metal gate (*Al*) is assumed in order to focus on the impact of QEs. The Table illustrates that for same electrical thickness of single dielectric configuration or stacked dielectric configuration, gate-capacitance remains same and further no change in device characteristics is seen on comparison of device i and device iv, except for the fact that an increase in physical thickness is achieved thus preventing gate tunneling.

**Table. 1.** $C_G$, Gate capacitance per unit area (μF/cm$^2$) using QM approach for different dielectric configurations and same electrical thickness of 1nm

| $V_G$ (V) | Single dielectric | | | | | | Gate-stack structure | |
|---|---|---|---|---|---|---|---|---|
| | $SiO_2$ | | $Si_3N_4$ | | $Ta_2O_5$ | | $Si_3N_4/SiO_2$ | $Ta_2O_5/SiO_2$ |
| | Model | Simulated | Model | Simulated | Model | Simulated | Model | Model |
| 0.5 | 2.126 | 2.13 | 2.126 | 2.13 | 2.126 | 2.13 | 2.126 | 2.126 |
| 1.0 | 2.418 | 2.42 | 2.418 | 2.42 | 2.418 | 2.42 | 2.418 | 2.418 |
| 1.5 | 2.538 | 2.54 | 2.538 | 2.54 | 2.538 | 2.54 | 2.538 | 2.538 |
| 2.0 | 2.6 | 2.6 | 2.6 | 2.6 | 2.6 | 2.6 | 2.6 | 2.6 |

The variation of drain current with gate-source voltage ($I_D$-$V_G$ characteristics) under CL and QM approach is plotted in Fig. 5 for Fig. 1 structures and the results so obtained are compared with self-consistent results [9]. Close proximity with published results shows the validity of our model. The comparison of drain current curves for CL and QM approach shows an overestimation in CL values and thus proves the incompatibility of CL approach for scaled devices as surface charge density is overestimated. As the gate dielectric is changed to high-*k* (device ii)

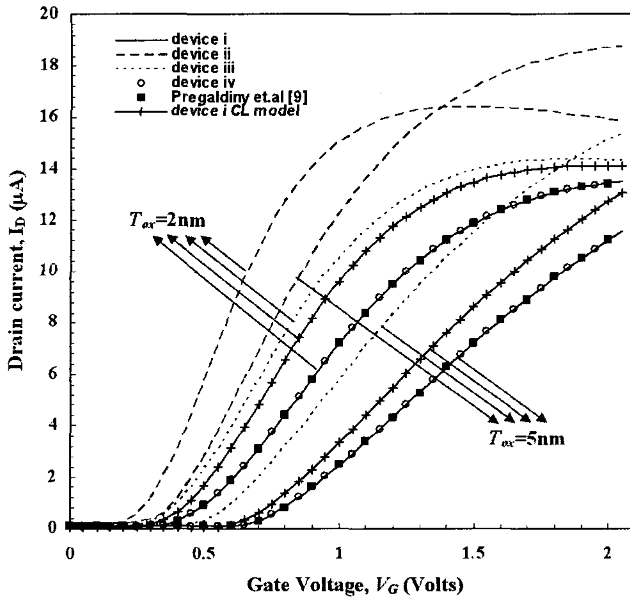


**Fig. 5.** Drain current variation with gate voltage. $V_d$=0.05V, $N_A$=3x10$^{17}$ cm$^{-3}$ and W/L=1.

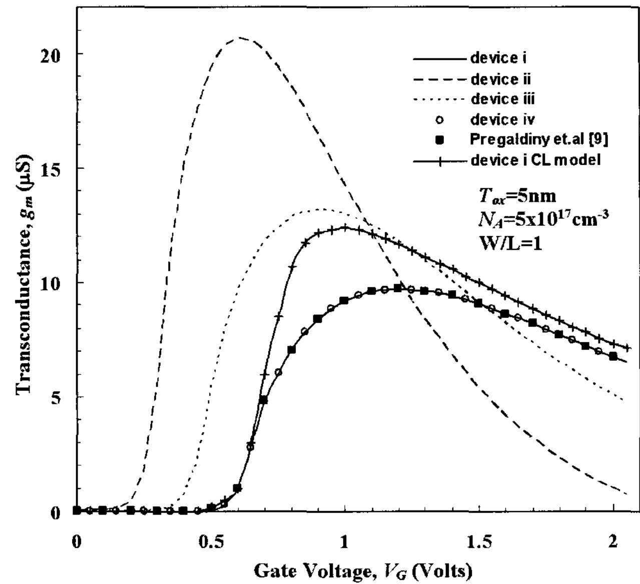


**Fig. 6.** Transconductance versus gate voltage at $V_d$=0.05V.

an enhancement in drain current is seen to that of device i configuration. This is due to an increase in electric field value (by replacement of dielectric) at the interface, leading to early inversion of charges at the same gate bias and thus producing a high value of drain current. On comparison of device iii (having gate-stack structure) with device i an increase in drain current is seen, because although the physical thickness of gate-stack is equal to that of device i, the electrical thickness of both the devices differ, and as the electrical thickness of gate dielectric is reduced in device iii, an increase in drain current can be seen. But, device iv resembles that of device i as it exhibits same device characteristics because the electrical thickness of both gate dielectrics are equal in magnitude. In this way, drain current is optimized for the given dielectric thickness and permittivity, at the same time reducing the gate tunneling of carriers.

Transconductance, an important device parameter is further studied in Fig. 6. Variation of transconductance ($g_m$) with gate-source voltage can be seen in the figure and model matches well with available self-consistent results [9]. One of the well known consequences of the QEs is the degradation of device transconductance, and can be inferred from the figure. Further, an increase in the value of transconductance is seen while switching from device i to device ii or device iii due to the reduction in the electrical thickness and generating more charge density for same physical thickness. The key idea to reduce gate leakage current is served, as shown by device iv characteristics. The increase in physical thickness without compromising desired characteristics is thus achieved by the use of device iv structure.

## IV. Conclusions

A comprehensive analytical surface potential based model with quantization effects has been presented. The poly-depletion effect is also incorporated in this work to analyze its impact on device performance. We can then conclude that ignoring quantum effects and poly-depletion leads to erroneous estimation of various device characteristics. The scaling down limit of silicon-dioxide is analyzed and an alternative is described without compromising gate controllability due to enhanced physical dielectric thickness. This effect of increase in dielectric constant/thickness in gate-stack architectures for the same equivalent thickness well reduces the gate leakage current. Finally, the validity of the model was proven by comparisons with available self-consistent and simulated results for various parameters.

## ACKNOWLEDGMENTS

The authors are grateful to the Department of Science and Technology (DST), Government of India, India for providing the necessary financial assistance to carry out this research work.

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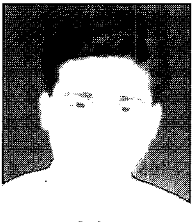

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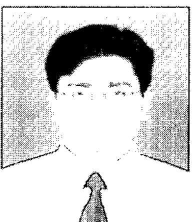

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