# A Novel Low Power Design of ALU Using Ad Hoc Techniques

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## Abstract

This paper presents the comparison and performance analysis for CPL and CMOS based designs. We have developed the Verilog-HDL codes for the proposed designs and simulated them using ModelSim for verifying the logical correctness and the timing properties of the proposed designs. The proposed designs are then analyzed at the layout level using LASI. The layouts of the proposed designs are simulated in Winspice for timing and power characteristics. The result shows that the new circuits presented consistently consume less power than the conventional design of the same circuits. It can also be seen that these circuits have the lesser propagation delay and thus higher speed than the conventional designs.

Key Words : Low power design, ALU, CPL, CMOS,

## 1. Introduction

Due to the emerging battery operated applications for the portable environment and wireless technology, there is a growing need to reduce the power consumption in CMOS (Complementary Metal Oxide Semiconductor) digital circuits while maintaining the computational throughput. Today there are an ever-increasing number of portable applications requiring lowpower and high throughput than ever before. For example, notebook and laptop computers, representing the fastest growing segment of the computer industry, are demanding the same computation capabilities that are found in desktop machines. Developments in personal communication services (PCS's) are equally demanding, such as the current generation of digital cellular telephony networks which employ complex speech compression algorithms and sophisticated radio modems in a pocket sized device. The proposed future PCS applications are even more dramatic with universal portable multimedia access supporting motion full digital video and control via speech recognition. New architectures for reduced power consumption with lowest possible supply voltage are being proposed everyday. These architectures are implemented in various technologies like bi-polar, dynamic logic, domino logic, complementary CMOS, bi-CMOS, pass gate CMOS multiplexer etc. to achieve different objectives such as high speed, low power, and reduced area. Due to the evolution of the shrinking technology and flexible circuits for the portable devices, the research efforts for developing high performance digital systems have been intensified. Portable applications requiring low power circuitry with minimal area are pushing the envelope in the terms of those requirements on the microprocessor designer. Thus, designing low-power digital systems, especially the processor, is becoming equally

important to designing a high performance one [1].

Advanced technology has enabled the building of integrated circuits where gradually more and more transistors can be placed onto a single chip to perform specific functions. Portable applications requiring low power circuitry with minimal area are pushing the envelope in the terms of those requirements on the microprocessor designer. An important element in the design of any processor is its ALU (arithmetic logic unit), which is the basic design block. Due to this, the design of low power ALU is becoming a paramount issue [2], which offers a wide range of tradeoffs in terms of speed, complexity and power consumption. There are several architectures available to design low power ALU at transistor level, each of which offers different characteristics. One such design can be achieved by using the CPL (complementary pass-transistors).

In this paper we have proposed a new technique of a low power 1-bit ALU, which becomes the basis for the bit sliced ALU and other hierarchical designs. The new design of ALU has been employed by using complementary pass transistors. This ALU is designed to perform the Logical functions: AND, OR, XOR, XNOR and INVERTER as well as and the arithmetical function: Full adder, Incrementor and multiplication. We shall be comparing this design with the standard design of an ALU. By looking into aspects like power consumption, cost effectiveness, propagation delays, speed and wiring complexity we shall identify the difference in the two designs. These results are obtained from Silos, LASI and Winspice simulations of the proposed designs.

These days the design can be specified at various levels, like architectural level, layout, process technology and circuit design level. By the proper choice of the technology at various levels the design can be made to work in a more efficient way. At circuit design level, this can be achieved by choosing a kind of combinational logic which employs the least number of gates. This is due to the fact that all the

important parameters governing power dissipation are strongly influenced by the chosen logic style. At layout level the wiring complexity is an important factor contributing towards the efficiency.

The interesting fact in design of proposed ALU is the design of the logical and arithmetic operations, which shows a significant reduction in the number of nMOS and pMOS transistors employed in the design. This results in increasing the speed and a significant reduction in the power consumption and the layout complexity.

## 2. DESIGN OF THE PROPOSED ALU

Fig. 1 shows the proposed design of the low power ALU. At the eight inputs of eight to one multiplexer we have result of the different functions coming in. Three select lines are used for selecting the desired function. The results from the full adder (A + B + Cin) and the incrementor (A + 1) circuit also has a carry and Carryinc respectively along with the Sum. The Sum from these circuits is allowed to propagate through the multiplexer.

We have different output pins coming for Carry and Carryinc. Thus by properly choosing the values of these three select lines we can allow any one of the given operations. Section 4 of this paper describes the circuits of different functions of ALU, which makes a unique design.
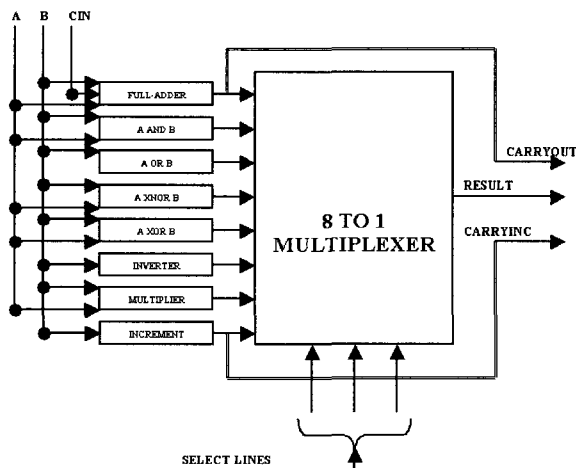


Fig. 1. Block Diagram of Proposed design of ALU.

## 3. COMPONENTS OF ALU

### 3.1 Novel Design of AND-gate and OR-gate

Layouts and the block diagrams of the proposed design of the AND-gate and OR-gate are shown in Fig. 2 (a), (b) and Fig. 3 (a), (b) respectively. Fig. 4 (a) and (b) show the Winspice simulation result for the layout analysis of proposed AND-gate and OR-gate respectively. It can be seen from Fig. 2 (a) and (b) that these designs are based on transfer gate logic [3]. Here the select line of the pass-transistor is shorted

to IN1, to give us OR-gate, whereas the select line of pass-transistor is shorted to IN0, to give us AND-gate. In other words, we can say that in this design the select line will be at the same logic as input-IN1 in case of OR-gate, and IN0 in case of AND-gate.
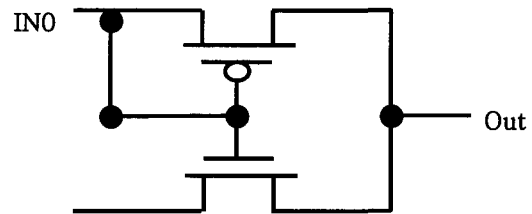


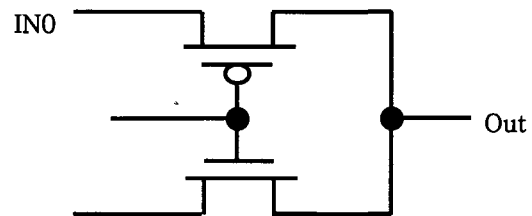Fig. 2. (a) Proposed design of AND-gate.



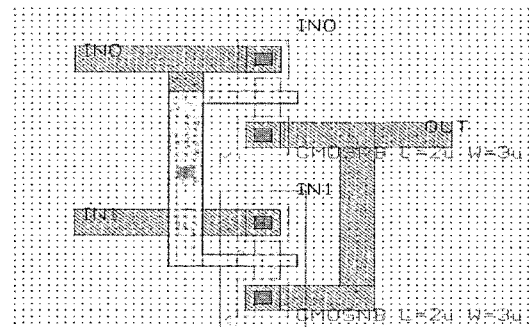Fig. 2. (b) Proposed Design of OR-gate.



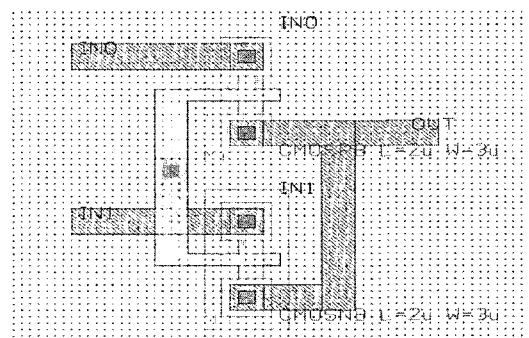Fig. 3. (a) Layout of Proposed Design of AND-gate.



Fig. 3. (b) Layout of Proposed Design of OR-gate.

It can be analyzed that both the circuits behave as the standard CMOS designs of the respective circuits. This can also be seen from the Verilog gate level coding style of both circuits as well. One interesting fact in these two designs is the difference in the number of the pMOS and nMOS

transistors employed for the OR-gate and AND-gate. In the conventional design, same logic is achieved by the use of six transistors, while in the proposed case two transistors are being used for the same function. This significant reduction in the transistor count increases the speed of the circuit, reduces the switching frequency which is an important parameter contributing towards the reduction in the Dynamic Power consumption. Another aspect to note in the proposed design is the absence of the explicit VDD and GND supply requirement.

## 3.2 Novel Design of XOR-gate and XNOR-gate

In this paper we also present the proposed low power designs of XNOR and XOR gates as shown in Fig. 5 (a) and (b) respectively. As seen in the Fig. 5 (a) and (b) these designs employ only four transistors against eight transistors as in the standard designs. There are different low power designs of XNOR and XOR gates [4].
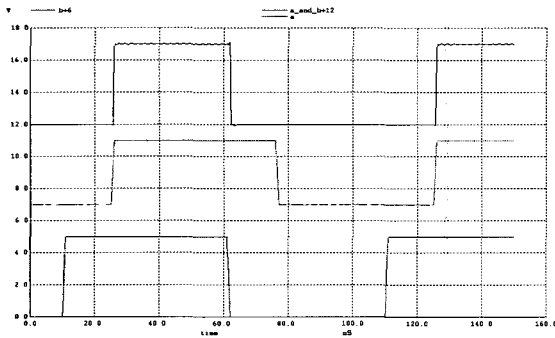


Fig. 4. (a) Winspice Analysis of Proposed Design of AND-gate.
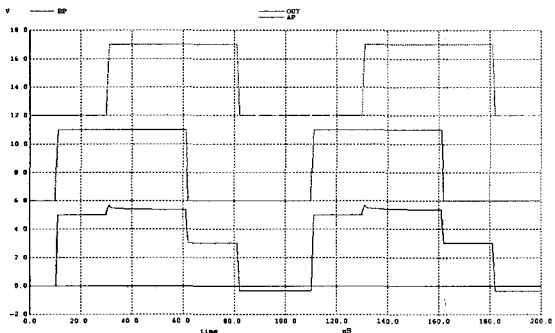


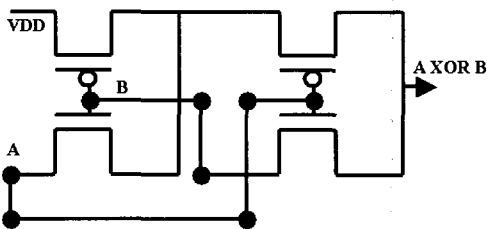Fig. 4. (b) Winspice Analysis of Proposed Design of OR-gate.



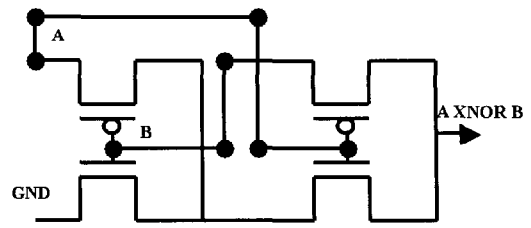Fig. 5. (a) Circuit Diagram of Proposed XOR-gate.



Fig. 5. (b) Circuit Diagram of Proposed XNOR-gate.

These low power designs have certain properties along with some tradeoffs in terms of power consumption and output swing. For example, Wang's XNOR-gate [4]does not have a ground connection, but is based on the CMOS technology, and employs fewer transistors than the standard design of the XNOR-gate. Similarly, the Inverter Based XNOR-gate [5] also employs four transistors. It does not have the ground connection, but it employs an inverter at the input to provide the full voltage swing, and at the output it exploits the property of the pass transistor to save the power consumed. The proposed designs of XNOR and XOR gates are based on transfer gates and thus have lesser propagation delay than other low power designs but will have lower value of output voltage swing [6]. Fig. 6 (a) and (b) shows the layout of the proposed designs of XOR and XNOR [6] gates respectively. Their respective Winspice simulation result can be seen in Fig. 7 (a) and (b). It can be analyzed from the Fig. 7 (a) and (b), that there are small voltage overshoots in the simulation results. This happens when nMOS has to pass logic-1 and pMOS has to pass logic-0. This results in slightly weaker outputs.
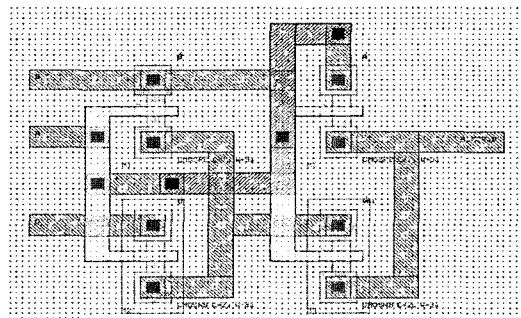


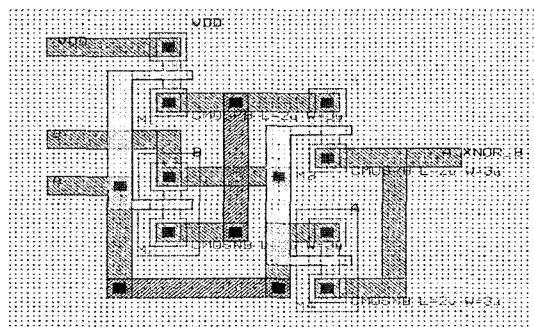Fig. 6. (a) Layout of Proposed Design of XOR-gate.



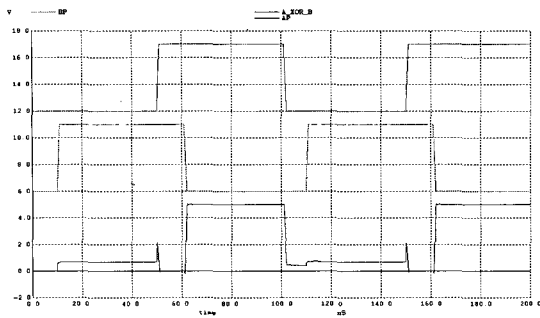Fig. 6. (b) Layout of Proposed Design of XNOR-gate.

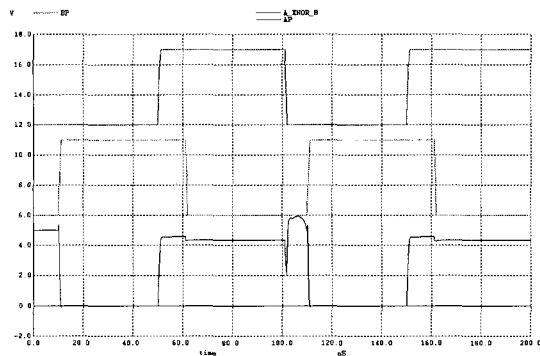Fig. 7. (a) Winspice Analysis of Proposed Design of XOR-gate.



Fig. 7. (b) Winspice Analysis of Proposed Design of XNOR-gate.

## 3.3 Low Power Design of an Incrementor Circuit

In the proposed Low Power ALU we have defined one of the functions to be an incrementor, i.e. A+1, resulting in Sum and Carryinc. Fig. 8 (a) and (b) show the proposed and the standard design for the Incrementor.

The layout of the proposed design of the inverter circuit and its Winspice analysis is shown in Fig. 9 (a) and (b) respectively. From the simulation result it can be analyzed from that due to the presence of the inverter circuit at the output of incrementor it has a good voltage swing. It also consumes less power than the conventional design due to presence of the transfer gate to implement CARRYINC. Notice that proposed design of the incrementor circuit employs four transistors against ten in the standard CMOS design.
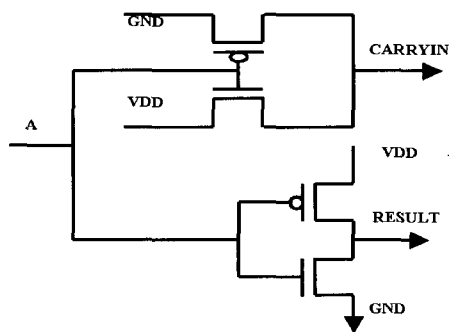


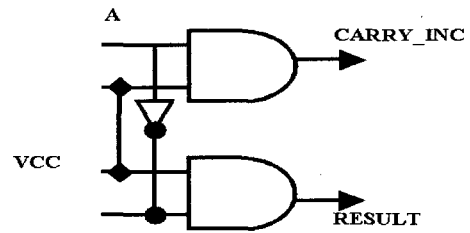Fig. 8. (a) Circuit Diagram for the Proposed Design of the Incrementor.



Fig. 8. (b) Block Diagram for the Standard Design of the Incrementor.
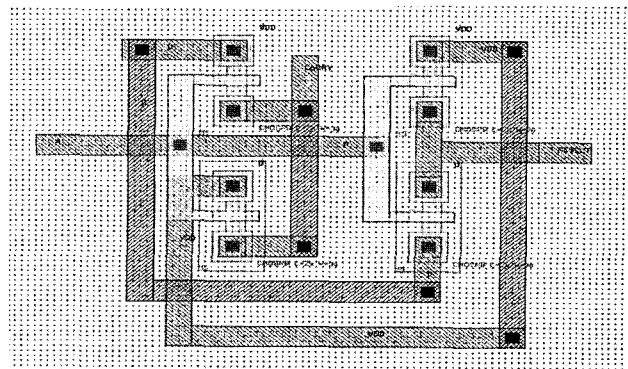


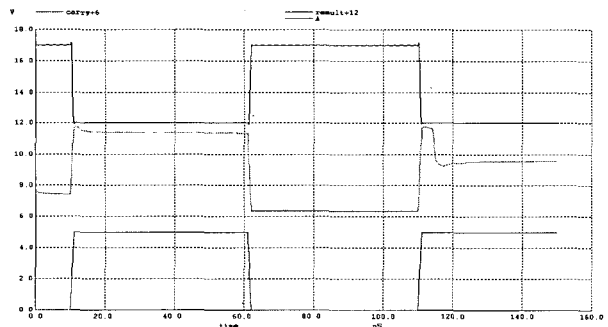Fig. 9. (a) Layout of the Proposed Design the Incrementor Circuit Using LASI.



Fig. 9 (b) Winspice Simulation Analysis for the Layout of the Proposed Design of the Incrementor Circuit.

## 3.4 Other Components of Proposed ALU

The remaining three components of proposed low power ALU are full adder circuit, inverter and the multiplier. The standard CMOS full adder circuit employs twenty eight transistors in its design. There is an existing low power design for the Full Adder [8], which employs only twelve gates against twenty eight as in the standard design. This design is based on the transfer gate, which uses low power due to the absence of explicit power supply. There are some trade-offs in this design in term of the voltage swing and the power consumption. Due to the absence of the VDD and the Ground connection we have a weak output and thus a lower output swing.

The last function that we define in our proposed design of the low power ALU is another logical function, the Inverter circuit. The design of a standard CMOS inverter circuit is the

best design until now. As it not only uses two transistors and has a good fan-in and fan-out value but also provides a good output swing, with pull-up and pull-down network. For this reason CMOS design of the Inverter is also extensively used for the restoration of the swing and also sometimes for boosting the driving capability of the circuit. Therefore we shall be employing this standard design of the inverter circuit in the proposed ALU.

# 4. ANALYSIS OF POWER CONSUMED IN THE PROPOSED DESIGNS

The main reason for implementing the majority of contemporary high-complexity designs in static CMOS is the almost complete absence of power consumption in steady-state mode. According to equation (1) [9] [10], the average power dissipation Pv in digital CMOS circuits include three distinct components.

$$P_v = P_{short\ circuit} + P_{switching} + P_{leakage} + P_{static} \qquad (1)$$

It can be seen from the above equation that the dynamic power dissipation for digital CMOS circuits depends upon clock frequency, transition activity, node capacitance, short circuit current and the power supply VDD.

## 4.1 Dynamic Consumption Due to Load Capacitance

Nodes in the digital circuit toggle between the two logic states, '0' & '1'. During the transition from one state to another, node capacitances need to be charged & discharged. The current passing through either p-channel or n-channel transistor while charging or discharging node capacitances cause the capacitive component $P_{cap}$ of the total power consumed. $P_{cap}$ is given by equation (2).

Here $f_{clk}$ is the clock frequency, VDD is the supply voltage, $C_L$ is the load capacitance and alpha is the transition activity. It can be clearly seen that more is the transition of the states the higher will be the power dissipation. In the proposed model due to the reduced number of transistor count the transition activity is reduced by 60% accounting in the reduced power consumed.

$$P_{switching} = P_{cap} = a \cdot C_L \cdot VDD^2 \cdot f_{clk} \qquad (2)$$

This capacitive load is originated from the capacitance between the gate and diffusion and the interconnecting metal and Polysilicon layers in our layouts shown. This can be substantially reduced by employing fewer transistors in our design and reducing the size of the transistor i.e. the length and the width of the channel to the minimum possible size. Also as mentioned above, there is the square law dependence of capacitive switching power on the supply voltage. Therefore, reducing the supply voltages is an effective means for reduction of $P_{cap}$. In many cases, supply voltage reduction and speed-up design techniques go along with reduction of the clock frequency $f_{clk}$ which reduces the capacitive switching power even further.

## 4.2 Leakage Power

Ideally, digital CMOS circuits should not exhibit any static power consumption at all. However, due to the non ideal sub threshold behavior of real MOSFETs, there is leakage current $I_{leak}$ flowing from the positive power supply to the ground even in the static case resulting in the leakage power $P_{leak}$, which is given by the equation (3)

$$P_{leak} = I_{leak} \cdot VDD \qquad (3)$$

Here, reduction in the requirement for the supply voltage and the number of transistors contributes in a significant reduction of power requirement.

## 4.3 Short Circuit power

Short circuit power (Pshort), is expressed as:

$$P_{short} = (1/2) \cdot a \cdot (t_r \cdot I_{short,max,r} + t_f \cdot I_{short,max,f}) \cdot V_{dd}$$
$$\cdot f_{clk} \qquad (4)$$

Where $I_{short,max,r}$ are the peaks of the currents flowing from positive power supply to ground when n- and p-channel transistors are conducting simultaneously for a infinitely small moment during node transition and tr/f are the fall and rise times of the node voltages. This short circuit power decreases with decreasing the switching activity 'alpha' and decreasing the clock frequency '$f_{clk}$'.

However clock frequency is usually regarded constant in order to fulfill some architectural requirement. So reduction in short circuit power can be achieved by reducing the number of transistors and thereby reduction in the switching activity. It can be observed that in all the cases the power consumed directly depends upon VDDi.e. the supply voltage. Due to the absence of the explicit power supply the theoretically the dynamic power consumed will be negligible, whereas static power consumption will be responsible for the total power consumed by the device.

# 5. CONCLUSION

According to the equations 1, 2, 3 and 4, power consumption mainly depends upon the VDD, number of transistors and switching frequency. So when there is no explicit VDD connection, the short circuit power consumption and the leakage power consumption are reduced substantially. However, there will be static power consumption, but switching power consumption is negligible. It can also be seen from the proposed design of the ALU that it employs thirty transistors in its design against seventy two transistors as in the standard design. . This saves of 58% of transistors. This saving of 58% transistors accounts for about 35% of the saving in the power requirements. Now due to the absence of the explicit power supply requirement the total saving of the power comes to the 60%. This makes the proposed designs an ideal one for devices, which require low power.

However, due the absence of explicit VDD or GND connection the pull-up network and the pull-down network in

the circuit are never formed as in the conventional CMOS technology. Therefore we do not have any means for defining a logic-0. This limits the application of the transfer gate based logic circuits [6] [10]. Yet, these circuits can be used in place of the logic circuits where we are already getting logic-0 or logic-1 from the predecessor gates. We can also connect an inverter at the input and drive at least three of the proposed design gates in series and connect an inverter again at the output. This will provide well defined logic levels at the input and a full voltage swing at the output and the goal of low power design is achieved as well.

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