Separation and Quantification of Parasitic Resistance in Nano-scale Silicon MOSFET

Jun-Ha Lee† , Hoong-Joo Lee*, Young-Jin Song and Young-Sik Yoon*****

Abstract - The current drive in a MOSFET is limited by the intrinsic channel resistance. All other parasitic elements in a device structure perform significant functions leading to degradation in the device performance. These other resistances must be less than 10%-20% of the channel resistance. To meet the necessary requirements, the methodology of separation and quantification of those resistances should be investigated. In this paper, we developed an extraction method for the resistances using calibrated TCAD simulation. The resistance of the extension region is also partially determined by the formation of a surface accumulation region that gathers below the gate in the tail region of the extension profile. This resistance is strongly affected by the abruptness of the extension profile because the steeper the profile is, the shorter this accumulation region will be.

Keywords: extraction, nano-scale MOSFET, parasitic resistance, quantification, separation

1. Introduction

In recent high density silicon devices, local properties caused by such things as dopant density variation, and structural and chemical uniformity of the dielectric layer affect the stability and reliability of the device operation [1]. With sizing effect, local dopant density variation also affects the characteristics and performance of the devices [2]. Ideally, the driving current of the MOSFET (metal oxide semiconductor field effect transistor) is controlled by the channel resistance, but the other resistive components, realistically, are major causes of the performance deterioration of the device [3]. So far, many studies have been done on the doping profiles and device structure in order to minimize the intrinsic and parasitic resistance in the MOSFET structures. However, they primarily use the mobility enhancement of the carrier as a main control factor. As a result they only provide information related to channel engineering. The parasitic resistance and capacitance, which bring about both the lowering of the current driving and the increment of the node capacitance, consequently have an effect on the CMOS (complementary metal oxide semiconductor) delay. It has been reported that both the shallow junction and the heavily doped extension, which are the methods to minimize the off-current and to stabilize the on-current of the sub-100nm scaled device known as the nano-scale device, can solve the short-channel effect and manufacturing difficulties [4-5]. In this study, performance improvement for high speed and high performance type devices has been presented through the resistance study using TCAD (technology computer aided design) simulation. The proposed method makes it possible to effectively extract the optimized process window by analyzing the relation between the process parameters and parasitic resistance and through the sensitivity analysis of the parasitic resistance in each region of the device.

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Received August 1, 2004 ; Accepted March 8, 2005

2. Principles and Method

2.1 Calculation of Parasitic Resistance

Fig. 1 depicts five resistive components and current flows that must be considered in MOSFET devices [6]. As the decrease of the source current lowers the gate driving ability, the source region must be thoroughly analyzed. Among five resistive components, ① to ④ are parasitic resistances. Each is classified as the contact resistance, the shunt resistance, the extension resistance and the accumulation resistance. ⑤ is the intrinsic channel resistance. Although Fig. 1 shows the transistor diagram without the cobalt silicide layer fabricated by the SALICIDE process, in reality, the resistance extraction has nothing to do with the silicide layer. The sheet resistance of each region is extracted by eq. (1) [7]. The current and quasi-fermi potential were used from the simulation results Using eq. (1), we can obtain the value of sheet resistance at

each node point along the x-axis.

$$I_{ds} = \int_0^\infty J(y)dy = \frac{d}{dx}\phi_n(x)\int_0^\infty qn(x,y)\mu(x,y)dy = \frac{\frac{d}{dx}\phi_n(x)}{R_{sh}(x)} \quad (1)$$

where x is the horizontal scale, Φn or Φp are electron/hole quasi-Fermi potentials, and Ids is the total current.

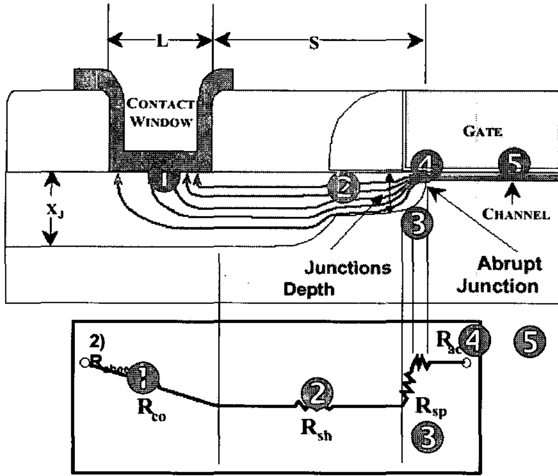

Fig. 1 The resistance part of the MOSFET

2.2 Process/Device simulation

To extract the substantial current values and quasi-fermi level in each region for a given process condition [8], the simulator calibration must be preceded in order that the results from the process and device simulation have the equivalent doping level and mobility value as those of the real device. In this paper, n/pMOS devices of which source/drain activation have been carried out by normal-RTA (rapid thermal annealing) and spike-RTA, have been used as targets of the calibration [9-10].

Fig. 2 presents the comparison between simulation results and measures of Lgate (gate length) versus Vth (threshold voltage). The results from the TCAD simulation show a good agreement with the electrical characteristics of the real device, based on the comparison between the simulation and measure for correlation of Idsat (saturation current) versus Ioff (off state current). The solid lines in Fig. 2 represent measurement values for the real device, and the dotted lines describe the simulation values. The error between measure and simulation has shown to be less than 10% for n/pMOS to which both the spike-RTA and normal-RTA have been applied. The error between measure and simulation for Idsat-Idoff curve from the short-channel region of the device to which only the normal-RTA has been applied, has shown to be greater than 10%.

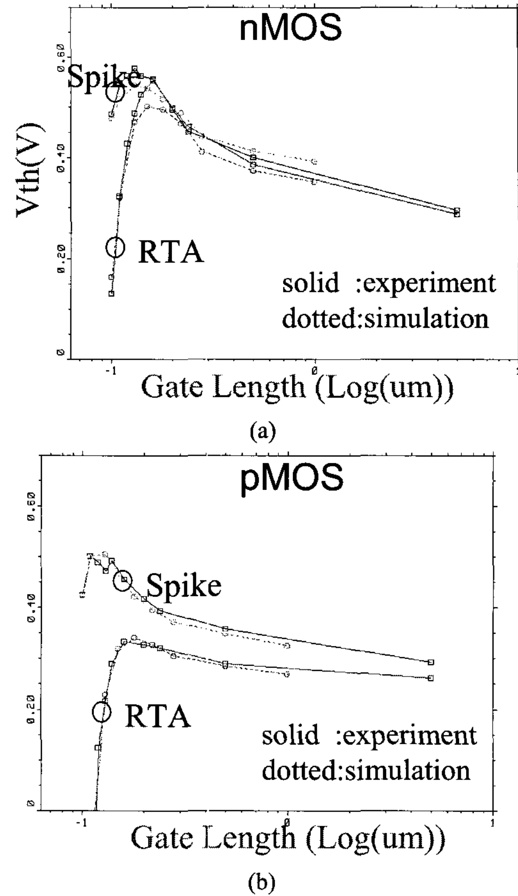

Fig. 2 The Lgate-Vth curve from TCAD simulation (a) nMOS (b) pMOS

3. Simulation Results

3.1 Separation & Quantification of Resistance

Fig. 3 shows the extracted sheet resistance for x-axis position for the nMOS device. The line represents the spike-annealed process, and the symbolized line represents the normal-RTAed process. The junction contours for each process are depicted using the dotted lines. A 25% shallower junction depth of 750Å for the case of spike-RTA has been obtained compared to the 1000Å junction depth for the normal-RTA. The proposed five resistive regions can be easily separated considering carefully the junction contour and the gate edge. The extracted resistance values from Fig. 3 are tabulated into Table 1 and Table 2. The spike-RTA demonstrates the larger total resistance compared to the normal-RTA due to incomplete activation with the shallower junction depth [11]. For both cases, the parasitic resistance is about 15% of the total resistance. Moreover, it is 17% of the channel resistance, which is similar to that introduced in ITRS (international technology roadmap semiconductor) [12].

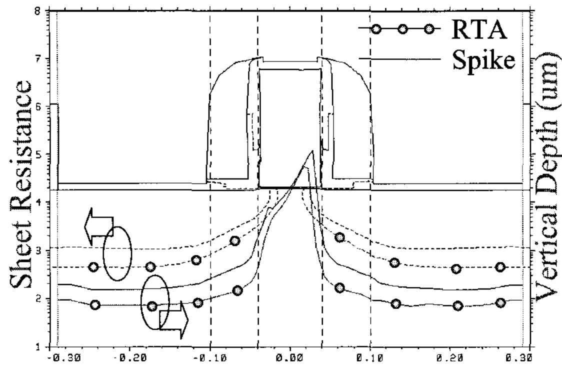

Fig. 3 Junction contour and sheet-resistance of nMOS

Table 1 Resistance component of RTA-annealed nMOS

nMOS RTA-anneal	Percentage (%)	Resistnace value (Ω)
Total Resistance	100	1041
Channel Resistance	86	892
Parasitic Resistance	14	149
Accumulation Resistance	5	50

Table 2 Resistance component of Spike-annealed nMOS

nMOS Spike-anneal	Percentage (%)	Resistance value (Ω)
Total Resistance	100	1847
Channel Resistance	85	1574
Parasitic Resistance	15	273
Accumulation Resistance	4	71

Fig. 4 shows the doping contour and the sheet resistance for the normal-RTA annealed pMOS device. The red contour lines represent the same doping concentration, and for the case of the pMOS device, the extension region is not shown to be indistinguishable from the source/drain region. Furthermore, the reason why the junction of the extension region of the pMOS device is deeper than that of the nMOS device is that it is difficult to achieve shallow and abrupt doping profiles due to the TED (transient enhanced diffusion) for the boron impurities [13]. The simulation value of the junction depth is about 1200Å. Parasitic resistances are also separated according to the separated regions shown in Figure 4. The green line represents the steep increase of sheet-resistance in the accumulation region, which means the parasitic resistance increases in proportion to the length of the accumulation region. In case of pMOS, the parasitic resistance forms about 23% of the total resistance, and also totals 30% of the channel resistance shown in Table 3. The spreading resistance is about 18% of the total resistance. Since 65% of the parasitic resistance is Racc (accumulation resistance), which is analyzed in Table 4, the parasitic resistance value is found to be quite high. Because the boron profile in the tail region is not abrupt enough, the excessive overlap beneath the gate has increased accumulation resistance. Therefore, the parasitic resistance can shrink into its half similar to the case of nMOS, if the Racc, 15% of the total resistance, is semi decreased [14-15].

Table 3 Resistance component of RTA-annealed pMOS

pMOS	Percentage (%)	Resistance value (Ω)
Total Resistance	100	489
Channel Resistance	77	376
Parasitic Resistance	23	113

Table 4 Analysis of resistance in the parasitic region

pMOS Parasitic Resistance	Percentage (%)	Resistance value (Ω)
Shunt(S/D) Resistance	2.2	11
Extension Resistance	2.0	10
Spreading Resistance	3.8	18
Accumulation Resistance	15.0	74

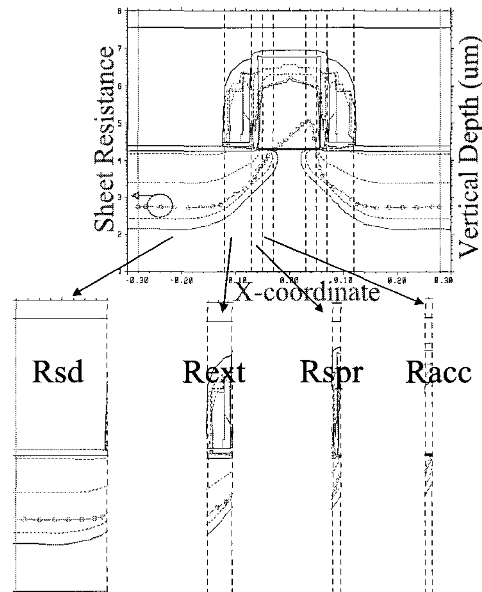

Fig. 4 Junction contour and sheet-resistance of pMOS

3.2 Analysis of the Contact Resistivity

Cobalt-silicide/silicon contact resistance is expected to compose a large portion of the parasitic resistance. The current flows on the distributed paths from the extension to the contact, and the exact path depends on the doping profiles and the device structure. The effective contact resistance is thus affected by the current flow lines, as well as the contact area of silicon and cobalt [16-17].

As silicidation consumes silicon atoms, the highly doped source/drain region could disappear or be located in the

silicide area. In this case, the resistivity of the silicide or the highly doped silicon region depends on the doping level in the adjacent region to the silicide. The doping level in the silicon near the cobalt silicide has been analyzed using the SIMS (secondary ion mass spectroscopy) measurement. As shown in Fig. 5, for the pMOS, the severe segregation of boron impurities occurs in the silicon region adjacent to the cobalt silicide, which becomes more serious with the higher temperature of silicidation. Therefore, the initial ion-implantation energy, the silicidation process condition, and the silicide thickness should be optimized to minimize the contact resistance. Additionally, the cross-sectional area of the current path must be maximized.

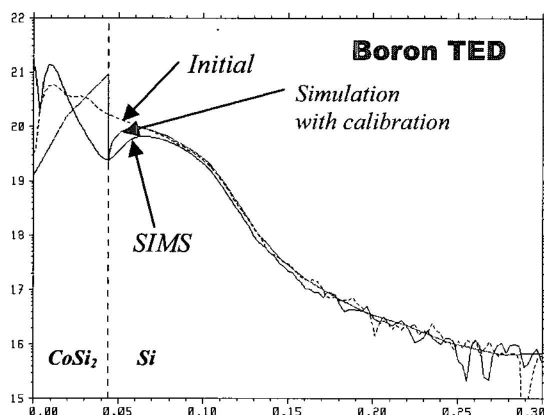

Fig. 5 Doping level adjacent to the Co-silicide

4. Conclusion

This paper has analyzed the resistive components of the contact that result in lowering the device performance. A flow has been proposed to obtain the sheet resistance at each node with the current values and quasi-Fermi levels calculated by the calibrated TCAD simulation. The rate between the channel resistance and the parasitic resistance as well as four parasitic resistive components and their relation to the normal and spike-RTA annealed n/pMOS devices, has been extracted to determine optimal process condition. Also, this work has presented the methods to optimize the contact resistivity depending on the doping level in the silicon adjacent to the cobalt silicide region. The proposed method can make it possible to effectively obtain the process window to minimize parasitic resistance in high speed devices.

References

[1] C. J. Kang, D. Jeon, and Y. Kuk, "Channel length effect in a MOSFET structure by scanning capacitance microscopy," *Surface Science*, vol. 544, iss. 1, pp. 87-92, Oct. 2003.

[2] R. J. Luyken, T. Schulz, J. Hartwich, L. Dreeskornfeld, M. Stadele, and W. Rosner, "Design Considerations for Fully Depleted SOI Transistors in the 25-50 nm regime," *Solid-State Electronics*, vol. 47, no. 7, pp. 1199-1204, July 2003.

[3] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, MA: Cambridge Univ. Press, pp. 30-45, 1998.

[4] Y. Taur, "MOSFET channel length extraction and interpretation," *IEEE Trans. Electron Devices*, vol. 47 pp. 160-170, Jan. 2000.

[5] S. D. Kim, C. M. Park, and J. Woo, "Advanced Model and Analysis for Series Resistance in Sub-100nm CMOS including Poly-depletion and overlap doping gradient effect," in *Proc. IEDM '00*, pp. 723-726, 2000.

[6] K. K. Ng and W. T. Lynch, "Analysis of the gate-voltage-dependent series resistance of MOSFETs," *IEEE Trans. Electron Devices*, vol. 33, pp. 965-972, July 1986.

[7] M. Y. Kwong, C. H. Choi, R. Kasnavi, P. Griffin, and R. Dutton, "Series Resistance Calculation for Source/Drain Extension Regions Using 2-D Device Simulation," *IEEE Trans. Electron Devices*, vol. 49, no. 7, July 2002.

[8] P. Degond and A. Ayyadi. "A Coupled Schrödinger Drift-Diffusion Model for Quantum Semiconductor Device Simulations," *Journal of Computational Physics*, vol. 181, pp. 222-228, 2002.

[9] J. H. Lee, K. D. Lee, K. H. Lee, T. K. Kim, Y. K. Park, and J. T. Kong, "Systematic Global Calibration of a Process Simulator," in *Proc. MSM2000*, 2000, pp. 121-125.

[10] A. Magna, P. Alippi, L. Colombo, and M. Strobel, "Atomic scale computer aided design for novel semiconductor devices," *Computational Materials Science*, vol. 27, iss. 1, pp. 10-15, Mar. 2003.

[11] J. O. Borland, "Low Temperature Shallow Junction Formation for 70nm Technology Node and Beyond," in *Proc. Mat. Res. Soc. Symp*, pp. 1-8, 2002.

[12] *International Technology Roadmap for Semiconductors*, SEMATECH, Austin, TX, 2001.

[13] B. S. Kim, H. U. Jeong and H. W. Lee, "Effects of Tungsten Size and Nickel Addition in DC acr Resistance of Cu-W Electrode," KIEE Int. Trans. On EA, Vol.4-C, No.2, pp. 68-72, 2003.

[14] C.M. Osburn and K.R. Bellur, "Low parasitic resistance contacts for scaled ULSI devices," *Thin Solid Films*, vol. 332, pp. 428-436, 1998.

[15] T. H. Gil, H. S. Kim and Y. S. Kim, "Characteristics of Ni/SiC Schottky Diodes Grown by ICP-CVD,"

KIEE Int. Trans. On EA, Vol.4-C, No.3, pp. 111-116, 2004.
[16] Y. M. Kim, I. S. Yu and J. H. Lee, "Fabrication and Characterization of Silicon Probe Tip for Vertical Probe Card Using MEMS Technology," KIEE Int. Trans. On EA, Vol.4-C, No.4, pp. 149-154, 2004.
[17] S. H. Woo and H. S. Lee, "Characteristics of Electron Beam Extraction in Large Area Electron Beam Generator," KIEE Int. Trans. On EA, Vol.4-C, No.1, pp. 10-14, 2004.

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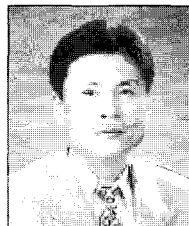

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