Digital Control of UPS Inverter with Time Response Specifications

Young-Tae Woo*, Jae-Sik Kim and Young-Chol Kim †**

Abstract - In this paper, a digital controller for satisfying time response requirements for UPS inverters is designed in a fixed sampling time. The CRA (Characteristic Ratio Assignment) is used as the continuous time design method to deal with the problems of overshoot and settling time. The main design approaches are the inward and outward approaches based on a double-loop feedback structure. The continuous-time controller is discretized by the emulation method. The performances of the proposed controller are evaluated through several simulations carried out with Simpower System Toolbox 3.0 from Simulink®.

Keywords: CRA, Digital Control, Inward Approach, Outward Approach, UPS Inverter

1. Introduction

In most modern UPS inverters, the system requires a controller that results in the following performances: maintaining the desired output voltage waveform, faster response, and lower total harmonic distortion (THD) during all loading conditions. Several different methods for the achievement of these objectives have been presented [1]. However, there are few constructive methods that are applicable to the controller design problems for which time response requirements are satisfied. In addition, inverter systems with feedback controllers are generally constructed in the form of double-loop feedback. This consists of a current-feedback loop as an inner loop and a voltage-feedback loop as an outer loop. Each loop has its own compensator. One of the most difficult problems associated with this control structure arises from the fact that the two loops are closely interconnected, so that each controller cannot be designed independently. Another problem may occur with a fixed sampling time when a digital controller is used. It is well known that in the case of a digital controller determined by the emulation method, low sampling rate has been a constraint. As a result, one cannot make the speed of response faster than a certain value. In many cases, the digital controller for UPS inverters must be designed under a given, specified sampling time because of cost limitations. As well, the sampling time is limited by the switching frequency of the PWM inverter.

In this paper, we present two different design approaches for the digital controller of a single phase UPS inverter. The specifications to be satisfied are the THD less than 5%, a small overshoot in response to an abrupt load change (e.g., the case of a full load applied from a no load state at the peak phase of output voltage), and a fast step response. The sample frequencies for the PWM inverter and the controller used here are 8 kHz. The performance evaluations of the resulting system are conducted under the conditions of no load, and a resistive load of 10[kW]. Digital control design is normally dealt with by means of either the discrete design or the emulation method. In this paper, only the emulation method is dealt with. In other words, we first design a continuous time controller for a continuous time plant, and then make the discretization of the controller with the previously given sampling time. The weakest point of this method is that its fidelity depends on the sampling rate and on the discretization method. But it has a big advantage in that one can apply sufficient design methods developed for continuous-time linear systems. The design approaches that we consider here are as follows: (1) the inward approach and (2) the outward approach based on a double-loop feedback structure. Basically, the inward approach has a control structure in which PI and first-order controller are occupied. On the other hand, the outward approach requires a first-order controller and an IMC (Internal Model Control) controller.

In these two approaches, the orders of each controller in the individual loops, which have been properly selected a priori, are equal to or less than 2. Also, the time-delay effect due to zero-order holder and processing time are modeled in the loop when the continuous-time controller is designed. In the inward approach, all controllers in both inner and outer loops are designed simultaneously so as to meet the performance requirements as well as stability of

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the overall system. But one must examine whether the dynamics of the resulting inner loop have the proper time response characteristics. If the response is too fast compared with the sampling rate, the digital implementation of such a controller may lose stability. In the outward approach, the design process is divided into two steps: the inner loop controller is first determined and then the outer loop controller is designed. In both approaches, we apply characteristic ratio assignment (CRA) [2] to achieve the time response requirements. In view of the performance, it is important to note that (1) PI and first-order controller in the inward approach has a fast transient response and relatively small overshoot but it cannot evade the phase delay effect of output response and, (2) IMC controller in outward approach eliminates the phase delay effect but inevitably increases the order of the system.

This paper consists of four main parts. Section 2 provides the mathematical model of an UPS inverter and its system parameters. Theoretical background on the design method (CRA) is also introduced there. Section 3 presents the procedure for designing a digital controller by way of the inward and outward approaches. In Section 4, performances of the proposed controllers are evaluated from the simulation results carried out by Simpower System Toolbox 3.0 from Simulink®. Finally, concluding remarks are provided in Section 5.

2. UPS inverter model and CRA

In this section, the model of an UPS inverter is developed and described as a transfer function. In addition, the system parameters in this configuration and some theoretical background on the CRA are given.

2.1 Basic configuration of UPS Inverter

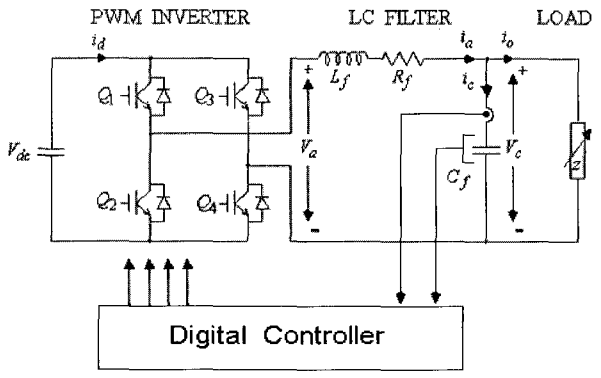

Fig. 1 Configuration of UPS inverter system

Fig. 1 shows the basic configuration of a single-phase UPS inverter system. From Fig. 1, we can draw the block diagram for a UPS inverter system as shown in Fig. 2. The variables V_{dc}, i_d, i_o, V_a and Q_i denote DC-link voltage and current, inductor current, inverter output voltage, and IGBT switching elements, respectively. To model this plant, we consider the feedback variables: the capacitor current i_c and the capacitor voltage V_c. Then the transfer function from $V_a(s)$ and $I_o(s)$ to $V_c(s)$ is expressed by

$$V_c(s)=\frac{1}{L_fC_fs^2+R_fC_fs+1}V_a(s)-\frac{L_fs+R_f}{L_fC_fs^2+R_fC_fs+1}I_o(s). \quad (1)$$

Furthermore, we have the following transfer functions for inner loop $G_I(s)$ and outer loop $G_O(s)$.

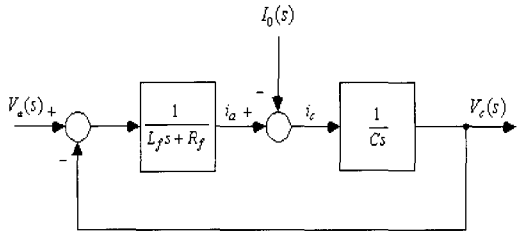

Fig. 2 Block diagram of UPS inverter

$$G_I(s)=\frac{I_c(s)}{V_a(s)}=\frac{C_fs}{L_fC_fs^2+R_fC_fs+1}, \quad (2)$$

$$G_O(s)=\frac{V_c(s)}{V_a(s)}=\frac{1}{L_fC_f(s)s^2+R_fC_fs+1}. \quad (3)$$

In the frame of the digital control scheme for the UPS inverter, the system parameters in Table 1 below are used for both of the proposed approaches.

Table 1 System parameters

System parameters		Values
Filter	Filter inductance (L_f)	200[μH]
	Filter resistance (R_f)	0.08[Ω]
	Filter capacitance (C_f)	120[μF]
Input voltage $(V_c^*(t))$		±150[V]
DC-link (V_{dc})		270[V]
IGBT's switching frequency (f_{switch})		8[kHz]
Sampling frequency (f_s)		8[kHz]

2.2 Theoretical background on CRA

2.2.1 Definitions

Let us consider a real characteristic polynomial as

follows:

$$\delta(s) = a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + a_0, \ \forall a_i > 0 . \quad (4)$$

Herein, we define characteristic ratios as

$$\alpha_1 = \frac{a_1^2}{a_0 a_2}, \ \alpha_2 = \frac{a_2^2}{a_1 a_3}, \cdots, \ \alpha_{n-1} = \frac{a_{n-1}^2}{a_{n-2} a_n}, \quad (5)$$

and the generalized time constant as

$$\tau = \frac{a_1}{a_0}. \quad (6)$$

Then the coefficients, a_i, of $\delta(s)$ can be represented in terms of α_i s and τ as follows:

$$a_1 = a_0 \tau , \quad (7)$$

$$a_i = \frac{a_0 \tau^i}{\alpha_{i-1} \alpha_{i-2}^2 \alpha_{i-3}^3 \cdots \alpha_2^{i-2} \alpha_1^{i-1}}, \ i = 2,3,\cdots,n. \quad (8)$$

It is evident that the corresponding polynomial $\delta(s)$, can be rewritten completely in terms of α_i s, τ and a_0.

τ is related to the speed of the time response of $\delta(s)$, and the α_i s is related to the damping and stability [2]. From these results, we can expand the properties of α_i to an all-pole transfer function.

Theorem 1 [2]: Let $G(s)$ be an all-pole transfer function:

$$G(s) = \frac{a_0}{\delta(s)} = \frac{a_0}{a_n s_n + \cdots + a_1 s + a_0}, \ a_i > 0$$

and let α_i s be the characteristic ratios of $\delta(s)$. Then

1) the frequency magnitude function $|G(j\omega)|$ is monotonically decreasing and
2) $\delta(s)$ has Hurwitz stability if the following two conditions hold:

A) $\alpha_1 > 2$;

B) $\alpha_k = \frac{\sin(\frac{k\pi}{n}) + \sin(\frac{\pi}{n})}{2\sin(\frac{k\pi}{n})} \cdot \alpha_1$, for $k = 2,3,\cdots,n-1$.

Theorem 1 shows how to construct an all-pole stable transfer function whose magnitude is monotonically decreasing. The construction mechanism involves only α_1 which we require to be greater than 2. This result allows us to characterize the reference all-pole systems by adjusting a single parameter, α_1, to achieve the desired damping. Since the generalized time constant τ, can be chosen independently of α_i, the coefficients of $\delta(s)$ are calculated as follows: For arbitrary a_0 and τ,

$$a_1 = \tau a_0 , \quad (9)$$

$$a_i = \frac{\tau^i a_0}{\alpha_{i-1} \alpha_{i-2}^2 \alpha_{i-3}^3 \cdots \alpha_1^{i-1}}, \ \text{for} \ i = 2,3,\cdots,n. \quad (10)$$

It is seen that for $\alpha_1 > 2$, larger values of α_1 correspond to greater damping in all-pole transfer functions. Fig. 3 presents the relationship between overshoot and α_1.

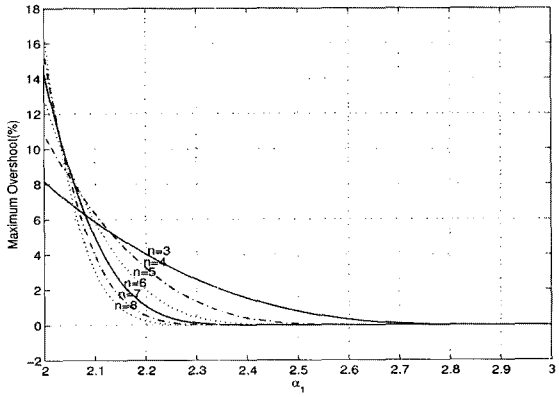

Fig. 3 Relationship between overshoot and α_1

2.2.2 Stability conditions in terms of α_i

The sufficient conditions for Hurwitz stability and instability expressed in terms of α_i are as follows:

Theorem 2 [3] $\delta(s)$ is stable if

$$\sqrt{\alpha_i \alpha_{i+1}} > 1.4656 \ \text{for} \ i = 1,2,\cdots,n-2 . \quad (11)$$

Theorem 3 [3] $\delta(s)$ is stable if

$$\alpha_i > 1.2374 \alpha_i^* \ \text{for} \ i = 2,3,\cdots,n-2 . \quad (12)$$

Theorem 4 [3] $\delta(s)$ is unstable if

$$\alpha_i \alpha_i^* < 1 \ \text{for} \ i = 1,2,\cdots,n-2 \quad (13)$$

3. Digital Controller Design

In this section, we design each continuous controller

using the proposed two approaches. The order of each controller in the individual loops, which has been properly selected a priori, is equal to or less than 2. Also, the time delay effect due to zero-order holder and processing time is modeled in the loop when the continuous time controller is designed. Lastly, the designed continuous-time controller is discretized by applying the Tustin approximation.

3.1 Digital Controller Design by Inward Approach

In the inward approach, all proposed controllers in both inner and outer loops are designed simultaneously so as to meet the performance as well as stability requirements of the overall system. Also the configuration, called the two-parameter configuration, is used in each loop. It implies that the effect of adding 'zero' to the overall transfer function of the closed loop does not exist. The time response characteristics of the inner loop and its relation to the sampling rate are taken into consideration. Fig. 4 indicates the proposed control scheme in which PI and first-order controllers are occupied for the inward approach.

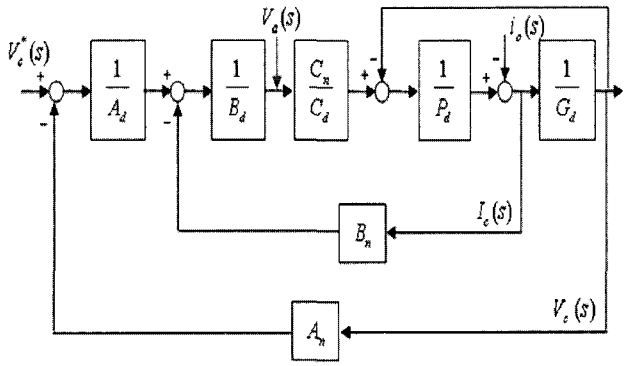

Fig. 4 Block diagram of controller (Inward Approach)

In Fig. 4, the model blocks are denoted by the following symbols:

PI controller: $\frac{A_n}{A_d} = \frac{b_1 s + b_0}{s}$,

First-order controller: $\frac{B_n}{B_d} = \frac{a_1 s + a_0}{s + a_2}$,

L-C filter: $\frac{1}{P_d} = \frac{1}{L_f s + R_f}$, $\frac{1}{G_d} = \frac{1}{C_f s}$,

Zero-order holder: $\frac{C_n}{C_d} = \frac{1 - \frac{3T_s}{4} s}{1 + \frac{3T_s}{4} s}$.

Herein, T_s denotes the sampling time, and the value of each parameter is referred to in Table. 2. Then the transfer function of the closed-loop system is expressed by

$$\frac{V_c^*(s)}{V_c(s)} = \frac{n(s)}{p(s)} \tag{14}$$

where

$$n(s) = C_n,$$

$$\begin{aligned} p(s) &= G_d P_d B_d C_d A_d + G_d A_d C_n B_n + C_n A_n + B_d C_d A_d \\ &= \frac{3C_f L_f T_s}{4} s^5 + \left(-\frac{3C_f T_s a_1}{4} + \frac{3C_f L_f a_2 T_s}{4} + \frac{3C_f R_f T_s}{4} + C_f L_f \right) s^4 \\ &\quad + \left(C_f a_1 - \frac{3C_f T_s a_0}{4} + \frac{3T_s}{4} + C_f R_f + \frac{3C_f R_f a_2 T_s}{4} + C_f L_f a_2 \right) s^3 \\ &\quad + \left(C_f R_f a_2 + 1 + \frac{3T_s a_2}{4} + C_f a_0 - \frac{3T_s b_1}{4} \right) s^2 + \left(b_1 - \frac{3T_s b_0}{4} + a_2 \right) s + b_0. \end{aligned}$$

Next, we set the target polynomial of the overall system. In section 2.2, it is shown that the polynomial can be generated by using (5) and (6) with holding conditions of (7) and (8). Therefore, by selecting $a_0 = 2.31*10^7$, $\alpha_1 = 2.8$ and $\tau = 1m[\text{sec}]$, we make the target polynomial as

$$\begin{aligned} p^*(s) = {} & 2.25*10^{-12} s^5 + 9.05*10^{-8} s^4 + 1.3*10^{-3} s^3 + 8.25 s^2 \\ & + 2.31\times 10^4 s + 2.31\times 10^7. \end{aligned} \tag{15}$$

Then the control gains are determined from the algebraic relation between $p(s)$ and $p^*(s)$ as follows:

$$\begin{bmatrix} a_2 \\ a_1 \\ a_0 \\ b_1 \\ b_0 \end{bmatrix} = \begin{bmatrix} 4.15*10^4 \\ 2.47 \\ 1.19*10^4 \\ -1.63*10^4 \\ 2.31*10^7 \end{bmatrix}. \tag{16}$$

Fig. 5 illustrates the Simulink® block of the voltage loop controller. Fig. 6 shows the current loop controller.

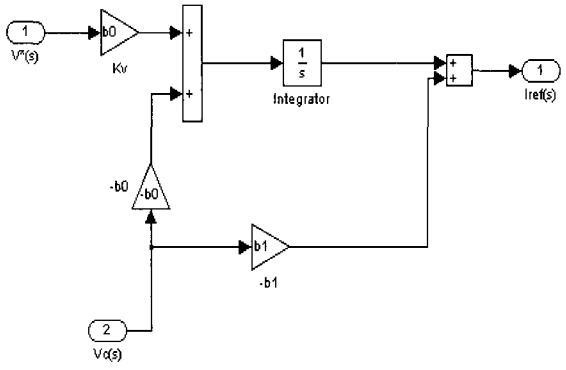

Fig. 5 Voltage loop controller (Inward Approach)

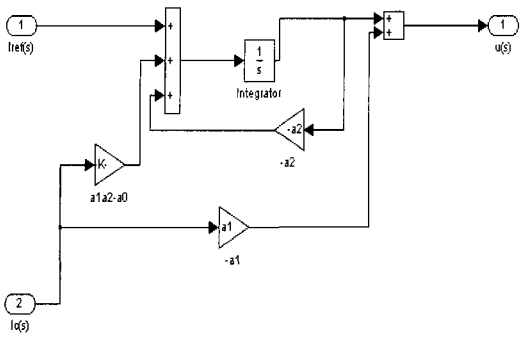

Fig. 6 Current loop controller (Inward Approach)

Lastly, applying digitization by the Tustin approximation to the designed continuous-time controller, the digital controller is given by

$$C_{inner,inward}(z) = \frac{0.9z + 0.48}{z + 0.44}, \tag{17}$$

$$C_{outer,inward}(z) = \frac{-0.26z^2 + 0.05z + 0.31}{z^2 - 0.56z - 0.44}. \tag{18}$$

Fig. 7 presents the digital controller determined by the inward approach.

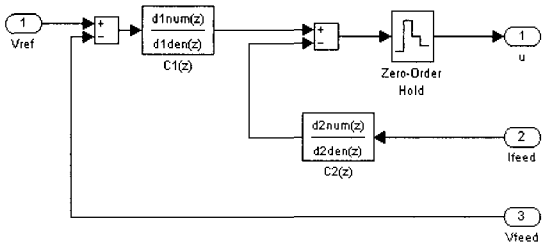

Fig. 7 Digital controller (Inward Approach)

3.2 Digital Controller Design by Outward Approach

In the outward approach, the design process consists of two main steps: first the inner loop controller is determined and then the outer loop controller is designed. Fig. 8 shows a block diagram in which the control scheme for the outward approach is included.

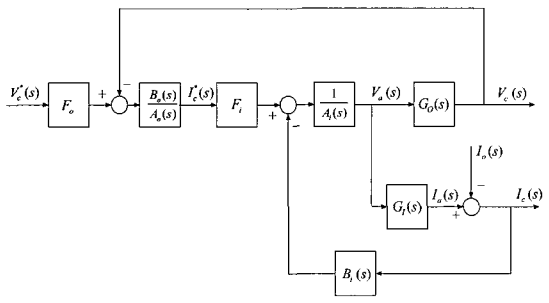

Fig. 8 Block diagram of controller (Outward Approach)

In Fig. 8, $G_I(s)$ and $G_O(s)$ are expressed by (2), (3) in section 2.1. The controller model blocks are denoted by the following symbols:

$$\text{First-order controller: } \frac{B_i(s)}{A_i(s)} = \frac{x_1 s + x_2}{s + x_3},$$

$$\text{IMC controller: } \frac{B_o(s)}{A_o(s)} = \frac{x_4 s + x_5}{s^2 + 2\varsigma\omega_n + \omega_n^2}.$$

Here, the values of $\varsigma = 0.3$ and $\omega_n = 120 * \pi$ of the IMC controller are predetermined by considering the characteristics of the input signal. The value of each parameter is referred to in Table. 2.

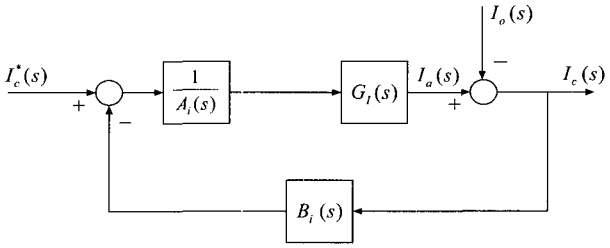

Fig. 9 Block diagram of current loop controller

In the first step, we design the controller for the inner loop $G_I(s)$ to eliminate the disturbances. This means that the overall transfer function of the inner loop should have a fast step response. Fig. 9 shows the proposed current loop control scheme for the outward approach. The transfer function of the inner loop is expressed by

$$G_T(s) = \frac{I_c(s)}{I_c^*(s)} = \frac{C_f s}{(s+x_3)(L_f C_f s^2 + R_f C_f s + 1) + (x_1 s + x_2) C_f s}. \tag{19}$$

By referring to (5) and (6), let us set the target polynomial of the inner loop by choosing $x_3 = 384000$, $[\alpha_1 \quad \alpha_2] = [5 \quad 10]$ and $\tau = 2.5 * 10^{-4}$.

$$\delta_i(s) = 2.4\times10^{-8}s^3 + 4.8\times10^{-3}s^2 + 5.9\times10s + 1.1\times10^6 \tag{20}$$

The control gains of the inner loop are determined from the relation between (19) and (20) as follows:

$$[x_3 \quad x_2 \quad x_1] = [384000 \quad 760946 \quad -36.88]. \tag{21}$$

Fig. 10 provides a visual of the current loop controller.

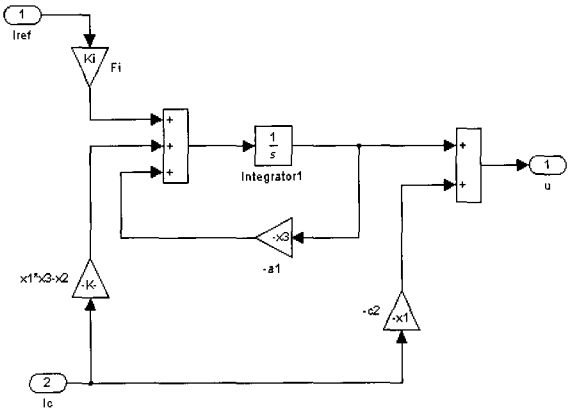

Fig. 10 Current loop controller (Outward Approach)

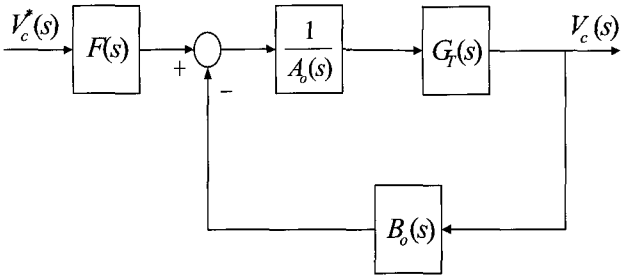

Fig. 11 Block diagram of voltage loop controller

Next, we design the controller for the outer loop that includes the transfer function of inner loop $G_T(s)$. Fig. 11 shows an IMC (Internal Model Control) controller used for robust voltage tracking. Then the overall transfer function of the outer loop is expressed by

$$\frac{V_c(s)}{V_c^*(s)} = \frac{n_o(s)}{p_o(s)} = F\frac{B_o(s)I_c(s)}{A_o(s)I_c^*(s)+B_o(s)I_c(s)} \quad (22)$$

With the given conditions for ζ and ω_n, we choose α_i, τ as

$$[\alpha_1 \quad \alpha_2 \quad \alpha_3 \quad \alpha_4]=[2.5 \quad 2 \quad 4.83 \quad 9.91], \tau = 8.333*10^{-4}. \quad (23)$$

Using (23), we set the target polynomial as

$$p_o^*(s) = 2.4*10^{-8}s^5 + 4.81*10^{-3}s^4 + 97.1*10^3 s^3 + 4.06*10^5 s^2 + 8.51*10^8 s + 7.12*10^{11} \quad (24)$$

Then the control gains of the outer loop are determined from $p_o(s)$ and $p_o^*(s)$ as follows:

$$[x_5 \quad x_4]=[78896853 \quad 900006]. \quad (25)$$

Finally, the digital controller is given by

$$C_{inner,outward}(z) = \frac{-2.34z+5.86}{z+0.78}, \quad (26)$$

$$C_{outer,outward}(z) = \frac{0.036z^3+0.037z^2-0.03z-0.04}{z^3-1.21z^2-0.56z+0.77}. \quad (27)$$

Fig. 12 shows the digital controller determined by the outward approach.

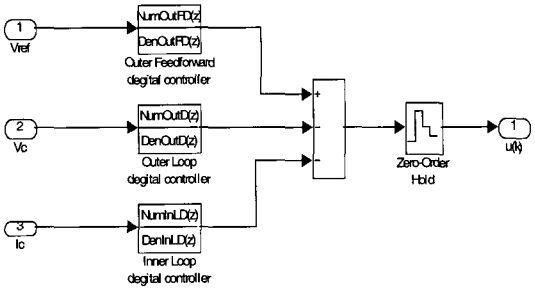

Fig. 12 Digital controller (Outward Approach)

4. Simulation Results

To evaluate the performance of the proposed controller, several simulations are carried out with Simpower System Toolbox 3.0 from Simulink®. Fig. 13 indicates the common UPS inverter system with the proposed controller. The simulations are conducted under two load conditions as follows: (1) no load, and (2) a resistive load of 10[kW].

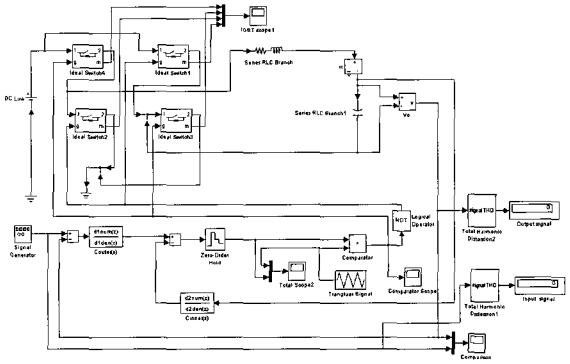

Fig. 13 UPS inverter system with proposed controller

In the Simulink block in Fig. 13, the parameters of the IGBT used are as follows:

Initial state: open, $R_{snubber} = 0.1[\Omega]$,
$R_{on} = 0.01[\Omega]$, $C_{snubber} = 0.22[\mu F]$.

Fig. 14 presents the output response of the UPS system under no load change by the inward approach. The results

show that the proposed controller gives a low steady-state error but has the phase delay effect of the output signal. The THD of the response was about 4.7%.

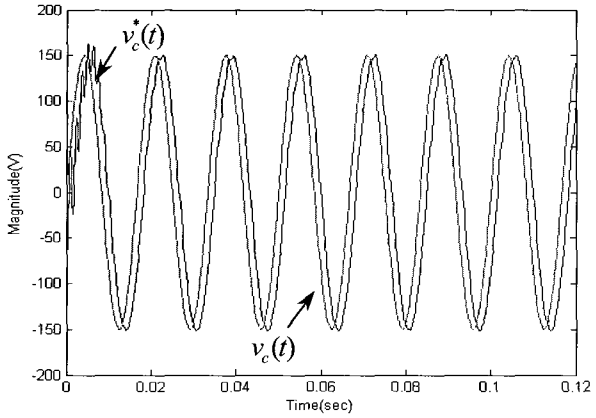

Fig. 14 Output response under no load

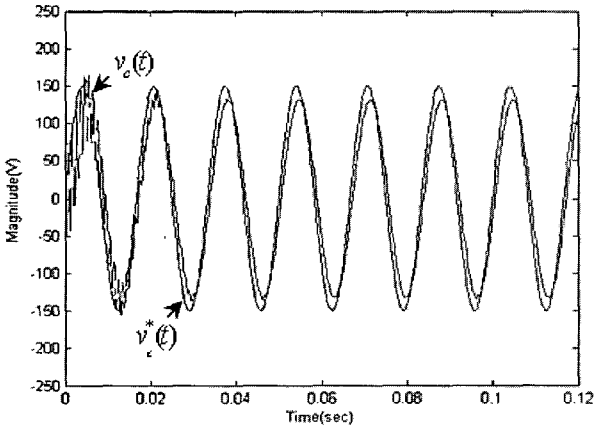

Fig. 15 Output response under no load

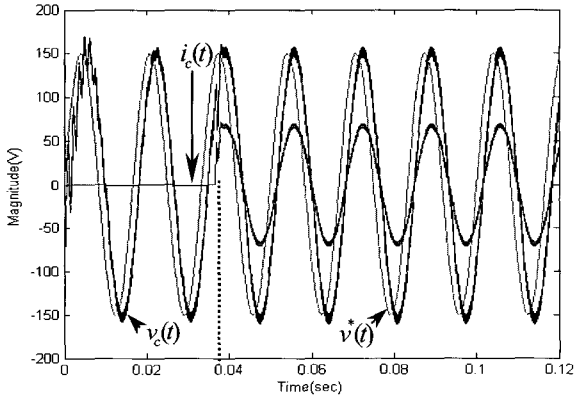

Fig. 16 Output response under a linear load change

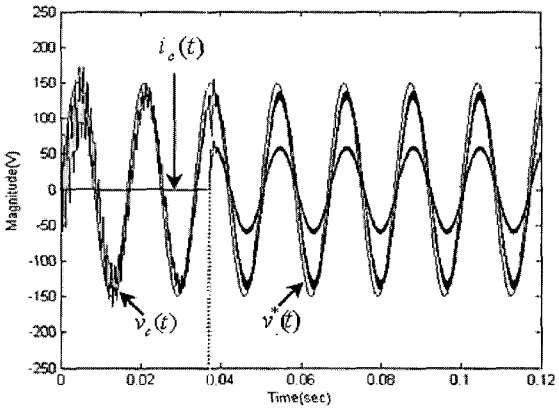

Fig. 17 Output response under a linear load change

Fig. 15 provides the output response under no load by the outward approach. The THD of the response was about 4.99%. This means that the proposed controller eliminates the phase delay effect but has a relatively high steady-state error. In both approaches, the steady-state error and phase delay effects are inversely proportional to each other.

In the second load condition, a 10[kW] resistive load is abruptly applied at the peak phase (around $t = 0.0037$ sec) to examine the size of the overshoot (occurs and how fast) and the speed of the controller response.

Fig. 16 shows the output response under a linear load change by the inward approach. In this case, the THD is about 4.4%. Fig. 17 shows the output response under a linear load change by the outward approach. The THD is approximately 4.9%. It is seen that both proposed controllers satisfy the given time response requirements and the step change has been reduced to within one and a half periods. The results in Fig. 16 and Fig. 17 signify that the output response by the inward approach has a lower overshoot than by the outward approach, but inevitably it has a poorer tracking ability.

5. Conclusions

When designing a digital controller for an UPS inverter, two different approaches are mainly applied using characteristic ratio assignment. With a fixed sampling time, the continuous controller is discretized by means of the emulation method. The proposed controllers satisfy the given time-response specifications while holding the stability of the closed-loop system. The summarized features of the proposed controllers for each approach are as follows:

The inward approach results in good system performance in terms of robustness for an on-line type UPS. The designed controller has a fast transient response and relatively small overshoot over a linear load change. Conversely, it cannot evade the phase delay and steady-

state error.

In the framework of the outward approach, the internal model control (IMC) method has been applied in the outer loop so as to better track the reference voltage. This results in a good, robust tracking performance and small steady-state error, but it has a relatively high overshoot in response to an abrupt change of loads. Therefore, this controller seems to be sensitive to disturbances.

The CRA is applied to the problem of time response requirements such as overshoot and settling time within the limitation on the speed of time response. The simulation results using Simulink® verify the performances of the proposed controller over all linear load conditions.

Acknowledgements

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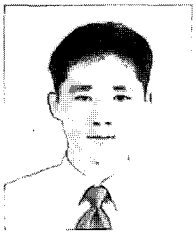

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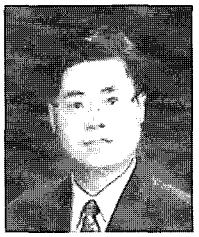

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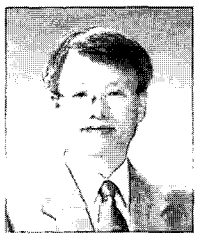

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[1] G. O. Young, "Synthetic structure of industrial plastics," in *Plastics*, 2nd ed., vol. 3, J. Peters, Ed. New York: McGraw-Hill, 1964, pp. 15–64.

[2] W.-K. Chen, *Linear Networks and Systems*. Belmont, CA: Wadsworth, 1993, pp. 123–135.

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