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Properties and SPICE modeling for a Schottky diode fabricated on the cracked GaN epitaxial layers on (111) silicon

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Abstract

The planar Schottky diodes were fabricated and modeled to probe the device applicability of the cracked GaN epitaxial layer on a (111) silicon substrate. On the unintentionally n-doped GaN grown on silicon, we deposited Ti/Al/Ni/Au as the ohmic metal and Pt as the Schottky metal. The ohmic contact achieved a minimum contact resistivity of 5.51×10^{-5} Ω· cm^2 after annealing in an N_2 ambient at 700 °C for 30 sec. The fabricated Schottky diode exhibited the barrier height of 0.7 eV and the ideality factor was 2.4, which are significantly lower than those parameters of crack free one. But in photoresponse measurement, the diode showed the peak responsivity of 0.097 A/W at 300 nm, the cutoff at 360 nm, and UV/visible rejection ratio of about 10^2. The SPICE(Simulation Program with Integrated Circuit Emphasis) simulation with a proposed model, which was composed with one Pt/GaN diode and three parasitic diodes, showed good agreement with the experiment.

Key Words : Schottky diode, photodetector, circuit model, cracked GaN, SPICE simulation

1. Introduction

Silicon is an attractive base substrate for III-nitride epitaxy, because it is possible to obtain the extensive real estate at a significantly low cost compared to the other substrate such as sapphire or SiC[1-2]. On the silicon substrate, there is thermal mismatch as well as lattice parameter mismatch, it is very hard to suppress the cracks on the overall area of the wafer perfectly by controlling the process parameters. In this sense, it is meaningful to investigate the metal-GaN contact properties on the cracked surfaces.

In this work, we studied and modeled the electrical characteristics of a Schottky diode the cracked GaN layer and fabricated the Schottky diode on the cracked GaN epitaxial layer grown on p-type (111) silicon substrate. Even though there was significant crack density in the GaN layer, we successfully fabricated a Schottky diode. We evaluate the feasibility on the usefulness of both contacts through SPICE simulation using the data from the experiment.

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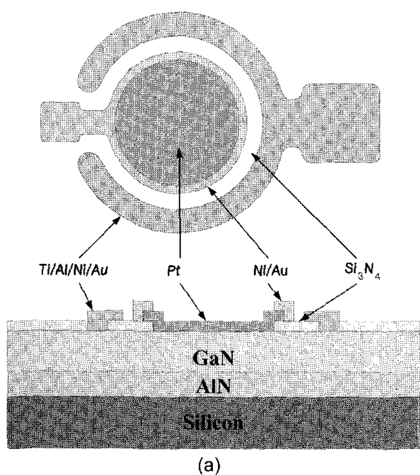
2. Experiment

We fabricated the planar type Schottky diodes[3] of circular area pattern on GaN/Si and GaN/sapphire. The diode on GaN/sapphire was used to compare the electrical characteristics and to extract the simulation parameters for an equivalent circuit modeling and SPICE simulation. In case of n-type GaN on silicon, Ti/Al/Ni/Au (350/2000/400/500 Å) layers are deposited for an ohmic metallization, and platinum (100 Å) and other metals for Schottky metallization. Both metallizations were achieved by the lift-off processes[4]. Si_3N_4 film was used for passivation between the two contacts[5]. Fig. 1 shows the fabricated device structure and process flow.

3. Result and Discussions

Fig. 2 shows the surface photomicrograph of GaN layers on silicon substrate. The unintentionally n-type conducting GaN on silicon had a significant density of cracks in the hexagonal GaN crystal directions as shown on the surface photomicrograph [Fig. 2][6]. The electron concentration of the GaN layer was 8.7×10^{18} cm^{-3} and mobility was 17 cm^2/Vs, which were roughly one order of magnitude lower than that of the GaN grown on sapphire.



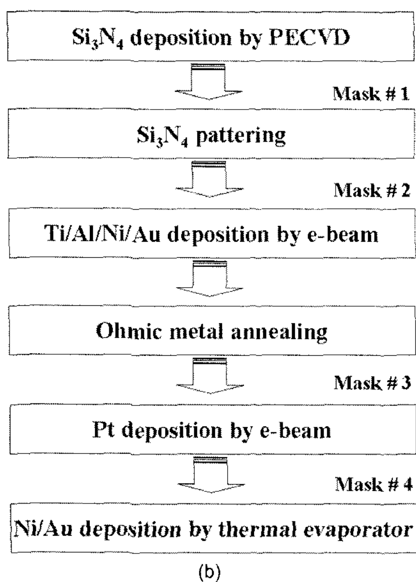


Fig. 1. (a) Schematic device structure and (b) fabrication process flow.

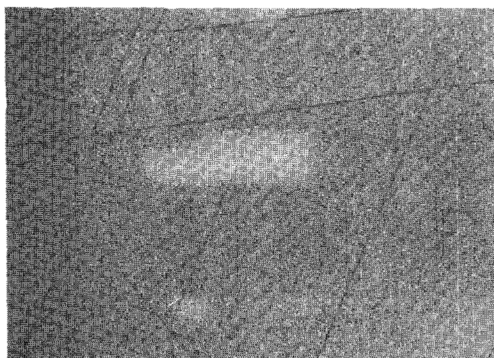


Fig. 2. Photomicrograph of the GaN layers grown on silicon.

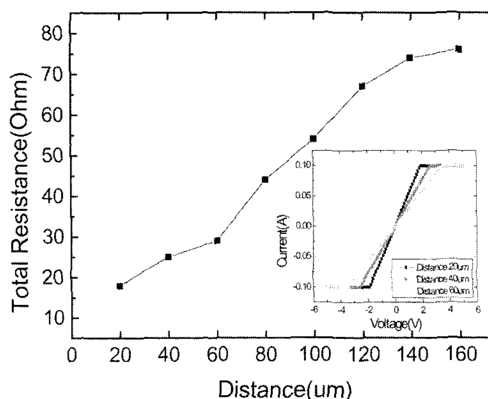


Fig. 3. Resistance versus distance plot from TLM measurement on the ohmic contact of n-type GaN/silicon.

Fig. 3(a) shows the transmission line method (TLM) measurement plot for the ohmic contacts on the n-type GaN layer on (111) silicon wafer. We used Ti/Al/Ni/Au multi-layer metals and annealed in an N_2 ambient at 700 °C for 30 sec for ohmic metallization. Inset of Fig. 3(a) is the I-V curve between two contact pads, which clearly shows ohmic properties of them. But the measured resistance data points on the plot does not exhibit ideal-linear in slope, which is thought to be caused by the random distribution of the cracks and random direction of them. The contact resistivity was as good as $5.5 \times 10^{-5}\ \Omega \cdot cm^2$ in this work.

Fig. 4(a) shows logJ-V characteristic of the fabricated Pt/Schottky diodes of different diameters on the n-type GaN grown on silicon. Fig. 4(b) shows logJ-V characteristic of Schottky diodes which were fabricated on n-type GaN on silicon and that on sapphire substrate. The one exhibit effective barrier height of around 0.75 eV and ideal factor of 2.4. The other Schottky diode showed the barrier height of 0.85 eV, which is significantly higher. The degradation of Schottky barrier properties is significant that definitely need to improve the surface morphology by more stringent growth process control. Up to now, however, it is still very challenging to obtain the completely crack-free GaN layers on silicon substrate[7].

On the other hand, Fig. 4(c) shows the spectral responsivity of the fabricated Schottky diode in the UV range. We got the cutoff wavelength of 360 nm, peak responsivity of 0.097 A/W at 300 nm, and UV/visible rejection ratio of about 10^2, which shows potential applicability to the opto-eletronic devices as well. Those electrical and photoresponse characteristics are telling

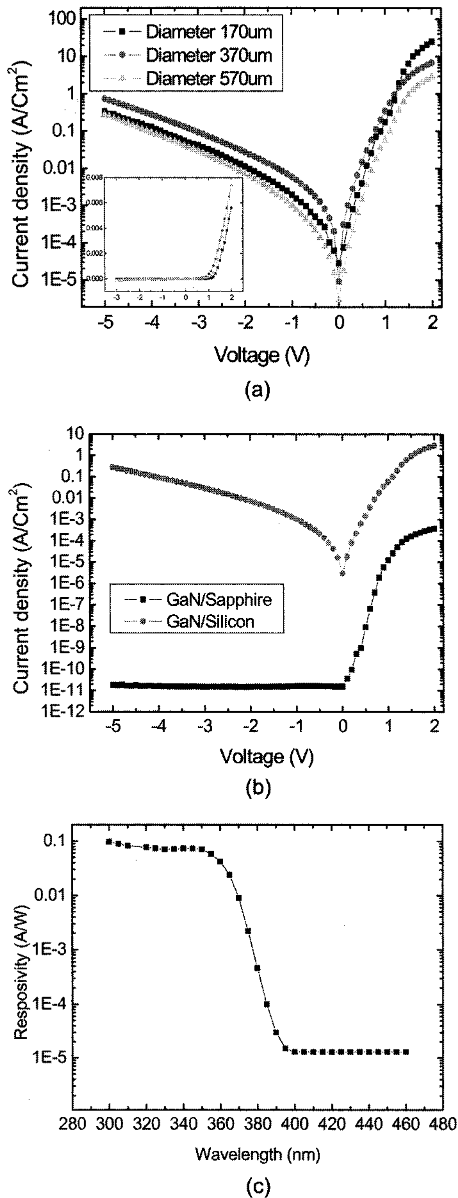


Fig. 4. logJ-V curves for Pt Schottky diodes fabricated on GaN/silicon. (a) I-V characteristics for different dimension devices, (b) A I-V comparison between Schottky diodes on the cracked GaN layer grown on silicon and crack-free GaN layer on sapphire, and (c) Spectral photo-responsivity of the Schottky diode on GaN/silicon.

us that the cracked GaN layer is not completely unacceptable for the device fabrication[8]. We need to consider how to manage the cracks for device application and also need to understand the electrical conduction mechanisms and photo-electric effects.

In the Schottky diode using the cracked GaN, the forward logJ-V characteristics do not exhibit uniform linearity either. It is thought that, because the cracks in GaN epi-layer provide the parasitic current conduction paths. And they cause the non-ideality in both forward and reverse characteristics. In the reverse I-V curve, it shows a leakage current increase according to the reverse bias. And the reverse breakdown voltage is 5~10 V above which the leakage current increases markedly.

One of the parasitic current paths is Pt/GaN side Schottky diode by platinum Schottky metal diffusion through the cracks. We expected that it worked in parallel with the intrinsic Schottky diode and caused its barrier lowing significantly.

We suggest another parasitic path, which may be modeled as a resistance and originated by the Pt contact to p-type silicon after diffusion through the cracks. Pt on p-type silicon makes ohmic contact because work function of Pt is higher than that of p-type silicon. This ohmic contact becomes leakage current path in reverse bias region. When we fabricate both ohmic and rectifying contacts on the cracked GaN, we have to select the metal combinations considering their work functions on each layer, so that we could obtain better electrical properties.

It is natural to add a circuit component to explain the diode-like, non-ideal current conduction paths due to the ohmic metal diffusion down to the silicon substrate through the cracks. The origins and circuit modeling concepts for each model components are summarized in Table 1. These elemental effects may become serious and complex as the density of the cracks on the surface becomes higher. So we tried to simulate using the contacts the circuit model incorporating the combined effects for the first time.

Fig. 5 shows a conceptual equivalent circuit to model the Schottky diode on the cracked n-type GaN on silicon substrate. We evaluated the diode current using our model based on both of the data for the cracked Schottky diode and for the crack free diodes. Adopting a SPICE model with the two parasitic diodes and applying proper parameters, we could optimize the electrical parameters of the devices. The optimized electrical characteristics for the proposed equivalent circuit components are also shown in Fig. 5. Table 1 is a summary of the optimized equivalent circuit parameters in this work. Even though it is simple approach for our first optimization, Fig. 6 exhibits a good

Table 1. Parameters and optimization result for the SPICE model

Model component	Origin	Effect	SPICE model	Barrier height [eV]	Is [A]
Crack-free Pt/GaN diode	Crack free Pt/GaN Schottky diode	intrinsic diode	data	0.8663	6.3×10^{-12}
Cracked Pt/GaN diode	Pt diffusion through the crack	parallel diode	data	0.6436	5.7×10^{-8}
Pt/Si series resistance	Pt diffusion through crack	leakage current path	resistor	-	-
Ti/Al/Ni/Au/Si diode	Ohmic metal diffusion through crack	reverse diode	M-S diode	0.7466	3.6×10^{-8}
GaN/Si diode	p-n junction with GaN and silicon	reverse diode	hetero-junction diode	-	1.7×10^{-8}

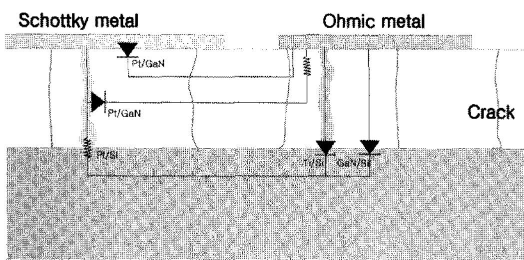


Fig. 5. Parallel conduction paths in the Schottky diode on the cracked GaN layer.

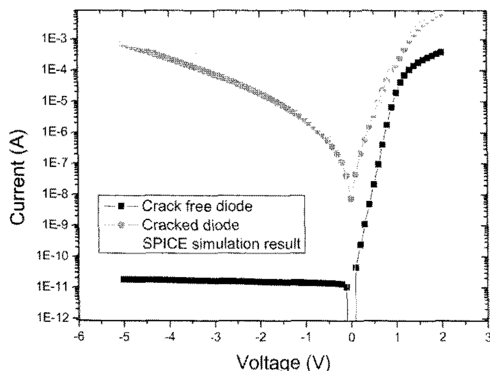


Fig. 6. LogJ Vs V comparison between SPICE simulation result using the circuit model and the experimental data for the diodes.

agreement between the SPICE simulation and the experimental data of the cracked n-type Pt/GaN diode.

4. Conclusion

The planar Schottky diodes were fabricated and modeled to probe the applicability of the cracked GaN epitaxial layer on a (111) silicon substrate. The fabricated Schottky diode exhibited the barrier height of 0.7 eV and the ideal factor of 2.4, which is significantly poorer than those parameters of crack free one. The ohmic contact achieved a contact resistivity of $5.51 \times 10^{-5}\ \Omega \cdot cm^2$ after annealing in an N_2 ambient at 700 °C for 30 sec. But in photoresponse measurement, the same diode showed the peak responsivity of 0.097 A/W at 300 nm and the cutoff at 360 nm with UV/visible rejection ratio was about 10^2. The SPICE simulation with a composite diodes model, composed of non-ideal Pt/GaN diode and three parasitic diodes, showed good agreement with the experiment.

In conclusion, even though there was significant crack density in the n-type GaN layer on silicon, we achieved rectifying contact and ohmic contact and successfully fabricated a Schottky diode which showed quite promising electrical properties. We evaluate the cracked diode through SPICE simulation using the data from the experiment. When we fabricate the opto-electronic devices on the cracked GaN, we may expect the better electrical properties by appropriate selection of the metal combinations considering their work functions. The result gives a positive signal to apply the cracked GaN layer on silicon substrate to the HFET's (Hetero structure Field Effect Transistor) and integration of the electronic devices.

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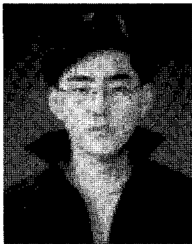

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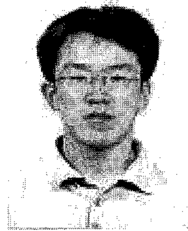

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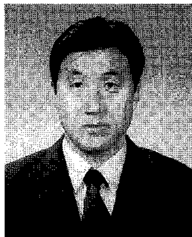

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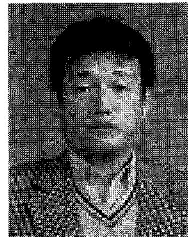

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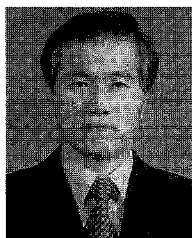

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