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# Single-Balanced Low IF Resistive FET Mixer for the DBF Receiver

Jee-Won Ko · Kyeong-Sik Min

## Abstract

This paper describes characteristics of the single-balanced low IF resistive FET mixer for the digital beam forming(DBF) receiver. This DBF receiver based on the direct conversion method is designed with Low IF I and Q channel. A radio frequency(RF), a local oscillator(LO) and an intermediate frequency(IF) considered in this research are 1950 MHz, 1940 MHz and 10 MHz, respectively. Super low noise HJ FET of NE3210S01 is considered in design. The measured results of the proposed mixer are observed IF output power of −22.8 dBm without spurious signal at 10 MHz, conversion loss of −12.8 dB, isolation characteristics of −20 dB below, 1 dB gain compression point(P1dB) of −3.9 dBm, input third order intercept point(IIP3) of 20 dBm, output third order intercept point(OIP3) of 4 dBm and dynamic range of 30 dBm. The proposed mixer has 1.0 dB higher IIP3 than previously published single-balanced resistive and GaAs FET mixers, and has 3.0 dB higher IIP3 and 4.3 dB higher P1dB than CMOS mixers. This mixer was fabricated on 0.7874 mm thick microstrip substrate( $\varepsilon_r$=2.5) and the total size is 123.1 mm× 107.6 mm.

***Key words*** : DBF, Receiver, FET, Single-Balanced Mixer, Resistive Mixer.

## Ⅰ. Introduction

Wireless mobile communication technologies have greatly progressed in recent years. This DBF receiver based on the direct conversion method is generally suitable for high-speed wireless mobile communications. In general, super-heterodyne receiver is widely used for wireless communications. This method has low noise characteristics and excellent stability, but circuit size due to multi-IF ports is large and complex. On the other hand, direct conversion receiver offers significant reduction of circuit complexity due to the elimination of IF circuitry, including IF filters and IF mixers[1]. One of the significant problems of this receiver architecture is DC offset. DC offset is mainly caused by self-mixing in the mixer circuit. In order to solve this problem, the low IF receiver is used. In this architecture, the received signal is converted to the low IF signal. Since the desired signal does not have DC components, the DC offset problem can be solved. The resistive FET mixer, due to its simple biasing requirements, is well suited for direct conversion applications. The resistive FET mixer only requires negative gate bias, with the LO applied to the gate, RF applied to the drain, and IF signal filtered from the drain[2]. Because there is no drain bias, problems regarding the separation of the baseband signal and DC bias voltage are eliminated. The single-balanced FET mixer generally has advantages, such as the better power-handling capabilities, rejection of spurious responses, reduction of external filters and improvement of isolation characteristics[3].

In this paper, we design and fabricate the simple mixer for the DBF receiver using the single-balanced low IF resistive FET mixer. Also, we present calculation and measurement results of single-balanced low IF resistive FET mixer using the microwave office(MWO) as RF design tool[4].

Table 1 tabulates the performance comparison between the previous published mixers and our proposed mixer[5]~[16]. In Table 1, the proposed mixer has higher IIP3 than previously published whole mixers, and has higher P1dB than CMOS mixers.

## Ⅱ. Design and Fabrication of the Single-Balanced Low IF Resistive FET Mixer

Fig. 1 shows the block diagram of DBF receiver and mixer specifications are summarized in Table 2. This mixer as shown in Fig. 1 is composed of band pass filter, a low pass filter, a DC bias circuit and FET[17]. It is also called as the direct conversion RF mixer. The received RF signal is directly converted to the baseband

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Table 1. The comparison between the previous published mixers and our proposed mixer.

| | Conversion Loss [dB] | P1dB [dBm] | IIP3 [dBm] |
|---|---|---|---|
| J. H. Kim et al.[5] | - 12.8 | N/A | 8.3 |
| D. A. Kruger[6] | - 10.0 | N/A | 19.0 |
| F. Ellinger et al.[7] | - 7.4 | 4.0 | 13.0 |
| S. H. Lee et al.[8] | - 10.5 | 10.5 | 18.0 |
| M. Nakayama et al.[9] | 10.0 | N/A | - 1.0 |
| C. C. Tang et al.[10] | 6.7 | - 18.0 | - 7.5 |
| A. N. Karanicolas[11] | 8.8 | - 16.1 | - 4.1 |
| S. Lee et al.[12] | - 0.8 | N/A | - 0.6 |
| P. J. Sullivan et al.[13] | 0.5 | - 15.0 | - 6.0 |
| H. Kilicaslan et al.[14] | 3.5 | - 8.2 | 2.2 |
| M. Lehne et al.[15] | 6.4 | N/A | 17.0 |
| P. J. Sullivan et al.[16] | 0 | - 10.0 | 2.0 |
| This Work | - 12.8 | - 3.9 | 20.0 |

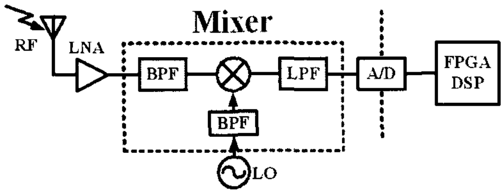


Fig. 1. Block diagram of DBF receiver.

Table 2. Specifications of mixer.

| Parameters | Specifications |
|---|---|
| RF Frequency | 1,950 MHz |
| LO Frequency | 1,940 MHz |
| IF Frequency | 10 MHz |
| Conversion Loss | < - 12 dB |
| P1dB | > - 4 dBm |
| IIP3 | > 20 dBm |
| OIP3 | > 4 dBm |
| Isolation | < - 20 dB |

signal, put into the LPF, and then the A/D converter. The converted digital signal is demodulated in the digital signal processor(DSP) or field programmable gate arrays(FPGA).

Fig. 2 shows a design model of the single-balanced low IF resistive FET mixer. Super low noise HJ FET of NE3210S01 is considered in design. The signals of RF and LO are supplied in phase to the drains and out of phase to the gates of FET, through the wilkinson power divider and hairpin band pass filter by using microstrip line, respectively. In order to achieve the quadrature phase relationship of I and Q channel, the LO signal is split by wilkinson power divider with a 90° delay line on one branch. The IF signal of 10 MHz is extracted from the drain by using lumped element low pass filter. In order to obtain phase information at IF output, the single-balanced low IF resistive FET mixer is considered to obtain the received signal into I and Q signals by using a quadrature hybrid, generally implemented by analog circuits. In design, the RF, the LO frequency and the IF are corresponding to 1,950 MHz, 1,940 MHz and 10 MHz, respectively. A bias voltage applied bias circuit is - 0.4 V.

Fig. 3 shows a photograph of the fabricated single-balanced low IF resistive FET mixer constructed on microstrip substrate with thickness of 0.7874 mm and $\varepsilon_r$ equals to 2.5. The DC bias is applied for open stub with 1/4 wavelength radial circuit. The total size of the fabricated single-balance low IF resistive FET mixer is 123.1 mm × 107.6 mm.

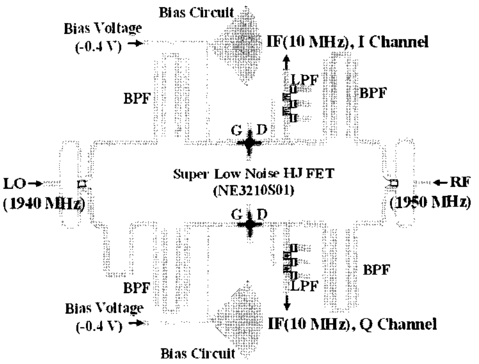


Fig. 2. Design model of the single-balanced low IF resistive FET mixer.

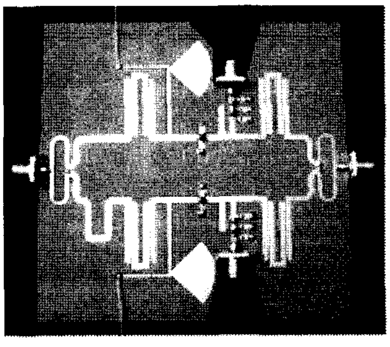


Fig. 3. Photograph of the fabricated single-balanced low IF resistive FET mixer.

## Ⅲ. Measurement of the Single-Balanced Low IF Resistive FET Mixer

Fig. 4 shows the IF spectrum of the fabricated single-balanced low IF resistive FET mixer. When the RF input power, the LO input power and $V_{GS}$ voltage are impressed −10 dBm, 6 dBm and −0.4 V, respectively, the calculated and measured IF output power at 10 MHz are observed −19.2 dBm and −22.8 dBm, respectively. Even though a little difference between the calculated and measured results due to the loss of the transmission line and the error of fabrication is existent, these values show reasonable result. As mentioned before, the single-balanced low IF FET mixer generally has advantage, such as the rejection of spurious signals. In Fig. 4, we confirmed that the proposed mixer rejects the harmonic component appeared at 20 MHz[18].

The calculated and measured IF output power of the single-balanced low IF resistive FET mixer at 10 MHz are shown in Fig. 5(a)~(c).

Fig. 5(a) shows variation of the calculated and measured IF output power versus RF input power of the single-balanced low IF resistive FET mixer. When the LO input power and $V_{GS}$ voltage are 6 dBm and −0.4 V, respectively, the RF input power is varied from −70 to 20 dBm. The IF output power with respect to the RF input power shows the linear characteristics. It is dependant on variation of the RF input power.

Fig. 5(b) and (c) show results of IF output power versus LO input power and $V_{GS}$ of the proposed mixer, respectively. In Fig. 5(b), when the RF input power and $V_{GS}$ are constant −10 dBm and −0.4 V, respectively, the LO input power is varied from −70 to 20 dBm. In Fig. 5(c), when the RF input power and LO input power are −10 dBm and 6 dBm, respectively, the $V_{GS}$ is varied from −1.2 to 0 V. Variation of the IF output power level is almost dependent upon RF and LO input power variation than one of $V_{GS}$. For example, when the RF input power, LO input power and $V_{GS}$ are −10 dBm, 6 dBm and −0.4 V, respectively, the measured IF output power of I channel is −22.8 dBm. The measured IF power is observed a good agreement with the calculated one.

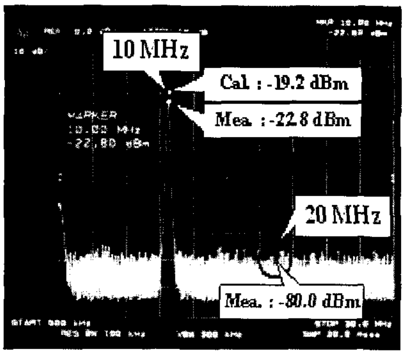
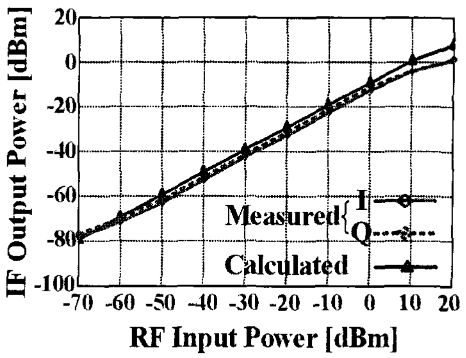
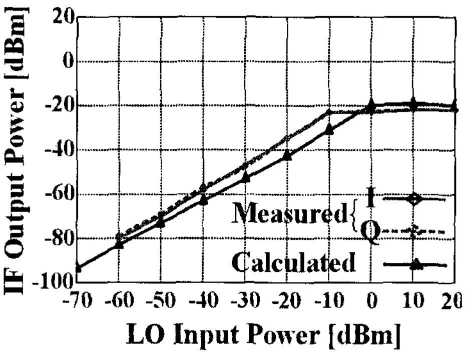


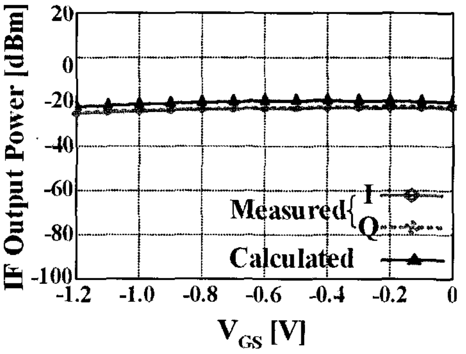
Fig. 4. IF spectrum of the single-balanced low IF resistive FET mixer.



(a) IF output power versus RF input power



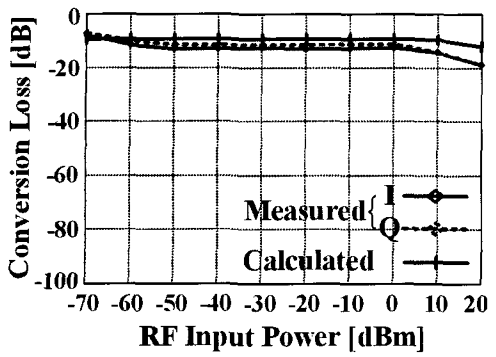
(b) IF output power versus LO input power



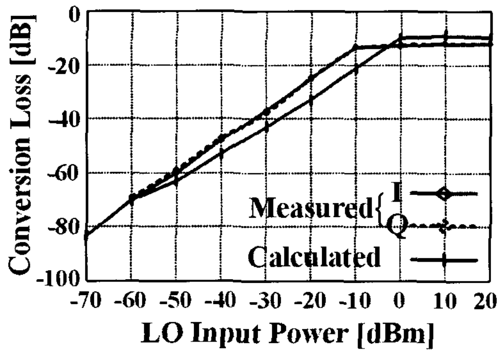
(c) IF output power versus $V_{GS}$

Fig. 5. Calculated and measured IF output power of the single-balanced low IF resistive FET mixer.

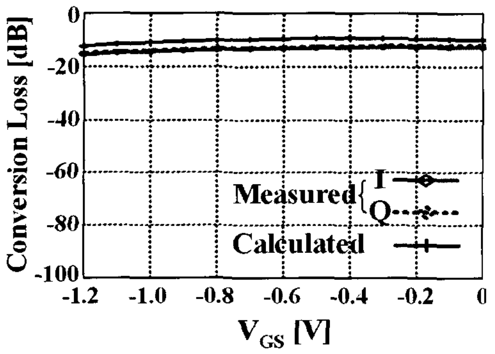
Fig. 6(a)~(c) show the calculated and measured conversion loss versus RF input power, LO input power and $V_{GS}$, respectively. In Fig. 6(a)~(c), the calculated



(a) Conversion loss versus RF input power



(b) Conversion loss versus LO input power



(c) Conversion loss versus $V_{GS}$

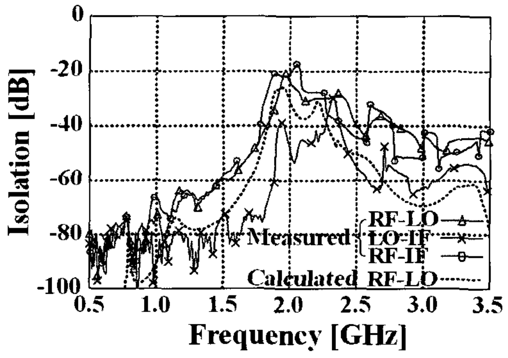
Fig. 6. Calculated and measured conversion loss of the single-balanced low IF resistive FET mixer.

and measured data show a similar trend with respect to the RF input power, LO input power and $V_{GS}$, respectively. When the RF input power, LO input power and $V_{GS}$ are set to $-10$ dBm, 6 dBm and $-0.4$ V, respectively, the measured conversion loss of I channel is $-12.8$ dB. As shown in Fig. 5 and 6, the measured results of I and Q channels show almost same characteristics.

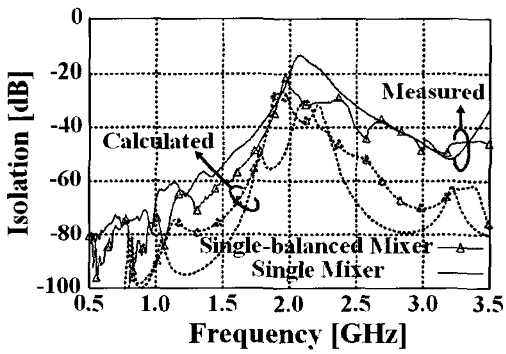
The calculated and measured isolation results of the proposed mixer, and the RF-to-LO isolation results of the single-balanced and single resistive FET mixer are shown in Fig. 7(a) and (b), respectively. In Fig. 7(a), the measured isolation characteristics of RF-to-LO, LO-to-IF and RF-to-IF at from 0.5 to 3.5 GHz band show $-20$ dB below and a good agreement with the calculated one. In Fig. 7(b), the measured RF-to-LO isolation characteristic of the single resistive FET mixer is $-13$ dB below. Therefore, the measured RF-to-LO isolation characteristic of the single-balanced resistive FET mixer is lower than one of the single resistive FET mixer.

Fig. 8(a) and (b) show the measured results of P1dB and two-tone characteristics of the third order intermodulation(IM3), respectively. When the LO input power is 6 dBm and bias voltage is $-0.4$ V, the measured P1dB is $-3.9$ dBm, IIP3 is 20 dBm and OIP3 is 4 dBm.

Fig. 9 shows a photograph of the fabricated single-balanced low IF resistive FET mixer with calibration circuit. Generally, the amplitude and phase characteistics of IQ waveforms have a little difference from each other. To solve the problems, we used the

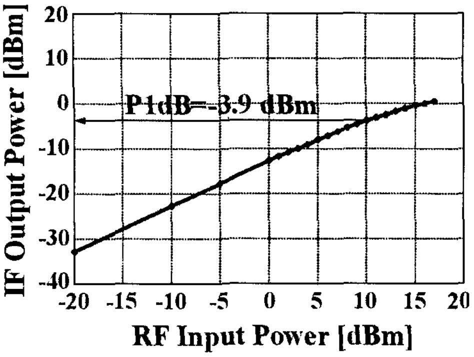


(a) Single-balanced resistive FET mixer

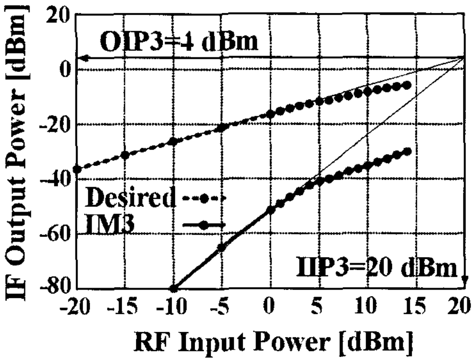


(b) Single-balanced and single resistive FET mixer

Fig. 7. Calculated and measured isolation results of the single-balanced and single resistive FET mixer.



(a) P1dB



(b) Two-tone characteristics

Fig. 8. Measured results of P1dB and two-tone characteristics of IM3.

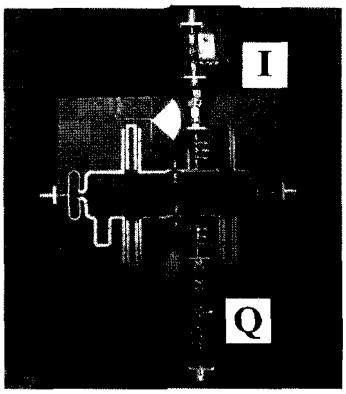
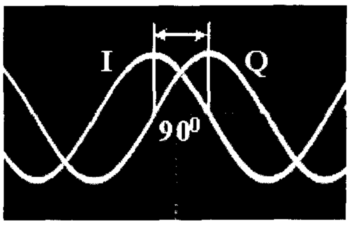
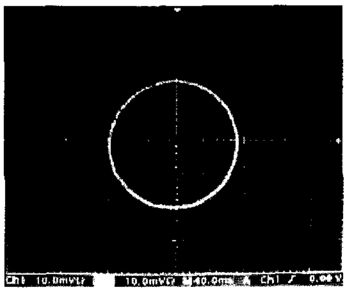


Fig. 9. Photograph of the fabricated single-balanced low IF resistive FET mixer with calibration circuit.



(a) IF waveforms



(b) Constellation

Fig. 10. IF waveforms and constellation of I and Q channel at 10 MHz.

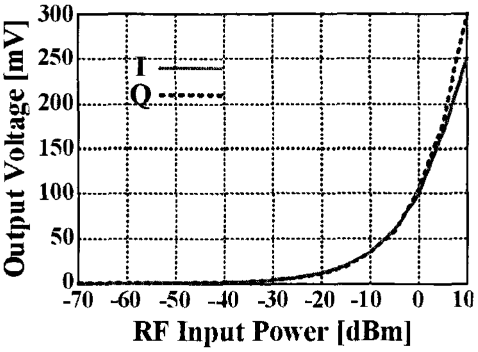


Fig. 11. Measured output voltages versus RF input power of the single-balanced low IF resistive FET mixer.

calibration circuit and the 90 degrees delay line on one branch(quadrature phase shifter).

Fig. 10(a) and (b) show the measured IF waveforms and constellation of I and Q channel at 10 MHz, respectively, when the RF input power, the LO input power and $V_{GS}$ voltage are constant $-10$ dBm, 6 dBm and $-0.4$ V, respectively. The information of I and Q channel should be obtained through the low pass filter at the drain sides. It is observed same amplitude and quadrature phase difference between two channels at an IF frequency of 10 MHz.

Fig. 11 shows variation of the measured output voltages versus RF input power of the proposed mixer. When the RF input power is varied from $-70$ to 10 dBm, the measured output voltages of I and Q channel varied from 0 to 300 mV. In from $-70$ to $-30$ dBm and from 0 to 10 dBm of RF input power, constellations show a spread and distortion characteristics, respectively. In from $-30$ to 0 dBm, we obtained constellations of accurate IF waveform without spread and distortion characteristics.

## Ⅳ. Conclusion

This paper presents characteristics of the single-balanced low IF resistive FET mixer. When the RF input power, the LO input power and $V_{GS}$ voltage are −10 dBm, 6 dBm and −0.4 V, respectively, the measured IF output power and conversion loss at 10 MHz are −22.8 dBm and −12.8 dBm without spurious signal, respectively. The proposed mixer is observed broadband isolation characteristics of −20 dB below, P1dB of −3.9 dBm, IIP3 of 20 dBm, OIP3 of 4 dBm and dynamic range of 30 dBm. As mentioned before, the proposed mixer has 1.0 dB higher IIP3 than previously published single-balanced resistive and GaAs FET mixers, and has 3.0 dB higher IIP3 and 4.3 dB higher P1dB than CMOS mixers. The use of this approach will surely contribute to design for the direct conversion mixer and the development of DBF receiver.

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