A 9-bit ADC with a Wide-Range Sample-and-Hold Amplifier

Jinup Lim*, Youngjoo Cho, and Joongho Choi

Abstract—**In this paper, a 9-bit analog-to-digital converter (ADC) is designed for optical disk drive (ODD) servo applications. In the ADC, the circuit technique to increase the operating range of the sample-and-hold amplifier is proposed, which can process the wide-varying input common-mode range. The algorithmic ADC structure is chosen so that the area can be significantly reduced, which is suitable for SoC integration. The ADC is fabricated in a 0.18-μm CMOS 1P5M technology. Measurement results of the ADC show that SNDR is 51.5dB for the sampling rate of 6.5MS/s. The power dissipation is 36.3mW for a single supply voltage of 3.3V.**

Index Terms —**Analog-to-Digital Converter, Sample-and-Hold Amplifier, Wide-Operating Range.**

I. INTRODUCTION

As the amount of data to be processed has been continuously increased, the optical disk drive (ODD) should be one of the most important storage devices in the computing system. For the recent ODD systems, frequent bidirectional data transfer through read/write operations are performed in contrast to the previous ones in which data are usually read for archival information retrieving. In addition, various types of storage media can be processed with a single unit, which requires multiple channels and data-rate operations for the ODD systems. As the data rate has been significantly increased, the servo data processing block also should fast operate as well as RF data processing block.

Performance of the high data-rate servo data processing block depends mostly on the specifications of data converters because control algorithms and their implementation are based upon the resolution and conversion rate of data converters. In this paper, the 9-bit algorithmic data converter is designed and fabricated in a 0.18-μm CMOS technology. In the algorithmic ADC, simple hardware resources are required since the desired resolution can be achieved by identical iterations. This helps to reduce the size of the designed ADC, which is suitable for integration in SoC (System-on-Chip) implementation of the servo application chip. Since the main system clock is much higher than the data conversion rate, the clock needed for this algorithmic ADC operation is easily available.

Since the servo data input show large variation in terms of the signal swing and common-mode input range, wide operating range of the sample-and-hold amplifier (SHA) is a critical specification for designing ADC. In this paper, the circuit technique is proposed to increase the operating range of the SHA that consists of the fully-differential operational amplifier.

II. ADC STRUCTURE

The block diagram of the 9-bit algorithmic ADC is shown in Fig. 1(a), which mainly consists of the sample-and-hold amplifier (SHA), multiplying digital-to-analog converter (MDAC), flash analog-to-digital converter (FADC), analog bias/reference block and digital clock/control block. In order to satisfy the given

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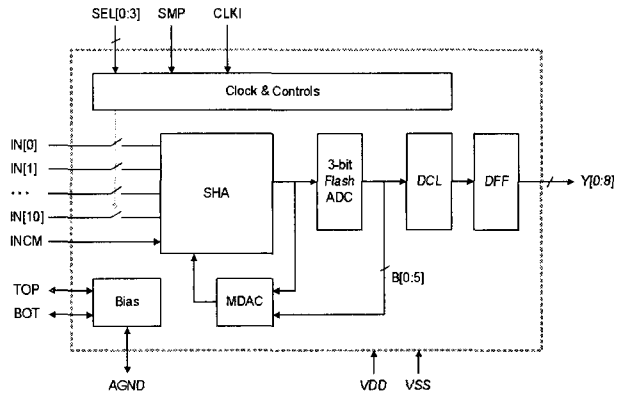
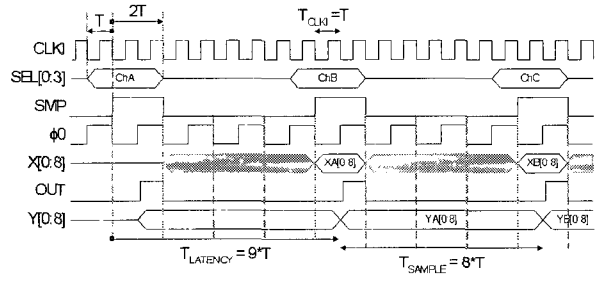
resolution specifications, several iterations through this MDAC-FADC path are performed. With the reduced number of bits in this internal data converter path, more iteration is needed, which implies that each block should run at a higher clock frequency.

By considering the trade-off between the hardware complexity (IP hardware area) and operating clock frequency (power consumption), both the resolutions of the internal MDAC and FADC are determined to be 3 bits in our design. Four iterations provide 9-bit conversion resolution with a 3-bit redundancy for digital error correction that overcomes the problem due to inaccuracy of the internal data conversion blocks.

As shown in Fig. 1(b), the operation is divided into 4 cycles, where a new analog input is applied to the SHA for every first cycle. Then during the next 3 cycles, the residues resulting from each ADC-DAC operation are processed and the corresponding intermediate digital outputs are produced. These digital outputs are combined in the error correction logic and the output strobe signal is activated for the final output at the data rate that is four times smaller than the main clock frequency.



(a)



(b)

(a) Block diagram (b) Operation

Fig. 1. 9-bit algorithmic ADC.

III. Circuit Design

1. Sample-and-Hold Amplifier (SHA)

Fig. 2 shows the block diagram of the conventional SHA using the fully-differential operational amplifier. When the Φ_1 is on (Fig. 2(b)), the input and offset voltage of the operational amplifier are sampled on the capacitor C and the desired output is available during Φ_2 (Fig. 2(c)). In Fig. 2(b) and (c), the common-mode levels of the input and output signals are also shown for the respective clock phases. In the cases when the input common-mode range (V_{INC}) is widely varied, the input common-mode level (V_{ICM}) of the operational amplifier should be changed accordingly since the output common-mode level (V_{OCM}) of the operational amplifier is set to be constant with the help of the common-mode feedback circuit in the operational amplifier as shown in Fig. 2(b) and (c). When the Φ_1 is on, the charges stored at C_1 and C_2 can be expressed as follows,

$$Q_1 = C_1(V_{IP} - V_{OCM1}) \quad (1.a)$$

$$Q_2 = C_2(V_{IM} - V_{OCM1}) \quad (1.b)$$

When the Φ_2 is on, they can be expressed as follows,

$$Q_1 = C_1(V_{OM} - V_{ICM2}) \quad (2.a)$$

$$Q_2 = C_2(V_{OP} - V_{ICM2}) \quad (2.b)$$

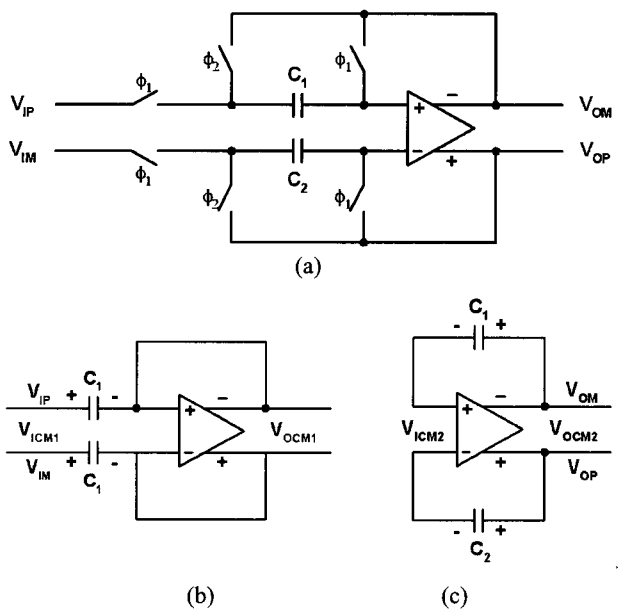
Therefore, the input common-mode level of the operational amplifier can be obtained as,

$$V_{ICM2} = V_{OCM2} + V_{OCM1} - V_{ICM1} \quad (3)$$

As known from (3), widely-changing input levels for servo applications, for example, results in large variation of the input common-mode level of the operational amplifier.

The fully-differential operational amplifier shown in Fig. 3 includes a pair of differential amplifiers which consist of nMOS and pMOS transistors, respectively. Two differential pairs are used to process the rail-to-rail input common-mode range. In Fig. 3, when the input common-mode range becomes close to GND, the nMOS differential pair turns off. This makes the bias currents of M_8 and M_9 to be reduced from $2xI_B$ to I_B. On the other hand, when the input common-mode range increases, the pMOS differential amplifier turns off and the corresponding bias currents of M_8 and M_9 become $3xI_B$. This bias current is controlled by the common-mode

feedback (CMFB) circuit consisting of M_{21}~M_{25}. Thus, the reduced (increased) amount of currents in these transistors implies that the output common-mode level goes up (down) with the CMFB loop. When the gain of CMFB is set to be lower for stability, the deviation of the output common-mode level results in the penalty in terms of the output voltage swing.



(a) Block diagram (b) Operation at ϕ_1 (c) Operation at ϕ_2

Fig. 2. Sample-and-hold amplifier.

Fig. 4 shows the proposed circuit technique to overcome this problem so that the output common-mode level can be kept to be constant independent of the input common-mode range. The circuit consisting of M_{30}~M_{31} and M_{36}~M_{37} detect the decreased and increased input common-mode ranges, respectively. When the input common-mode level decreases, the control current of M_{34} and M_{35} are also reduced, which makes the tail bias current of the CMFB differential amplifier through the current mirror of M_{28} and M_{29}. This reduction of current can help to reduce the bias current of M_8 and M_9 so that the output common-mode level can be unchanged. When the input common-mode level increases, the opposite situation occurs. In Fig. 5, there are the simulation results of the operational amplifier. Fig. 5(a) shows the output common-mode level is plotted with respect to the input common-mode level. In the case when the proposed circuit is used(dotted line), the output common-mode level is shown to be quite constant throughout the rail-to-tail input range compared with the conventional amplifier (solid line). Fig. 5(b) shows the transient simulation results where the input common-mode level is near to supply voltage. As like DC simulation result, the output common-mode level with the proposed CMFB is quite more constant than that with conventional CMFB.

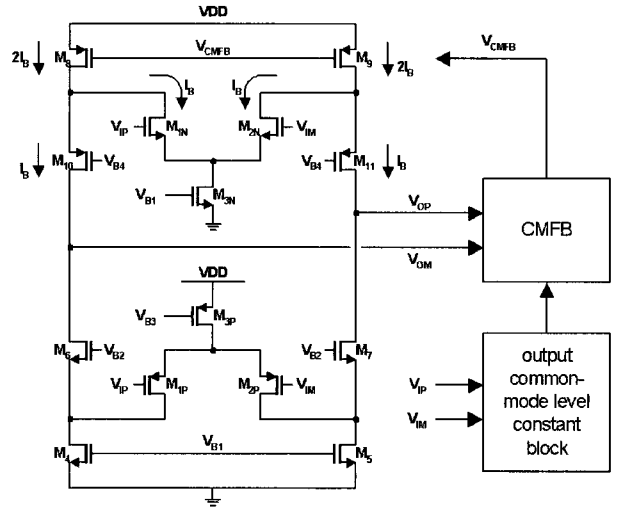


Fig. 3. Operational amplifier

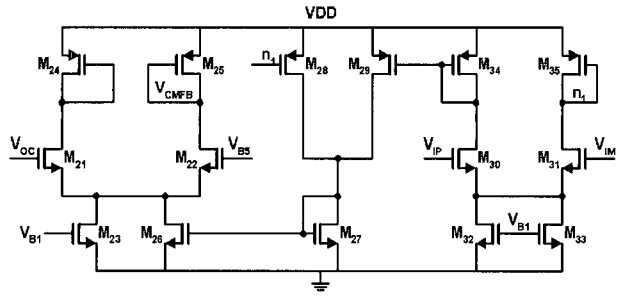
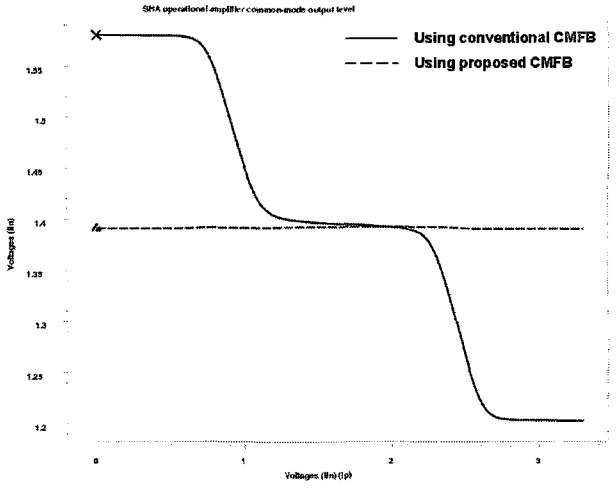


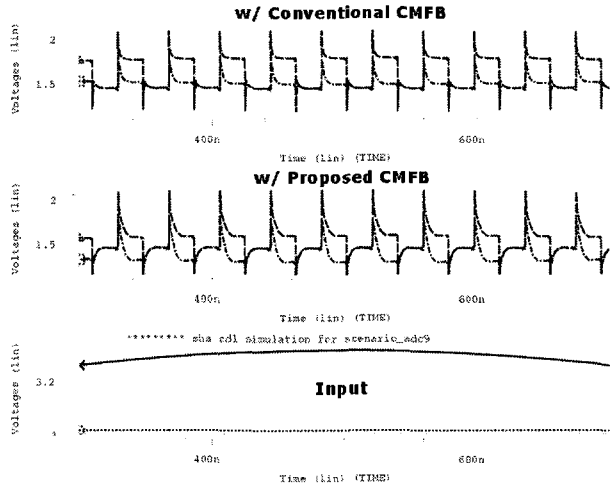
Fig. 4. The proposed circuit to keep the output common-mode level constant.

2. Multiplying Digital-to-Analog Converter (MDAC)

The circuit schematic of the multiplying digital-to-analog converter (MDAC) is shown in Fig. 6, where the fully-differential switched-capacitor amplifier is used for residue multiplication. When the ϕ_2 is high, the MDAC operates in sample mode and samples the input signal throughout all capacitors. For the next half cycle of ϕ_1, it amplifies the sampled signal to produce the proper residue operations. According to 6bit thermometer code, the MDAC input references are selected whether TOP or BOT and the dynamic range is doubled by the difference between TOP and BOT.



(a) DC simulation



(b) Transient simulation

Fig. 5. Simulation results of the operational amplifier.

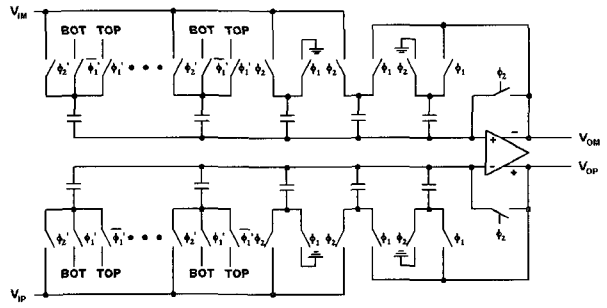


Fig. 6. Block diagram of MDAC.

3. Flash Analog-to-Digital Converter (FADC)

The flash-type analog-to-digital converter(FADC) consists of 6-level resistor array, 6-level comparator array for RSD code processing and digital control logic including thermometer-to-binary decoder and digital error correction (DCL) block.. The block diagram of this FADC is shown in Fig. 7. Each comparator consists of the pre-amplifier and latch so that offset-voltage compensation and fast decision operations can be achieved.

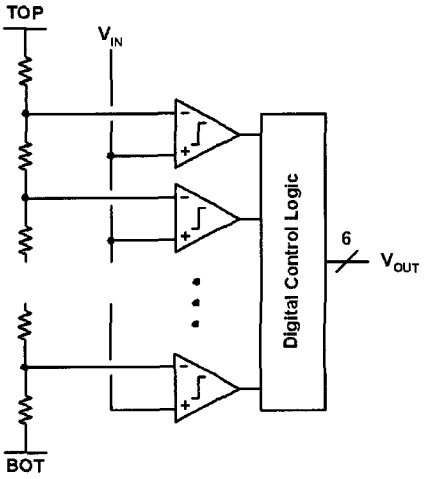
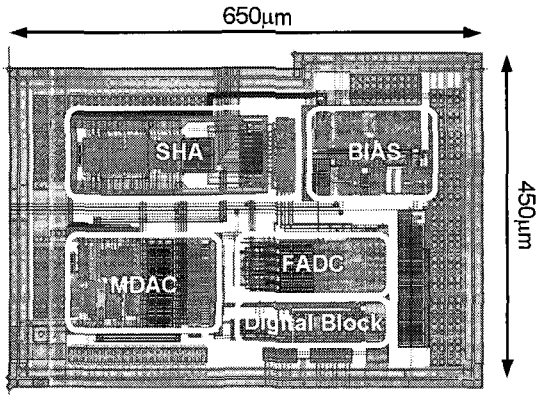


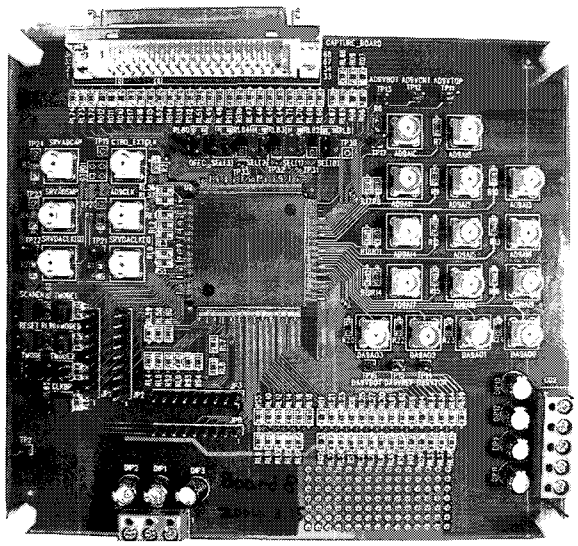
Fig. 7. Block diagram of FADC.

4. Implementation

The designed 9-bit algorithmic ADC is fabricated in a 0.18-μm CMOS 1P5M technology with a thick gate-oxide option. The layout and test PCB are shown in Fig. 8. The active area of the designed ADC is 650 x 450μm^2. Fig. 9 shows measured FFT spectrum of ADC. The converter achieves SNDR of 51.5dB and ENOB of 8.26bit at a input frequency of 100kHz and a sampling rate of 6.5MS/s. Measured INL and DNL are ±0.75 and ±0.6 LSB, respectively. The power consumption is 36.3mW for a supply voltage of 3.3V. Table 1 summarizes the measurement results of the 9-bit algorithmic ADC.



(a)



(b)

Fig. 8. Layout and test PCB of the 9-bit ADC

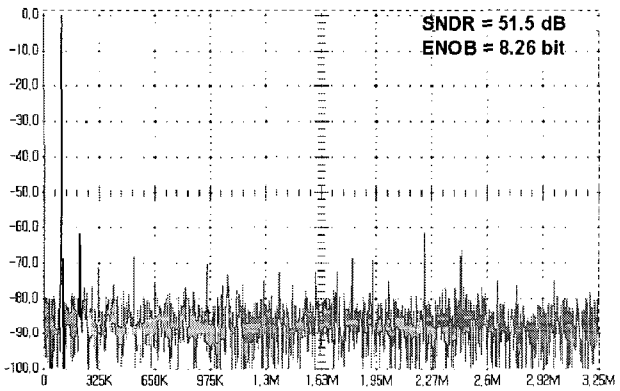


Fig. 9. Measured FFT spectrum for a 100kHz input

Table 1. Measurement Summary

Specifications	Results
Structure	9-bit Algorithmic
SNDR	51.5 dB
ENOB	8.26 bit
INL	< ± 0.75 LSB
DNL	< ± 0.6 LSB
Technology	0.18-μm CMOS 1P5M
Sampling Rate	6.5 MS/s
Power Supply	3.3 V
Power Dissipation	36.3 mW

IV. Conclusion

In this paper, the operational amplifier with the improved common-mode feedback is proposed. It can be utilized for implementing the wide operating range sample-and-hold amplifier. The 9-bit ADC based upon this approach is designed for ODD servo applications.

Acknowledgment

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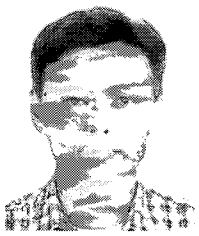

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