

Accuracy of Current Delivery System in Current Source Data-Driver IC for AM-OLED

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Abstract—Current delivery system, in which the analog current produced by a unique DAC circuit is stored into a current-memory circuit and delivered in a time-divided sequence, shows variation of output current as low as 4% in a current source data-driver IC for AM-OLED driven by a current-programmed method without any fuse repairing after fabrication. This driver IC has 54 outputs and can sink constant current as low as 3 μA with 6-bit analog levels. Such a low current level without variation can hardly be obtained by an ordinary MOS transistor because the current level is in the sub-threshold region and changes exponentially with threshold voltage variation. Thus we adopted a current mirror circuit composed of bipolar transistors to supply well-controlled current within a nano-ampere range.

Index Terms—AM-OLED, current-programmed pixel circuit, data-driver, current sink, analog current delivery system, BiCMOS

I. INTRODUCTION

Organic Light Emitting Diode (OLED) displays have now become one of the most promising candidates for next generation displays due to its excellent properties such as thin thickness, wide viewing angle, and high contrast in dark environments [1,2]. Passive Matrix (PM) driven panels have already entered the marketplace, but its panel size is restricted to a few inches in diagonal due to a limitation in the number of

scanning lines. Therefore, currently, the research of active matrix (AM) driving is pursued more actively than that of PM driving, in order to achieve a large-sized and high-resolution full color OLED panel.

However, AM driving of OLED displays has a serious problem with respect to luminance uniformity. The back-plane of an AM-OLED display is fabricated using an amorphous silicon (a-Si) or low-temperature poly-silicon (LTPS) process. The threshold voltage of an a-Si TFT easily shifts by several volts due to bias-temperature stress (BTS), which causes a sticking image. On the other hand, LTPS TFTs have a very large fluctuation of both mobility and threshold voltage, thus resulting in luminance non-uniformity. Therefore the compensation circuit or driving method is an integral part of both types of TFT processes.

Current programmed driving is the one of the most effective methods to compensate both threshold voltage and mobility variations [3]. The current level through the OLED in a pixel is set directly by the current from the data-driver and not by the voltage in this driving method. Therefore a constant current source/sink data-driver is needed.

A constant current source driver has already been developed for use as a column driver for PM-OLED displays. However, such a circuit has not been available for use as the data-driver of current programmed AM-OLED displays because the current level of the AM-OLED driver is required to be about a hundredth of PM-OLED current level. In other words, the maximum current required for an AM-OLED data-driver is just several micro-amperes, compared to several hundred micro-amperes for a PM-OLED data-driver. In addition, in order to obtain a half-tone level of 6-bits, the minimum current level we must control can be as low as 10 nA.

II. DIFFICULTY OF SMALL CURRENT

Figure 1 shows the transfer characteristics of a typical n-channel MOSFET, as a function of the W/L ratio, when a drain voltage of 5 V is applied. The dimension of W/L=1 is already a small value, but the current is still too large to control the current within the sub-micro ampere range. This is because the current range is located in the subthreshold region, which is very sensitive to threshold voltage variation. Hence we must use transistors with a W/L ratio as small as 0.01 to operate in the saturation region. Since the channel width is also restricted by design rules, the channel length must be enlarged instead of shortening the channel width to obtain the W/L ratio of 0.01. A transistor with such an irregular dimension is neither reliable nor practical. Thus, it can be concluded that the MOSFET is not suitable to produce current less than 1 μ A.

Bipolar transistors are usually used when dealing with large currents. However, even for small currents, it is useful because the transistor size is decreased and it operates in the regular range. In this work a BiCMOS process is employed to generate small current for AM-OLED drivers in a novel manner.

Figure 2 shows the basic block diagram of the driver developed in this work. The diagram is composed of only 4 blocks, the digital-to-analog converter (DAC), shift register, current latch and current mirror. The two

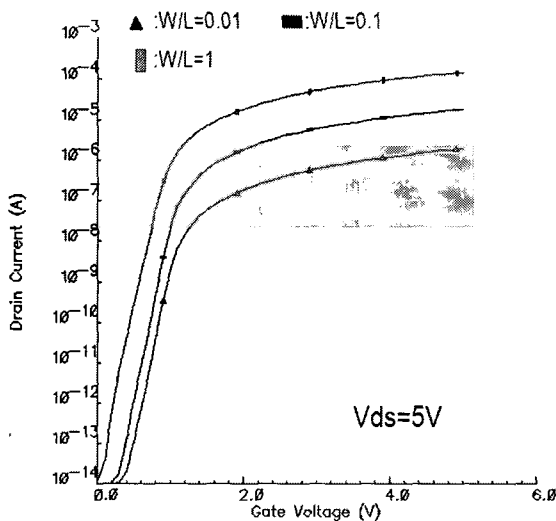


Fig. 1. Typical MOS transfer characteristics

III. PRINCIPLE DIAGRAM

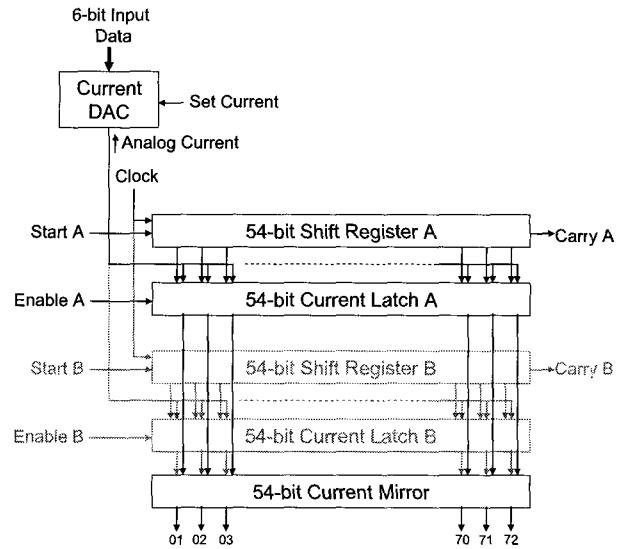


Fig. 2. Block diagram of current source data-driver for AM-OLED.

sets of shift registers and current latch blocks are used to provide continuous output, which is achieved by switching the read and write states of the two sets alternately.

The DAC block converts the 6-bit input data to the 64-level analog current, which is latched sequentially to the current memory circuit in the current latch block specified by the shift register. The analog current delivery system has the following two advantages: First, to eliminate the variation of DAC characteristics. In general a driver has the same number of DAC circuits as that of the output, so the variation of the DAC characteristics directly results in the variation of outputs. However, since only one DAC circuit exists in our system, this variation does not occur. The second advantage is to save a chip area by reducing the number of DAC circuits required.

1. Current DAC

Figure 3 shows the current DAC circuit, which provides analog current with 6-bit levels in sink mode. The input S can set the full-scale current level from the 4 μ A to 45 μ A at the outputs by a constant voltage. The pnp bipolar transistors, Q1 to Q6, and the resistors, R1 to R6, are designed to provide current with the ratio of

1:2:4:8:32:64. Therefore switching the p-channel MOSFETs by using the inputs, D1 to D6, can provide 6-bit analog current from output terminal, Y.

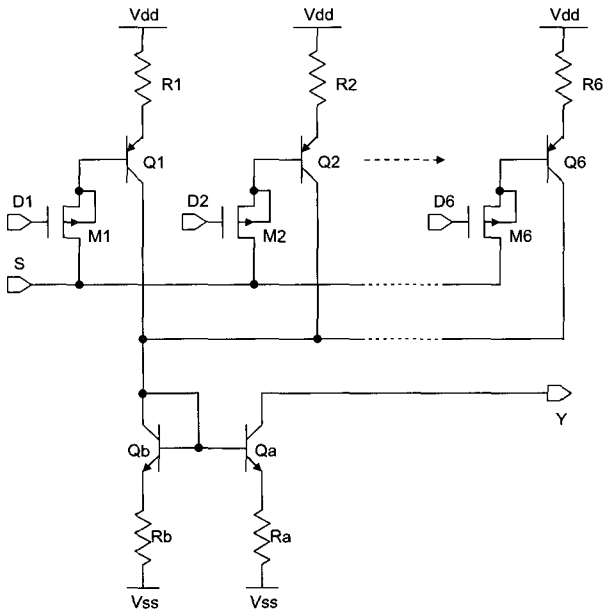


Fig. 3. Current DAC circuit

2. Current latch

The current latch block is composed of 54 current memory circuits as shown in Fig.4. The current memory circuit can store the analog current level when the write signal from the shift register is input and can output the same analog current in parallel by using the enable signal. The current memory circuit is shown in Fig.5. The terminals S, E, A, and Y correspond to the write enable signal, the enable input, the current input, and the current output signals in Fig.4, respectively. During the writing state the transistors M1 and M2 are ON and M4 is OFF, and the current at terminal A flows through M2 and M3 from Vdd. The gate voltage of M3 is automatically set to follow the writing current because of the constant current source from the current DAC circuit and the stored charge across storage capacitance C1. On the other hand, during the read state, M1 and M2 are OFF and M4 is ON, thus the current flows through the M3 and M4 to terminal Y. Since the gate voltage of M3 is stored in C1, the same current during writing period is maintained. This principle is almost the same as that of the pixel circuit used for current programmed AM-OLED. Since this circuit can store the input

current value in memory and can output the same current value when desired, we call it a “current memory” circuit.

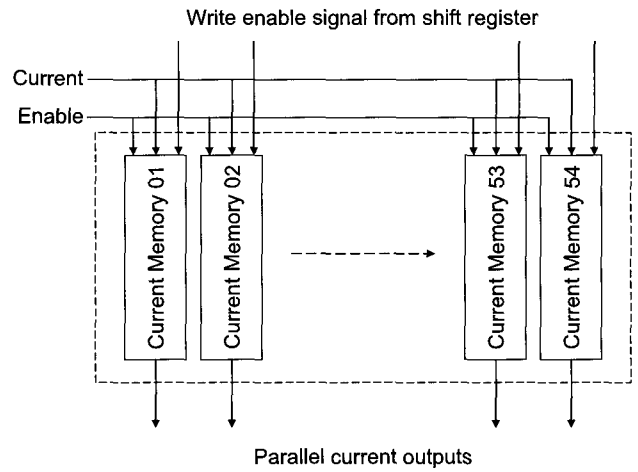


Fig. 4. Block diagram of the current latch

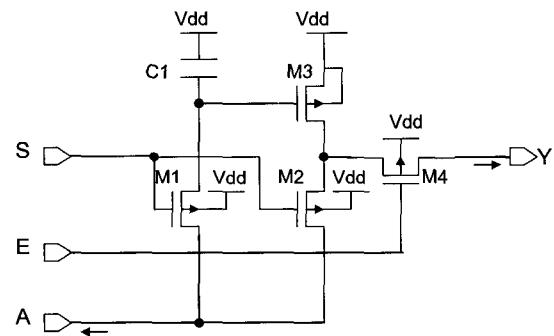


Fig. 5. Current programmed circuit

There are two factors that account for the deviation between the input and output current values. The first is the imperfection of the saturation characteristics of M3. If non-saturation characteristics exist on M3, the output current may increase because the source-drain voltage of M3 increases during reading periods compared with that of the writing period. Good saturation characteristics are also needed to provide constant output current, which is independent of the load conditions. The second factor is the feedthrough voltage that occurs when the charge from the gate capacitance of M3 is reduced due to leakage through the parasitic capacitances of M1 and M2 when the voltage of S swings. This can be reduced by increasing C1 but this would also result in the increase of chip area and a longer writing time.

The writing speed of the current memory is

determined by the capacitance on the input line, which includes the parasitic capacitance as well as the storage capacitance, and the input current level. Basically the writing time is decided by C_{line}/I_{input} . Therefore the number of outputs is restricted by the select time divided by the writing time. To get a large number of outputs we must either use a large input current or decrease the capacitance. However, this is not feasible since the input current is dictated by the output current level and the capacitance cannot be decreased indefinitely. Thus, the best way to achieve a fast writing time is to employ a current mirror circuit, which can decrease the output current down to the level required for the current programmed AM-OLED panel.

3. Current mirror

Figure 6 shows the current mirror circuit. As mentioned before the circuit consists of bipolar transistors to provide a small current. We successfully reduced the current by the factor of 10. In the current mirror circuit, the current ratio is decided not only by the ratio of resistances, $R1/R2$ but also by the ratio of transistor dimensions. In general the variation of resistance is much larger than that of transistor characteristics, so we designed the circuit where the current ratio is predominantly decided by the transistor dimensions. It was confirmed that the resulting ten-fold decrease in current in the current mirror circuit made the writing time sufficiently short to deliver the current from DAC to the 54 current memory circuits within 10 μ sec.

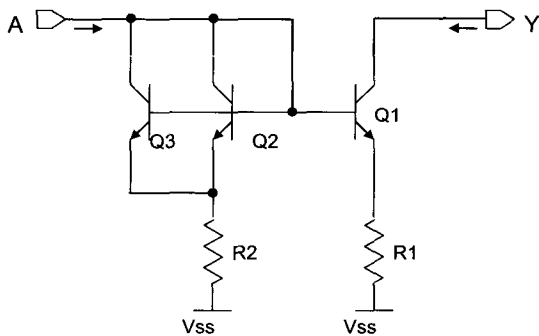


Fig. 6. Current mirror circuit

IV. CHIP LAYOUT

Figure 7 shows a picture of the chip layout. The chip

was fabricated using the BiCMOS process of Chartered Semiconductor Manufacturing Ltd. The chip size was 3.7 mm \times 3.1 mm. Only the chip edge area with a width of 1 mm was used for the driver circuit and the area in the center was used for the TEG circuit. Therefore this circuit design can make the chip very compact if we use the common long rectangular driver configuration.

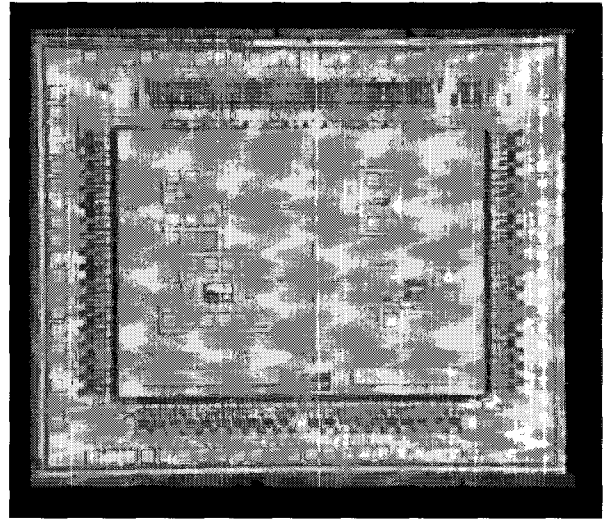


Fig. 7. Chip layout

V. OUTPUT CHARACTERISTICS

Figure 8 shows the output current waveform when sequentially decreasing digital data bit by bit were input. The rectangle waveform is the highest bit of input data for the timing reference. The linearly decreasing waveform shows the correct operation of the driver. Slight deviations from the triangular shape can be attributed to the DAC circuit error and since all the output waveforms show the same deviation, it can be concluded that the current delivery system works correctly.

Figure 9 shows the variation of the output currents. The horizontal axis shows the output number and the vertical axis shows the average current increase per one level. There exist many methods that can be used to evaluate the variation of the output. We adopted the percentage of the difference between the maximum and minimum values per the standard value. This value was evaluated to be 4 %, which does not satisfy the requirements of panel image quality, since ideally, only 1 % variation is

allowed. However, this value is very respectable in comparison with other drivers, especially with the drivers that provide such a small current.

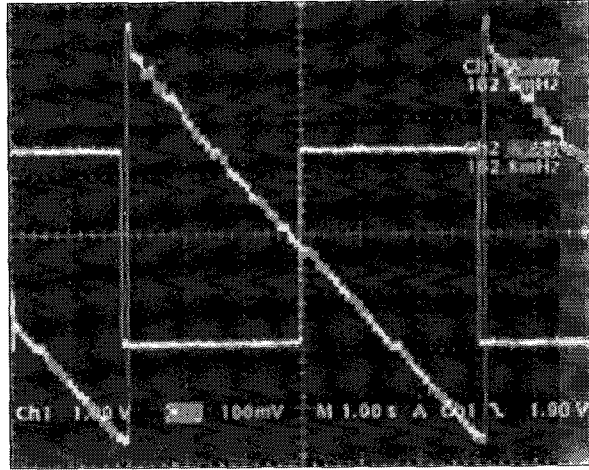


Fig. 8. Output waveform

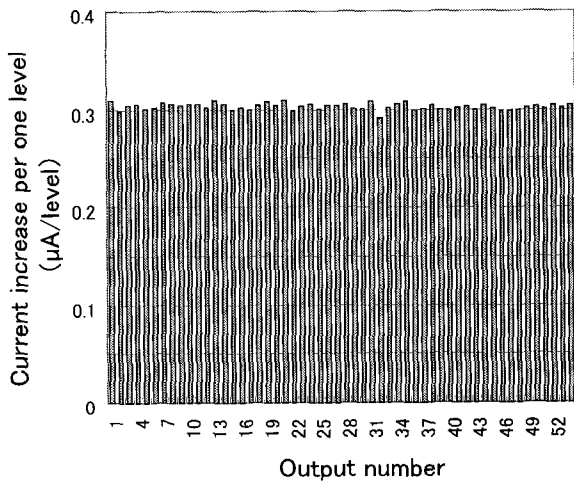


Fig. 9. Variation output current

VI. WRITING SPEED IN CURRENT MEMORY

In this section the writing speed of current memory will be discussed to evaluate how many current sources can be output from a unique DAC in current delivery system. Figure 10 shows the equivalent circuit of current memory during a writing period. The capacitance in the figure represents the capacitances including the gate-capacitance of MOS transistor, C_{gate} , the storage capacitance in current memory circuit, C_s , and the parasitic capacitance fixed on the line from DAC circuit, C_{line} . The current, I_{data} is supplied from the DAC as a

constant current.

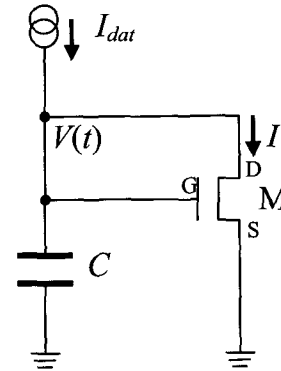


Fig. 10. Equivalent circuit of current memory during a writing period.

This circuit gives the following differential equations:

$$C \frac{dV(t)}{dt} = -\frac{\beta}{2} V(t)^2 + I_{data} \quad (1)$$

$$\begin{cases} \beta = C_{in} \mu_e \frac{W}{L} \\ C = C_{line} + C_s + C_g \\ V_{th} = 0 \end{cases} \quad (2)$$

where C_{in} gate insulator capacitance, μ_e mobility, V_{th} threshold voltage and β the coefficient showing the current drivability. Solving this differential equation, we get the following equations;

$$V(t) = V_\infty \left(\frac{V_\infty \tanh \frac{t}{\tau} + V_0}{V_\infty + V_0 \tanh \frac{t}{\tau}} \right) \quad (3)$$

$$\begin{cases} V_{(0)} = V_0 \\ V_{(\infty)} = V_\infty = 2\sqrt{I_{data}}/\beta \end{cases} \quad (4)$$

$$\tau = \frac{C}{\sqrt{\beta I_{data}}/2}, \quad (5)$$

where we can treat τ as a time constant showing the writing speed. The equation (5) indicates that smaller capacitance, larger current drivability and larger input current make the writing speed higher. Assuming the C_{in} , μ_e , and W/L to be 100 nF/cm², 800 cm²/Vs and 1, respectively, we get 80 $\mu\text{A}/\text{V}^2$ for β . Using this value and assuming I_{data} and C to be 10/64 μA and, respectively, we obtain 0.4 μsec for τ . The current value

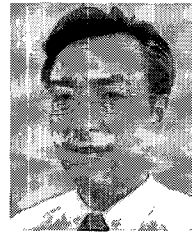
of $10/64 \mu\text{A}$ corresponds to the minimum current from the DAC circuit when the 6 bit analog current with $10 \mu\text{A}$ full scale is applied. Therefore 87 current memory circuits can be written during the selecting time for VGA is $35 \mu\text{sec}$. The 1 pF of C is never an underestimated value, so that this number proof that this driver can work correctly in 18.4 MHz clock, which is needed to use in VGA, 60 Hz refreshing rate.

VII. CONCLUSIONS

We have developed a current sink type data-driver IC with 54 outputs, 64-gray levels, and a 3 to $45 \mu\text{A}$ controllable full current range. The novel aspects of this driver are the analog current delivery system and the bipolar transistor current mirror circuit. The variation of output current among the outputs was evaluated to be 4 %, which is a sufficiently good value in drivers providing such a small current range.

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