Optimization of Gate Stack MOSFETs with Quantization Effects

Tina Mangla*, Amit Sehgal*, Manoj Saxena, Subhasis Haldar***, Mridula Gupta*, and R. S. Gupta***

Abstract—**In this paper, an analytical model accounting for the quantum effects in MOSFETs has been developed to study the behaviour of high-*k* dielectrics and to calculate the threshold voltage of the device considering two dielectrics gate stack. The effect of variation in gate stack thickness and permittivity on surface potential, inversion layer charge density, threshold voltage, and I_D-V_D characteristics have also been studied. This work aims at presenting a relation between the physical gate dielectric thickness, dielectric constant and substrate doping concentration to achieve targeted threshold voltage, together with minimizing the effect of gate tunneling current. The results so obtained are compared with the available simulated data and the other models available in the literature and show good agreement.**

Index Terms—**Quantization effects (QEs), Triangular Potential Well (TPW), Gate stack, Equivalent oxide thickness (EOT)**

I. INTRODUCTION

The continued growth of silicon-based VLSI technology over time has led to orders of magnitude of improvement in performance, device density and cost. The successful scaling of MOSFETs toward shorter channel lengths requires thinner gate oxides and higher doping levels in order to achieve high drive currents and minimized short-channel effects [1-2]. Currently, for MOSFET applications, traditional SiO_2 gate oxide is quickly approaching its physical scaling limit due to severe direct tunnelling leakage and poor reliability [3]. To overcome these problems, it is necessary that a suitable alternative gate oxide be developed having similar properties and could act as a replacement to traditional SiO_2. Some studies have shown that the gate tunnelling current is significantly reduced with the use of the high-*k*#gate dielectrics even though the barrier height decreases with the increase of gate dielectric constant [4-5]. Much effort is currently underway on alternative high-*k* gate dielectrics such as Ta_2O_5, TiO_2, ZrO_2, HfO_2, and $HfSi_xO_y$ [6-10]. However, most of the work so far has been mainly concentrated on material issues such as achieving a stable interface with silicon as well as the gate contact material. Very few detailed analysis of the effect of high-*k* dielectrics on sub-micron MOSFET performance has so far been undertaken [11], but analytical modeling is still lacking.

For these state-of-the art devices, it was demonstrated a long time ago, that as the gate oxide thickness is scaled down to 10nm and below, it can result in very large transverse electric fields (of the order of 10^7 -10^8 V/m) at the Si-SiO_2 interface leading to significant bending of the energy bands at the Si-SiO_2 interface. With that sufficient band bending, the potential well can become sufficiently narrow to quantize the motion of inversion layer carriers in the direction perpendicular to the interface and the electrons confined in the narrow potential well of an inversion layer would not behave classically [12-14]. This gives rise to a splitting of the

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once continuous energy bands into discrete bands (2-D Density of states), such that the lowest of the allowed energy levels for electrons does not coincide with the bottom of the conduction band, and a shifting of the charge centroid away from the Si-SiO_2 interface occurs [15-16]. Since then quantization effects (QEs) have significant influence on threshold voltage [14, 17], gate capacitance attenuation [18], current driving capability and transconductance degradation [19-20]. Extensive investigations on this issue have been carried out with both experiments and numerical calculations [21-23].

As QEs comes into picture, it is necessary to obtain self-consistent results of coupled Schrödinger's and Poisson's equations to estimate quantum inversion space charge density [13, 24]. The troublesome, fully self-consistent treatment [25, 26, 30] of the system accounts for the quantum-mechanical aspects of the MOS physics. But involves demanding numerical effort and the results, once obtained, are hard to transfer to different experimental situations, due to implicit and complex interrelation of the results to the input parameters. So, it is important to develop simple and convenient model to predict QEs on MOSFET characteristics [16, 21].

We have assumed the triangular-potential well (TPW) approximation as shown in Fig. 1; a simplest approximation, so that Schrödinger equation has an analytical solution [21, 22, 26] which is a good approximation when the device is in strong inversion.

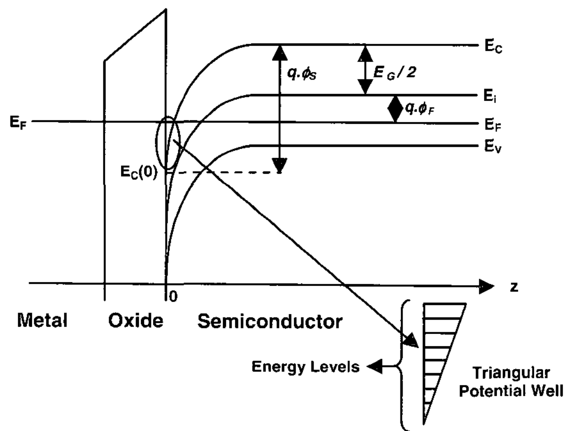

Fig. 1. Energy band diagram of an n-channel MOS transistor in strong inversion. Splitting of energy levels is shown in Triangular Potential well Approximation (TPW). Energy levels E_{ij} are measured with respect to conduction band edge ($Ec(0)$).

Using this TPW approximation, the formulation of charge density is extended to develop a surface potential based model accounting for QEs using Fermi-Dirac statistics in order to offer a suitable basis for MOSFET modeling. The model can be applied to analyze QEs on inversion layer carrier density (N_{Inv}) as well as on surface potential (ϕ_S). Using the analytical model, the effect of variation in gate stack (using high-*k* dielectric) thickness and permittivity on surface potential, inversion layer charge density, threshold voltage, and drain current; with the extension into saturation regime along with the variation of substrate doping and oxide thickness are studied. We have studied the impact of high-*k* dielectric using the different dielectric structured MOSFETs shown in Fig. 2. The results so obtained are compared with the available simulated data and the other models available in literature and show good agreement.

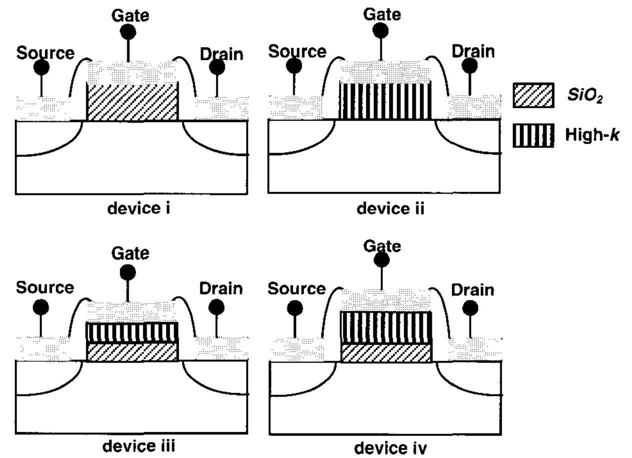

Fig. 2. Various MOSFET device structures used for analysis. ***device i***: conventional SiO_2 with oxide thickness of 1.5nm. ***device ii***: high-*k* gate dielectric (*k*=10) with thickness 1.5nm ***device iii:*** Gate Stack structure with upper dielectric (*k*=10) and lower dielectric SiO_2 (*k*=3.9) physical thickness of both layers 0.75nm. ***device iv:*** Gate Stack structure same as device iii but with an equivalent oxide thickness (EOT) of 0.75nm SiO_2 for upper dielectric.

II. Quantum Inversion Space Charge Density

In the effective mass approximation, if the Bloch waves are constrained to travel parallel to the interface, the three-dimensional Schrödinger's equation can be decoupled into a one-dimensional Schrödinger's equation. The envelope function normal to the interface (z

direction) is $\xi_{ij}(z)$ for i^{th} valley and j^{th} subband and satisfies Schrödinger's equation

$$\frac{d^2\xi_{ij}(z)}{dz^2}+\frac{2\cdot m_{zi}}{\hbar^2}\cdot\left[E_{ij}+q\cdot\phi(z)\right]\cdot\xi_{ij}(z)=0 \quad (1)$$

where m_{zi} is the effective mass perpendicular to the surface, E_{ij} is the energy state of ith valley (the lower and the higher) and j^{th} subband (j = 1,2,...), q is the electronic charge, $\hbar$ is the reduced Planck constant and $\phi(z)$ is the electrostatic potential representing the band bending at oxide-semiconductor surface satisfying the Poisson equation

$$\frac{d^2\phi(z)}{dz^2}=-\frac{\rho(z)}{\varepsilon_{Si}} \quad (2)$$

where ε_{Si} is the silicon permittivity and $\rho(z)$ is total space charge concentration given by

$$\rho(z)=q\cdot\left[N_D^+-N_A^-+p(z)-n(z)\right] \quad (3)$$

in which N_D^+ and N_A^- are the concentrations of the ionized donors and acceptors, respectively, $p(z)$ is the density of holes and $n(z)$ is the density of electrons. Although in the classical calculation, electron density is given as the Boltzmann distribution, while in the quantum mechanical model, it can be expressed in terms of wave functions and energy levels determined by solving Schrödinger's equation. Summing the electron density of all the sub-bands, $n(z)$ is given as [26]

$$n(z)=\sum_{i,j}N_{ij}\cdot\left|\xi_{ij}(z)\right|^2=\left(\frac{k_B\cdot T}{\pi\cdot\hbar^2}\right)\cdot\sum_i n_{vi}\cdot m_{di}\sum_j \ln\left[1+\exp\left(\frac{E_F-E_{ij}}{k_B\cdot T}\right)\right]\cdot\left|\xi_{ij}(z)^2\right| \quad (4)$$

where n_{vi} is the degeneracy of the energy subbands, m_{di} is the density-of-states mass per valley, k_B is the Boltzmann's constant, T is the temperature, E_F is the Fermi energy and N_{ij} is the induced 2-D inversion sheet electron density for the jth sub band from the ith valley. The values of m_{zi}, n_{vi}, and m_{di} are the same as those used by Stern [26] for a <100> surface and are given in *Table-I.*

III. Surface Potential Based Model

The set of equations given in the section II can be solved by the various numerical techniques, but it is complicated by the mutual dependence and the implicit coupling of the charge and potential distributions via the Poisson and Schrödinger equations. Also it is very time consuming. And from circuit simulation point of view, together with accuracy and efficiency, model used should be as simple as possible in order to limit simulation time. As a good approximation, a triangular potential distribution at the oxide-semiconductor surface is assumed to decouple Schrödinger's equation from Poisson equation. Using triangular potential well (TPW) approximation, we replace the potential $\phi(z)$ in equation (2) by $-F_S.z$ (where F_S is the surface electric field) for $z>0$ and by an infinite barrier for z<0; [26]. Under this approximation, solution of Schrödinger's equation is represented by Eigen-functions as an Airy function solution

$$\xi_{ij}(z)=Ai\left(\left(\frac{2\cdot m_i^{\perp}\cdot q\cdot F_S}{\hbar^2}\right)^{\frac{1}{3}}\cdot\left(z-\left(\frac{E_{ij}^0}{q\cdot F_s}\right)\right)\right) \quad (5)$$

and the corresponding Eigen-energy values are:

$$E_{ij}^0=\left(\frac{\hbar^2}{2\cdot m_i^{\perp}}\right)^{\frac{1}{3}}\cdot\left[\frac{3}{2}\cdot\pi\cdot q\cdot F_S\cdot\left(j+\frac{3}{4}\right)\right]^{\frac{2}{3}} \quad (6)$$

where $F_S=\frac{q}{\varepsilon_{Si}}\cdot\left[N_{Inv}+N_{Dep}\right]$ is the surface electric field (7a)

$N_{Dep}=\sqrt{\frac{2\cdot\varepsilon_{Si}\cdot\varepsilon_0\cdot\phi_S\cdot N_A}{q}}$ is the depletion charge density (7b)

and $N_{Inv}=\sum_{i,j}N_{i,j}$ is the inversion charge density. (7c)

Since the depletion layer charge is due to ions, not the carriers, no quantum calculation is required for its analysis. The energy levels E_{ij}^0 forming the 2-DEG inversion layer are expressed with reference to energy value $Ec(0)$ of conduction-band edge at the $Si\text{-}SiO_2$ interface.

$$\text{i.e.} \quad E_{ij}=E_{ij}^0+Ec(0) \quad (8)$$

where $Ec(0)$ is given by the relation $Ec(0)-E_F=q\cdot\left(\frac{E_G}{2}-\phi_S+\phi_F\right)$ and is shown in Fig. 1 in which E_G is the energy band-gap of silicon, and ϕ_S is the surface potential determined by

$$V_G=V_{fb}+V_{ox}+\phi_S \quad (9)$$

where $V_{ox}=\frac{\varepsilon_{Si}}{C_{ox}}\cdot F_S$

V_{fb} is the flat-band voltage of the device.

In our work, we have analyzed the device for V_{fb} = n+ poly-*Si* gate with substrate chosen to be uniformly doped. The poly-*Si* gate chosen is so heavily doped that the fermi energy level in gate is same as the conduction band.

Thus, solving equations (6) – (9) iteratively, the relation between N_{Inv} and $Ec(0) - E_F$ is determined i.e. one can express N_{Inv} as a function of gate-to-source voltage (V_G) for a given oxide thickness (t_{ox}) and substrate doping (N_A). Furthermore this ϕ_S - based model can be extended to evaluate threshold voltage (V_{Th}) and drain current (I_D) of the device.

1. Threshold Voltage

The threshold voltage V_{Th} in MOS transistor is one of the most important parameter for circuit, device and process characterization. By definition, the conventional strong inversion condition is the surface potential $\phi_{STh} = 2.\phi_F$, which we say is the classical definition of threshold voltage. However, due to the inversion layer quantization effect, the electron distribution is pushed away from the surface; the conventional strong inversion condition will not be valid then. For this reason, we use the following strong inversion condition [17]:

$$\left|\frac{dQ_{Inv}}{d\phi_S}\right|_{\phi_S=\phi_{STh}} = \left|\frac{dQ_{Dep}}{d\phi_S}\right|_{\phi_S=\phi_{STh}} \tag{10a}$$

which in turn is equivalent to equation

$$\left|\frac{dQ_{Inv}}{dV_G}\right|_{V_G=V_{Th}} = \left|\frac{dQ_{Dep}}{dV_G}\right|_{V_G=V_{Th}} \tag{10b}$$

where Q_{Inv} and Q_{Dep} are the inversion layer charge and depletion layer charge; equals to product of electronic charge with N_{Inv} and N_{Dep} respectively, and V_{Th} is the threshold voltage. Appendix A provides the system of equations used in determining threshold voltage of the device based on the condition described by equation (10b).

2. Drain Current

A major advantage of surface potential (ϕ_S) based – model is the drain current (I_D) calculation, which uses a single equation for the whole operation range. The approach of the charge-sheet model [27], which is based upon the drift-diffusion equation and Gauss's Law, is used in our analysis. Under the assumptions of gradual channel and charge-sheet approximations, and if the mobility μ is assumed to be constant along the channel [27], the drain current can be written as

$$I_D = I_{Drift} + I_{Diffusion} \tag{11}$$

where,

$$I_{Drift} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_G - V_{fb}) \cdot (\phi_{SL} - \phi_{S0}) - 0.5 \cdot (\phi_{SL}^2 - \phi_{S0}^2) - \frac{2}{3} \cdot \gamma \cdot (\phi_{SL}^{1.5} - \phi_{S0}^{1.5}) \right] \tag{12}$$

γ is the body-effect coefficient given by $\gamma = \frac{\sqrt{2 \cdot \varepsilon_{Si} \cdot \varepsilon_0 \cdot q \cdot N_A}}{C_{ox}}$

and

$$I_{Diffusion} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot V_t \left[(\phi_{SL} - \phi_{S0}) + \gamma \cdot (\phi_{SL}^{0.5} - \phi_{S0}^{0.5}) \right] \tag{13}$$

where V_t is the thermal voltage; $V_t = \frac{k_B \cdot T}{q}$

In the above equations, ϕ_{SL} *and* ϕ_{S0} denote the surface potential at the drain end and source end respectively. *W* is the width of the device, *L* is the channel length and C_{ox} is the oxide capacitance per unit area. The above equations do not depend on whether a classical or a quantum formulation based surface potential is used. It is a result of the very basic drift-diffusion equation and Gauss's Law, which have the same form in terms of charge and gradients of charge for both quantum and classical approaches. However, it differs in the way, in which surface potential is calculated.

For the classical approach, surface potential ϕ_S is found from the following expression:

$$\phi_S^{CL} = V_G - V_{fb} + \frac{Q_S^{CL}}{C_{ox}} \tag{14}$$

in which

$$Q_S^{CL} = -\gamma \cdot C_{ox} \cdot \sqrt{V_t \cdot \left[\alpha + \exp\left(\frac{-2 \cdot \phi_F - V_{cb}}{V_t}\right) \cdot \left(\exp(\alpha) - 1 - \alpha \cdot \exp\left(\frac{V_{cb}}{V_t}\right) \right) + \exp(-\alpha) - 1 \right]} \tag{15}$$

where V_{cb} varies from V_S at the source end to the V_D at the drain end, and $\alpha = \frac{\phi_S^{CL}}{V_t}$.

For the quantum drain current calculation, once ϕ_{S0}^{QM} , quantum approach based surface potential at the source end *(x=0)* is determined using equation (9) for a given substrate doping, oxide thickness and gate bias, we have determined ϕ_{SL}^{QM} , surface potential at the drain end

(x=L) by inputting incremental values of V_D [20].

The same equation for drain current (I_D) is extended for the saturation region by replacing the drain bias voltage with the saturation drain voltage ($V_D = V_{Dsat}$) at the particular applied gate voltage without taking into account the effects of channel length modulation (CLM) and kink effect. The value of saturation voltage V_{Dsat} is extracted by setting the derivative of drain current with respect to drain bias to zero (pinch-off condition) i.e. $\left.\frac{\partial I_D}{\partial V_D}\right|_{V_D = V_{Dsat}} = 0$.

IV. Introduction Of High-k Gate Dielectrics

The sub-100 nm MOSFETs face a scaling limit, when a SiO_2 gate dielectric is used, and it requires alternative gate-dielectric materials with higher permittivity and greater physical thickness which prevents tunneling. However, the use of a high-k#gate material may result in dielectric thickness comparable to the device gate length, resulting in increased fringing fields [28] from the gate to the source/drain regions and compromised short-channel performance. Thus, understanding the impact of different high-k dielectric materials on device performance is important. Essentially the key idea in high-*k* design is to produce the same drain current performance in using SiO_2, but replacing the SiO_2 dielectric thickness with a thicker high-*k* that suppresses tunneling effect.

A high-*k* film will be physically thicker than a pure SiO_2 layer by the ratio of its dielectric constant to that of SiO_2, and still provide the same gate capacitance, as

$$C_{ox} = \frac{k_{ox} \cdot \varepsilon_0}{t_{ox}} = C_{high-k} = \frac{k_{high-k} \cdot \varepsilon_0}{t_{high-k}} \quad (16)$$

implying

$$t_{high-k} = \left(\frac{k_{high-k}}{k_{ox}} \right) \cdot t_{ox} \quad (17)$$

thus potentially reducing direct tunneling current substantially.

In the context of high-*k* dielectrics, we express eqn (17) in terms of the equivalent oxide thickness (EOT) defined as the thickness of a pure SiO_2 layer which provides the same gate capacitance as a high-*k* layer,

$$EOT = \left(\frac{k_{ox}}{k_{high-k}} \right) \cdot t_{high-k} \quad (18)$$

At first glance, it would seem that an arbitrarily high-*k* value would allow a substantially thick dielectric film to meet very small EOT targets. In practice, the extreme gate dielectric thickness-length aspect ratio that would result from a very high-*k* value and hence a very thick insulator leads to fringing field effects which undermine the gate electrode's ability to maintain control of the channel [11]. Also, it is known that silicon-single high-*k* material systems might suffer from unacceptable levels of bulk fixed charge, high density of interface trap states, and low silicon interface carrier mobility [29]. An extremely thin interfacial oxide is used to passivate the interface and minimize interface states when high-*k* gate materials are deposited. Also, using the low-*k* gate dielectric one can well confine the electric-fields within the channel region thereby significantly reducing the fringing fields from gate-to-source/drain regions. Thus, use of multiple material layers is a good approach to the gate dielectric for scaled MOSFETs with gate lengths less than 100nm.

In order to model gate stack structure, we have analyzed dielectric thickness (physical/equivalent) of 1.5nm in our cases with n+ poly-*Si* gate. In the modeling section, V_{ox} given in equation (9) is replaced by $V_{ox1}+V_{ox2}$ with the introduction of gate stack architecture in which

$$V_{ox1} = \frac{Q_S}{C_{ox1}} \text{ and } V_{ox2} = \frac{Q_S}{C_{ox2}} \quad (19)$$

for different dielectric layers ϵ_1 and ϵ_2. The EOT of the dielectric stack can be obtained by the above equation in terms of dielectric constants and thicknesses as

$$EOT_{Stack} = t_{SiO_2} + \left(\frac{k_{SiO_2}}{k_{high-k}} \right) \cdot t_{high-k} \quad (20)$$

V. Results And Discussion

All calculations were made for temperature $T = 300$ *K*. Fig 3 shows the variation of surface potential (ϕ_S)

versus gate voltage (V_G) with flat band voltage V_{fb} = n+ *poly-Si* gate for both classical and quantum-mechanical cases. The inset of the figure proves the validity of model by matching the results with the available fully self-consistent results of Y. Ma etal. [30]. It is clear that in quantum-mechanical case, surface potential does not become constant in strong inversion regime, and rather follows a gradual increase. This happens due to confinement of inversion carriers, which results in a peak of inversion charge density separated from the interface and an increased width of inversion layer.

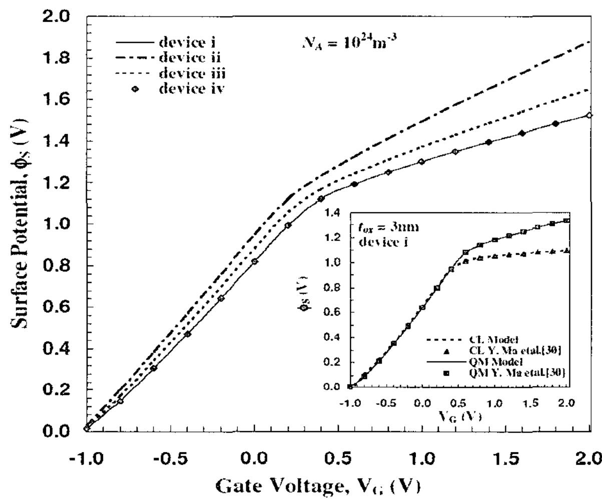

Fig. 3. Surface potential variation with gate voltage for the system shown in Fig. 2 for n+ poly gate. **Inset** shows ϕ_S vs. V_G for classical (CL) and quantum approach (QM) together with self-consistent results of Ma Y etal.

Thus, the same charge density would result in a higher surface potential in comparison to classical case. The figure also shows surface potential for the four devices under consideration as shown in Fig. 2. An increase in surface potential is seen, as the dielectric permittivity of dielectric increases. It is due to the fact that the capacitance of dielectric is directly proportional to its permittivity, and high capacitance influences more charge thereby increasing surface potential of the device. But, in order to optimize the device characteristics i.e. to obtain the same surface potential, a gate stack system is analyzed to retain the same surface charge density allowing the gate dielectric permittivity to change and in turn corresponding thickness of the high-*k* gate dielectric is calculated using equation (20). One can thus obtain the same EOT for the stack, but with greater physical thickness, in order to have low gate tunneling currents. Thus, the variation of surface potential for the fourth device is found to be same as that of using single dielectric SiO_2.

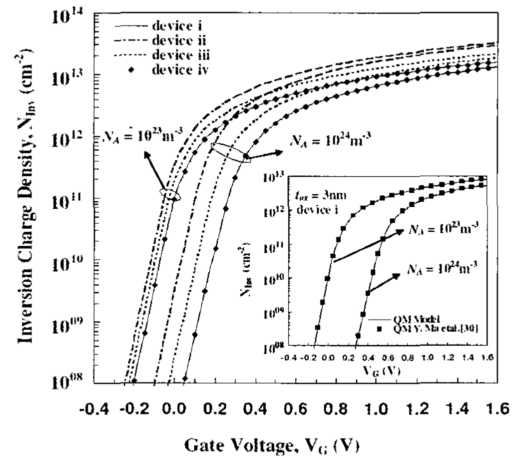

Fig. 4. Variation of Inversion charge density with gate voltage for Fig. 2 devices for different doping densities. Inversion charge density together with Ma Y etal. results are shown in **inset**.

The inversion charge density (N_{Inv}) variation with gate bias together with Y. Ma etal. results [30] at different doping concentrations are shown in Fig. 4. The results so obtained coincide well with the reported self-consistent solution (Y. Ma etal.) as shown in inset of the figure. It can be clearly understood from the graph, that due to carrier energy quantization the total inversion charge induced at a given gate voltage is decreased with increase in doping. Furthermore comparison for the four devices under consideration is done in the drawn figure. As can be interpreted, with increase in the dielectric permittivity of the gate dielectric, the same charge density is achieved at earlier gate voltages. Also the device (iv) in Fig. 2 is found to be analogous to single dielectric SiO_2.

Fig. 5 and its inset show the variation of device threshold voltage with doping concentration for the Fig. 2 devices along with simulated results [11]. The parameters used in our calculations are taken from [11]. One of the well known consequences of the energy quantization in the inversion layer is the increase of the threshold voltage. The values of threshold voltage extracted are found to be in good agreement with the data justifying the analysis. Also a shift in the value of threshold voltage is found while obtaining the results from classical approach to quantum theory i.e. QEs lead

to increase in threshold voltage. This shift in threshold voltage with doping concentration is plotted in Fig. 6 and agrees well with T. Janik etal. results [17]. The shift in V_{Th} value from classical to quantum approach is due to over-estimation of the inversion charge carrier density in classical case.

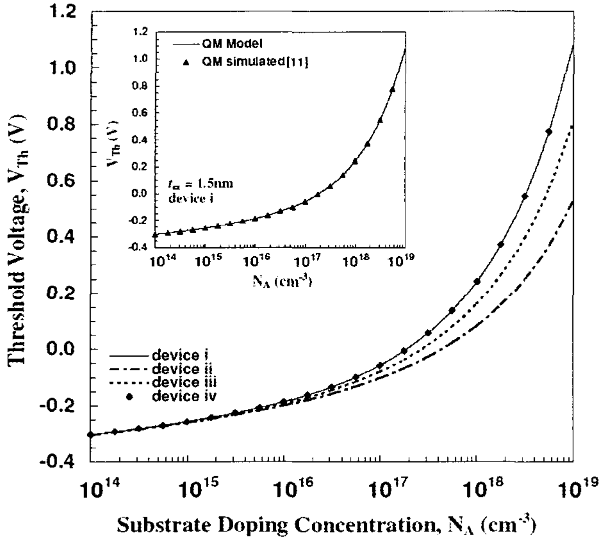

Fig. 5. Threshold voltage variation with doping concentration with simulated data is shown in **inset**. Fig. 2 system is analyzed for the variation of threshold voltage with doping concentration.

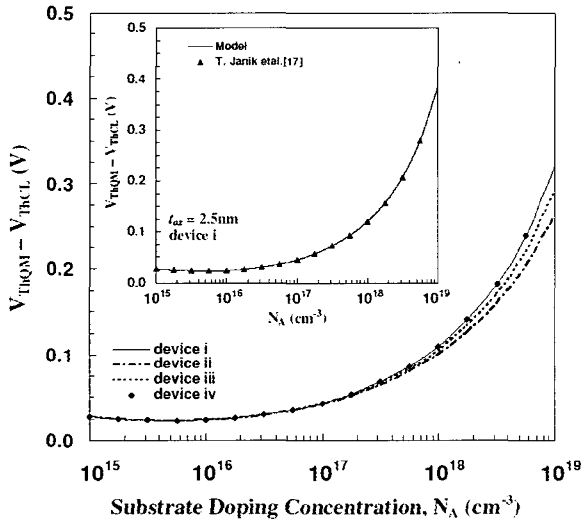

Fig. 6. Threshold voltage shift variation with doping concentration due to CL and QM approach with Janik T etal. results.

Using the developed surface potential based model, drain characteristics of the devices illustrated in Fig. 2 are obtained for two gate voltages 1.2V and 1.8V in Figs. 7a and 7b. Curves show comparison of classical and quantum approach together with simulated data [20] for the same set of parameters as shown in Fig. 7a. The developed results are in fair agreement with the available simulated results. One infers from the graphs that an increase in the value of permittivity results in higher value of drain current at the same gate bias. It is found that with the increase in the dielectric permittivity of gate dielectric saturation voltage decreases as high-k influences more charge and hence more channel potential at same gate bias. Also the pinch-off approach adopted in our analysis for calculating the saturation voltage of the device and thus obtaining saturation current is more promising and is free from any fitting parameters.

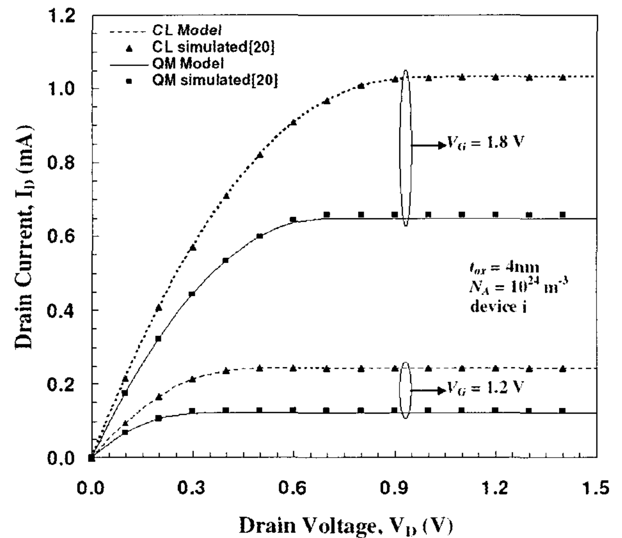

Fig. 7a. Drain characteristics with drain bias at V_G = 1.2V and 1.8V for CL and QM models together with available simulated results for n+ poly gate for device i. W/L =10, μ = 250 cm^2/V.sec (constant)

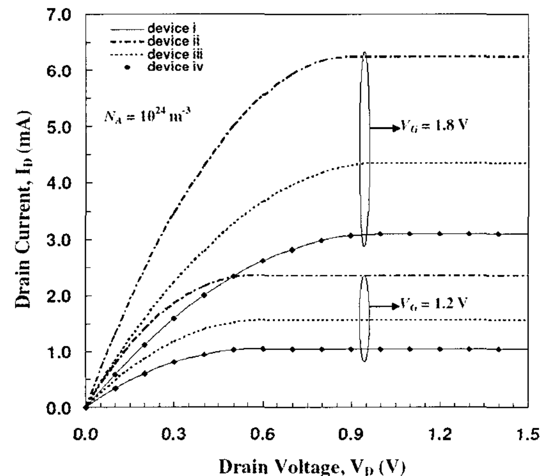

Fig. 7b. Drain current variation with drain bias at V_G = 1.2V and 1.8V for Fig. 2 devices.

Variation of physical dielectric thickness of upper dielectric (k_1) with doping concentration is plotted in Fig. 8 to achieve targeted threshold voltage keeping configuration of lower dielectric layer adjoining to substrate to be fixed (t_{ox2} = 0.5nm and k_2 for SiO_2). Curves show that with the increase in substrate doping, the dielectric thickness decreases whereas on increasing the dielectric constant for the same set of parameters yields in the increase in dielectric thickness. Also the change in dielectric thickness with dielectric constant k_1 can be seen in inset. The demarcation line shown in the inset resembles the device with single dielectric configuration i.e. SiO_2 only. Figure shows that at constant threshold voltage, on comparison with single dielectric gate structure, increase in dielectric permittivity increases the physical thickness of the dielectric sandwiched between gate electrode and substrate resulting in greater distance between the gate electrode and the substrate thus reducing the gate leakage current. Thus the formulation in turn gives the relation between different parameters such as gate dielectric thickness, gate dielectric constant and doping density required for device fabrication for the given threshold voltage.

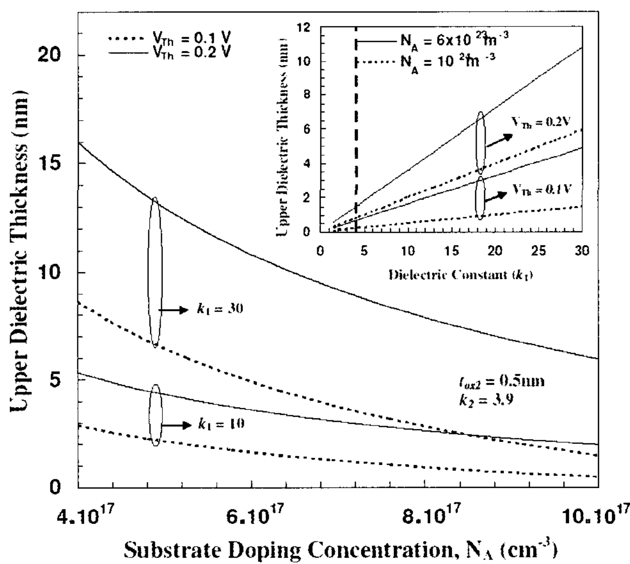

Fig. 8. Upper physical dielectric thickness variation with doping density for obtaining targeted threshold voltages at different dielectric permittivity keeping lower dielectric thickness and permittivity fixed and equals to 0.5nm and 3.9 (SiO_2). **Inset** shows variation of Upper dielectric thickness with dielectric thickness for same device threshold at different doping concentration.

VI. CONCLUSION

The surface potential based model is developed and is used to determine the characteristics of the device. This model considers the decoupling of Poisson's and Schrödinger's equations using triangular potential well (TPW) approximation instead of fully self-consistent approach by Y. Ma etal. [30]. The characteristics obtained by the model matches well with available data. The threshold voltage analysis is based on a definition more applicable for the quantum approach and on more realistic assumptions. A compact analytical model quantitatively describes the threshold voltage shifts due to quantum effects as a function of the doping concentration. The gate voltage dependence of the inversion layer charge is thus modeled quite accurately by the use of the triangular potential well approximation. Consequently, this approximation is found to be both an accurate and efficient method for modeling the I-V characteristics of the MOS transistor. Also introduction of gate stack architecture improves the characteristics of the device. One can interpret that with the increase in gate dielectric thickness tunneling current in the channel decreases. This allows one to use physically thicker films thereby reducing the tunnelling current while maintaining the same gate capacitance needed for scaled device operation. So downscaling of dielectric thickness is possible without compromising the reduction in physical thickness of gate dielectric, and this has become possible due to the introduction of gate stack architecture. An optimization of gate dielectric thickness yields as a helping aid in device fabrication with targeted threshold voltages.

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APPENDIX A

$$\frac{dQ_{Inv}}{dV_G} = q \cdot \left(\frac{k_B \cdot T}{\pi \cdot \hbar^2}\right) \cdot \sum_i n_{vi} \cdot m_{di} \cdot \sum_j \frac{-\exp\left(\frac{E_F - E_{ij}}{k_B \cdot T}\right)}{1+\exp\left(\frac{E_F - E_{ij}}{k_B \cdot T}\right)} \cdot \frac{1}{k_B \cdot T} \cdot \frac{dE_{ij}}{dV_G} \tag{A1}$$

$$\frac{dQ_{Dep}}{dV_G} = \sqrt{\frac{q \cdot \varepsilon_{Si} \cdot \varepsilon_0 \cdot N_A}{2 \cdot \phi_S}} \cdot \frac{d\phi_S}{dV_G} \tag{A2}$$

$$\frac{dE_{ij}}{dV_G} = \left(\frac{\hbar^2}{2 \cdot m_i^{\perp}}\right)^{\frac{1}{3}} \cdot \left[\frac{3}{2} \cdot \pi \cdot q \cdot \left(j + \frac{3}{4}\right)\right]^{\frac{2}{3}} \cdot \frac{2}{3} \cdot F_S^{\frac{-1}{3}} \cdot \frac{dF_S}{dV_G} - q \cdot \frac{d\phi_S}{dV_G} \tag{A3}$$

$$\frac{d\phi_S}{dV_G} = 1 - \frac{\varepsilon_{Si}}{C_{ox}} \cdot \frac{dF_S}{dV_G} \tag{A4}$$

$$\frac{dF_S}{dV_G} = \frac{1}{\varepsilon_{Si}} \cdot \left[\frac{dQ_{Inv}}{dV_G} + \frac{dQ_{Dep}}{dV_G}\right] \tag{A5}$$

The above system of equations is solved iteratively to get the threshold voltage of the device using condition given by equation (10b).

Table 1. Physical quantities used in the calculations. All effective masses are in units of the free electron mass.

Surface	**< 100 >**	
Valleys	**Lower**	**Higher**
i	1	2
n_{vi}	2	4
m_{zi}	$0.916.m_0$	$0.190.m_0$
m_{di}	$0.190.m_0$	$0.417.m_0$

$m_0 = 9.1 \times 10^{-31}$ Kg = free electron mass

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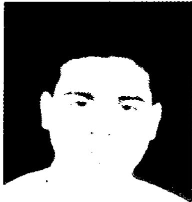

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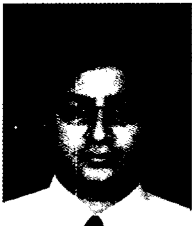

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