Cell Signal Distribution Characteristics For High Density FeRAM

Hee-Bok Kang, Young-Jin Park, Jae-Jin Lee, Jin-Hong Ahn, Man-Young Sung*, and Young-Kwon Sung*

Abstract—**The sub-bitline (SBL) sensing voltage of a cell and total cell array can be measured by the method of SBL voltage evaluation method. The MOSAID tester can collect all SBL signals. The hierarchical bitline of unit cell array block is composed of the cell array of 2k rows and 128 columns, which is divided into 32 cell array sections. The unit cell array section is composed of the cell array of 64 rows and 128 columns. The average sensing voltage with 2Pr value of 5μC/cm^2 and SBL capacitance of 40fF is about 700mV at 3.0V operation voltage. That is high compensation method for capacitor size degradation effect. Thus allowed minimum 2Pr value for high density Ferroelectric RAM (FeRAM) can move down to about less than 5μC/cm^2.**

Index—**Ferroelectric memory, boost voltage control, hierarchical bitline, SBL, MBL**

I. Introduction

FeRAM[1][2] is best suited for devices, which require high security and low power consumption. FeRAM write cycle time is short enough to be ignored. Writing time of 1 byte data on FeRAM is 1/30,000 less than EEPROM. FeRAM current consumption is estimated for low power smart card application. Utilizing the advantages of high-speed read-write and high-security, FeRAM is fit for smart cards. Battery Backed-up SRAM (BBSRAM) consists of an SRAM and a battery. With two components, BBSRAM is fairly expensive, and also using battery is not environmentally friendly. FeRAM is a perfect solution for both problems. Since FeRAM doesn't need a battery, it can replace the SRAM and the battery. This will bring the user three benefits of lower cost, maintenance free, and environmentally friendly. FeRAM RF-ID chip can provide the following advantages, which could not be provided by commonly used EEPROM based RF-ID chip. Low power consumption can improve the operating range. Energy consumption of FeRAM is 1/400 of less than EEPROM. The power delivered to the load must provide certain threshold voltage and power for the circuits to function. Because of the low power consumption nature of FeRAM, the operating range could be improved within given field strength or power density. Given the bandwidth limitations and anti-collision schemes, low power consumption tag offer better data rate in exchange of speed of identification. FeRAM is best fit for this purpose. FeRAM has process advantage without much investment comparing with other memory to shrink the die size further. With read-write endurance of more than 1E12 or 1E15, FeRAM is more durable and suitable for applications, which requires frequent write. To overcome the conventional sensing voltage margin issues from weak memory cells and long term data retention, one method is to enhance the properties of ferroelectric capacitor. Another option is to enhance the circuit performance in sensing scheme to compensate FeRAM cell weakness. To enhance the sensing margin

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in bitline (BL), BL capacitance is targeted to smaller than that of DRAM. The BL and plateline (PL) are boosted to higher voltage than supply power voltage. For this purpose, we propose sensing scheme with hierarchical BL, where BL is separated into sub-BL (SBL) and main-BL (MBL) with common MBL bus (CMB)[3]. Isolated SBL loading is 40fF, and the resulting enhanced SBL sensing voltage triggers NMOS current gain transistor (CGT) with static current margin window of more than 100μA, which is compared to high performance SRAM cell current. MBL sensing voltage is determined by the current ratio between CGT and MBL sensing load (MSL) device. The total load connected to CGT drain is estimated to be 2pF and more than 50 times larger than that of SBL.

II. Overview Of FeRAM, MRAM And PRAM

Like a DRAM cell, the unit FeRAM cell structure comprises a transistor (1T) to access a stored data and a capacitance (1C) to store data as shown in figure 1. However, different from DRAM, which uses such paraelectric oxide layer as silicon oxidized film or silicon nitride film for the storage capacitance, the FeRAM structure uses ferroelectric material. As a result, FeRAM technologies are similar to DRAM cell technologies, and the two technologies can be cooperated relatively easily. Cell stored data is detected by reading the charges in polarization capacitor when a voltage is applied to the PL. To understand the principles of operation of FeRAM, hysteresis loop as the dependence of electric charge in polarization on bias voltage need to be understood. The horizontal axis represents the potential of the bottom electrode with respect to the top electrode. The vertical axis represents the electric charge corresponding to the potential.

When voltage applied to the ferroelectric capacitor is 0V, the ferroelectric characteristics of −Pr and +Pr are used for the two states of polarization for data '0' and data '1', i.e., the -Pr polarization for data '0' and the +Pr polarization for data '1'. In precharge period, the BL, WL and PL is 0V state. In read operation period, the BL is changed to float state and the WL and PL are changed to high state, then each charges of +Pr and -Pr are met to the equalized states with the BL charges of data '1' and data '0' respectively.

The ferroelectric film on the memory cell capacitor is made of PZT (Pb(Zr, Ti)O3), SBT (SrBi2Ta2O9), or BLT ($Bi_{4-x}La_xTi_3O_{12}$) permitting high storage density. Also, write operation of FeRAM is controlled by the electrical polarization of ferroelectric capacitor by applying the electric field, compared to writing by injecting hot electrons, as is done on Flash Memory.

PZT is chemically expressed as ABO3, with an octahedron constructed by six oxygen atoms including a smaller metallic element near their center. PZT has high remnant polarization values of 2Pr. SBT or BLT, has a low Ec, enables an operating low voltage by making the film thinner, and exhibits little fatigue even after polarization has been reversed more than 10E12 times. The ferroelectric polymer thin film is also can be the candidate polarization material in FeRAM. The ferroelectric polymer film has the characteristics of low polarization value of about less than 5μC/cm^2 and low temperature process of about 200 °C. Consequently, PZT or SBT is seen as a promising material for highly integrated FeRAM, but the ferroelectric polymer film is expected to low cost material for simple process FeRAM

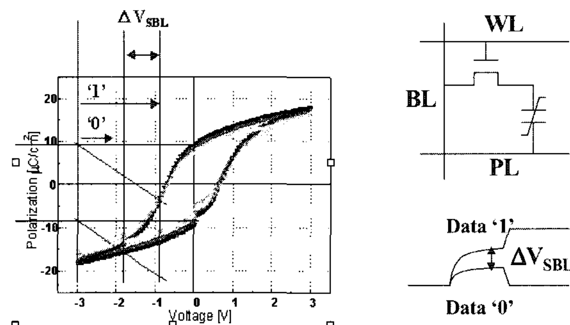


Fig. 1. FeRAM cell structure and operation

The operation of magnetoresistive RAM (MRAM) is to utilize the change of magnetic tunnel junction (MTJ) resistance, which is determined by the magnetic field direction of free (or program) layer to the fixed layer as shown in figure 2. There are several major issues in scaling. First is the write current increasing, which is opposed to the write metal line scaling. Second is cell-to-cell interference, which means a selected MTJ placed at cross point of selected writing bitline (BL) and writing wordline (WL2) during writing operation disturbs adjacent MTJs resulting in false states.

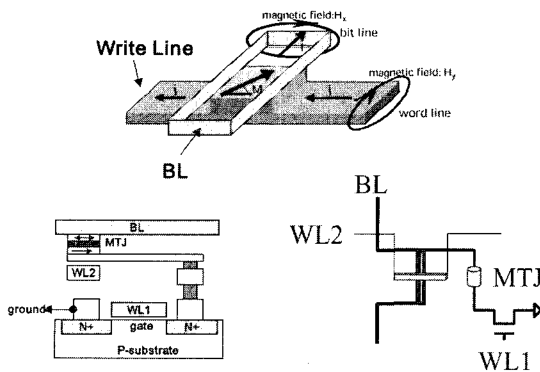


Fig. 2. MRAM cell structure and operation

The operation of phase-change RAM (PRAM) is to utilize the change of different resistance states, which is determined by the current induced heat of 600 °C in chalcogenide semiconductor based material as shown in figure 3. There are several major issues in scaling. First is the high level of RESET current, which is burden to the metal oxide semiconductor field effect transistor (MOSFET) based cell structure scaling. Second is smaller sensing window of read voltage range in cell size scaling.

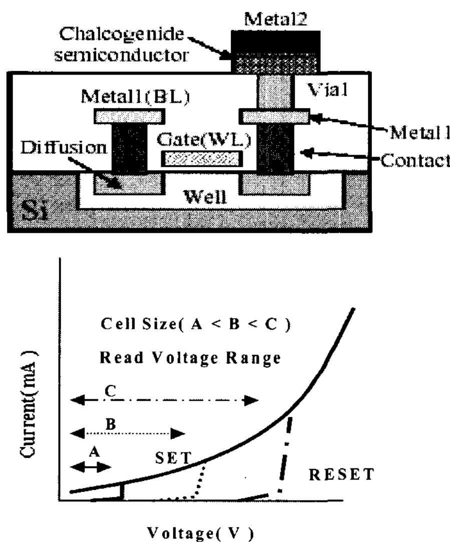


Fig. 3. PRAM cell structure and operation

III. FeRAM Circuit Scheme And Measured Results

The SBL sensing voltage of data '1' and data '0' is determined by the characteristics of hysteresis curve of ferroelectric capacitor as shown in figure 1. Thus SBL sensing voltage of ΔV_{SBL} is calculated from polarization charge and SBL capacitance. The data '1' voltage is from the switching charge of P* divided by SBL capacitance and data '0' voltage is from the non-switching charge of P^ divided by SBL capacitance. SBL sensing voltage is maximized by certain SBL capacitance and reduced according to the difference level from certain SBL capacitance. The SBL sensing voltage of a cell and total cell array can be measured by the method of SBL voltage evaluation method as shown in figure 4. The MOSAID tester can collect all SBL signals. The unit cell array block is composed of the cell array of 2k rows and 128 columns, which is divided into 32 cell array sections. The unit cell array section is composed of the cell array of 64 rows and 128 columns with SBL, SBL switch (SBSW) devices of SBPD, SBSW1 and SBSW2, and CGT device. MBL is driven by one out of 32 SBL, biased by MSL device. The 128 sense amplifiers (SAs) in peripheral circuit region are shared to all cell array blocks.

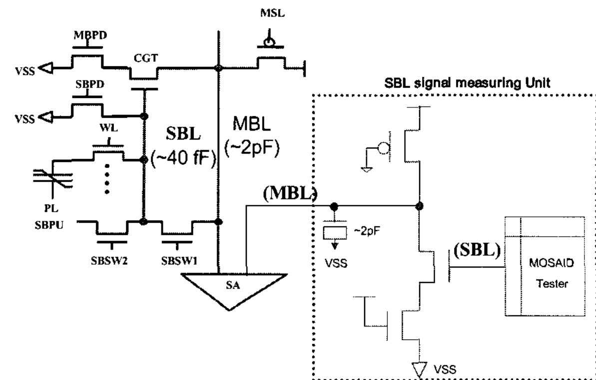


Fig. 4. Hierarchical bitline cell array architecture and SBL voltage evaluation method

The operational timing diagram of hierarchical bitline is shown in figure 5. The proposed boosted voltage control of SBL and PL in hierarchical bitline scheme is worked well for sufficient operating voltage margin of FeRAM cell.

In the period t5, all selected cells are written to data '1' with boosted voltage in SBL and ground voltage in PL. In the period t6, the cells of data '0' are restored or rewritten to data '0' with boosted voltage in PL and ground voltage in SBL. But in same period t6, the

remained cells of data '1' are sustained to data '1' with boosted voltage in SBL and Boosted voltage in PL. The 2Pr trend to capacitor size variation is shown in figure 6.

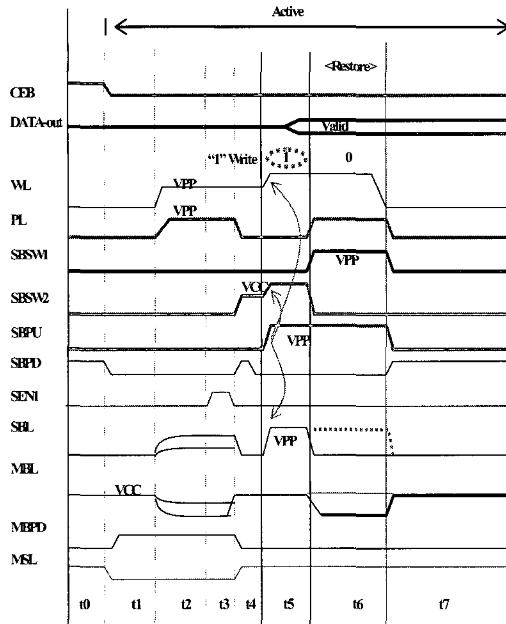


Fig. 5. Memory cell operation timing diagram

The remnant polarization of a certain capacitor is proportional to the capacitor size. Thus the 2Pr value of remnant polarization is more decreased at small capacitor size. The slope is mainly depended to the process matured level. In initial state of a certain process technology development, the slope will be steep. But in matured state of the technology, the slope will change to stabilized horizontal level.

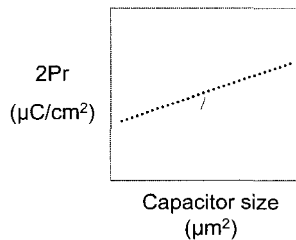


Fig. 6. 2Pr trend to capacitor size variation

The 2Pr values of SBT and PZT are shown in figure 7. The typical 2Pr values of SBT and PZT are about $10\mu C/cm^2$ and $30\ \mu C/cm^2$ in normal capacitor size of above $1.0\mu m^2$, respectively.

The measured SBL signals of 2Pr value of about $10\mu C/cm^2$ at capacitor size of $0.7\mu m^2$ is shown in figure 8. The average sensing voltage at SBL of 40fF is about 900mV at 3.0V operation voltage. The sensing voltage distribution is about 1.5~2.0V ranges. That is key issue for cell characteristics for high density in FeRAM cell size scaling.

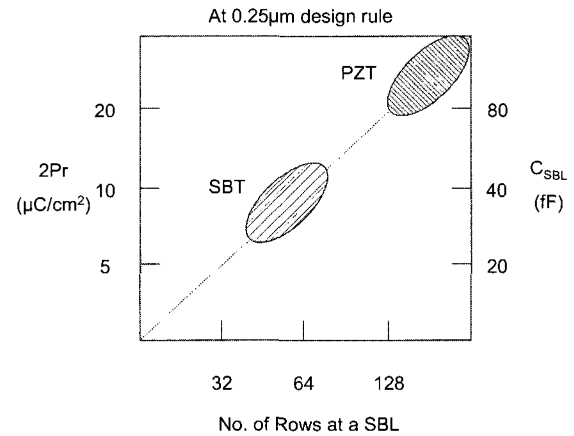
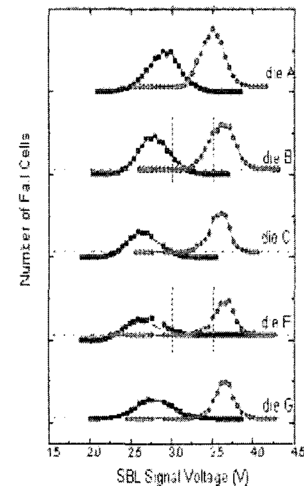


Fig. 7. 2Pr characteristics of SBT and PZT



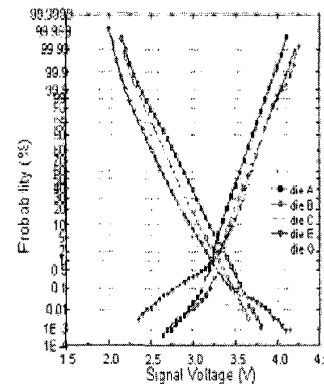


Fig. 8. Measured SBL signals at $2Pr = \sim 10\mu C/cm^2$ and $C_{SBL}=40fF$

The distribution properties of FeRAM cell are mainly from the grain and domain orientation or direction effect in ferroelectric capacitor. The PZT material is simple tetragonal structure, but the SBT material is more complicated layered supper lattice structure. The domain orientation is dependent to the activation energy in the ferroelectric film process. The domain orientation is non-uniform so that the 2Pr characteristics are also non-uniform. The activation energy control mechanism and method during the ferroelectric film process should be severely studied. Which is more controllable material between PZT and SBT.

We must focus to the material, which can be easily controllable in cell size scaling.

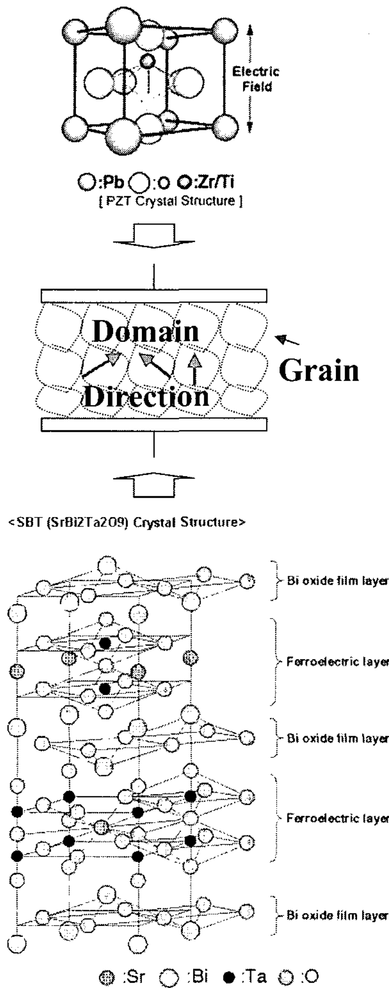


Fig. 9. The grain and domain orientation effect

The measured SBL signals of 2Pr value of 5μC/cm^2 at capacitor size of 0.7μm^2 is shown in figure 10. The average sensing voltage at SBL of 40fF is about 700mV at 3.0V operation voltage. The distribution of cell data moved to the more uniformed state. The 2Pr value of 5μC/cm^2 is more marginal than the 2Pr value of 10μC/cm^2. The urgent issue for FeRAM cell is not the 2Pr value. More urgent issue for FeRAM cell is uniformity. The hierarchy circuit scheme can accept the more small 2Pr values if it has good uniformity. The circuit scheme can solve the capacitor-size dependant 2Pr degradation effect. Thus allowed minimum 2Pr value for high density FeRAM can move down to about less than 5μC/cm^2. The detailed mechanism on increased uniformity in small 2Pr value is not clear until now. We can induce the clue for perfect uniformity control from this somewhat changed characteristics.

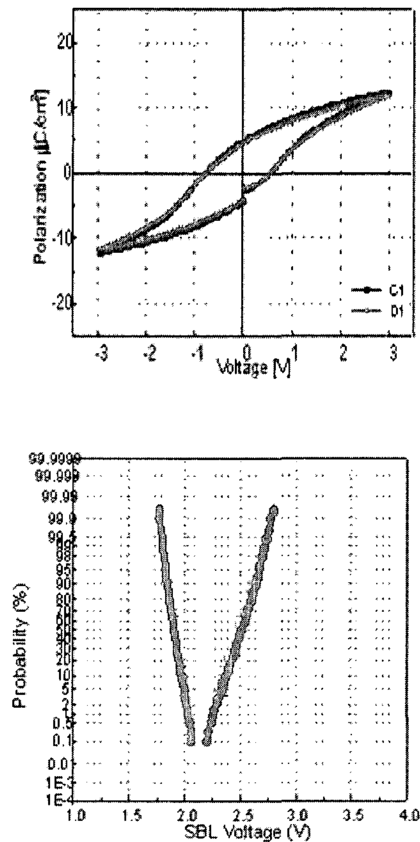


Fig. 10. Measured SBL signals at 2Pr=5μC/cm^2 and C_{SBL}=40fF

IV. CONCLUSIONS

The all cell characteristics of a FeRAM chip at SBL level can be evaluated by the proposed external

measurement method. The major key issue for FeRAM cell scaling is the cell data uniformity property. The 2Pr value can not be major issue with the hierarchical bitline scheme on the base of small SBL capacitance of 40fF or less and boosted SBL and PL voltage control.

The allowed 2Pr value of hierarchical bitline structure falls less than 5μC/cm^2 at SBL capacitance of 40fF and capacitor size of 0.7μm^2 in the design rule of 0.25μm range.

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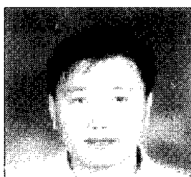

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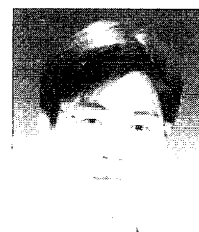

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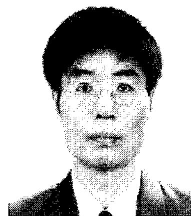

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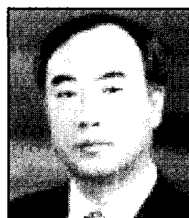

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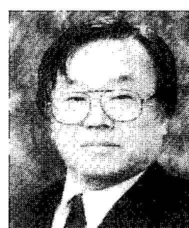

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