Wafer-Level Three-Dimensional Monolithic Integration for Intelligent Wireless Terminals

R.J. Gutmann, A.Y. Zeng, S. Devarajan, J.-Q. Lu, and K. Rose

Abstract—**A three-dimensional (3D) IC technology platform is presented for high-performance, low-cost heterogeneous integration of silicon ICs. The platform uses dielectric adhesive bonding of fully-processed wafer-to-wafer aligned ICs, followed by a three-step thinning process and copper damascene patterning to form inter-wafer interconnects. Daisy-chain inter-wafer via test structures and compatibility of the process steps with 130 nm CMOS SOI devices and circuits indicate the viability of the process flow. Such 3D integration with through-die vias enables high functionality in intelligent wireless terminals, as vertical integration of processor, large memory, image sensors and RF/microwave transceivers can be achieved with silicon-based ICs (Si CMOS and/or SiGe BiCMOS). Two examples of such capability are highlighted: memory-intensive Si CMOS digital processors with large L2 caches and SiGe BiCMOS pipelined A/D converters. A comparison of wafer-level 3D integration with system-on-a-chip (SoC) and system-in-a-package (SiP) implementations is presented.**

Index Terms—**3D Integration, wafer bonding, intelligent wireless terminal, memory-intensive digital processors, pipelined A/D converters**

I. Introduction

As the density of RF ICs increases with improved two-dimensional (2D) packaging of chips and vertical three-dimensional (3D) chip stacking, the relative cost of packaging increases as well. While a monolithically integrated system-on-a-chip (SoC) is a worthy long-term objective for digital systems, the heterogeneous IC technologies necessary for high-performance RF systems such as intelligent wireless terminals makes a SoC implementation difficult. While a hybrid assembled system-in-a-package (SiP) implementation is a more realistic objective for intelligent wireless terminals, the long-term cost of either 2D or 3D die-stack packaging solutions will be impacted by chip handling and assembly.

One viable solution for such RF ICs is a wafer-level 3D monolithic integration of heterogeneous silicon ICs, in which digital CMOS, SiGe RF BiCMOS, silicon-on-insulator (SOI) and future silicon technologies can be wafer-level "packaged" with micron-size, through-die, vertical interconnects. While the manufacturing technology is not in place for such implementations, various research and development activities are underway. Key applications driving the technology are three-fold: vertically integrated memory stacks, vertical integration of microprocessor with large L2 cache memory (with reduced access time and cycle time), and smart imagers (such as CMOS imagers with signal processing at each pixel). All three applications, along with RF/microwave transceivers, are important in intelligent wireless terminals.

II. 3D IC Technology Platform

A comparison of 3D implementation of ICs with micron-size through-die interconnection is beyond the scope of the manuscript; die-to-die, die-to-wafer and wafer-to-wafer approaches are in various stages of research and development. Clearly wafer-to-wafer

Manuscript received June 4, 2004; revised July 22, 2004.
Center for Integrated Electronics Rensselaer Polytechnic Institute, Troy, New York 12180
E-mail: gutmar@rpi.edu

implementations are a longer-term solution, but also have the lowest cost for high-volume products since chip handling is minimized and vertical interconnectivity is achieved by a batch monolithic process. Various wafer-to-wafer technology platforms are under development involving oxide-to-oxide bonding [1], copper-to-copper bonding [2, 3], and dielectric adhesive bonding [4]. Our dielectric adhesive bonding approach accommodates wafer distortions and interface contaminants; in addition, a handling wafer is not required and wafers are thinned only after bonding to a host wafer.

A three-wafer stack depicting our IC technology platform is shown in Figure 1 [4, 5]. Fully processed wafers are aligned to within a micron in an EVGroup SmartView^{TM} aligner after spin coating with ~1-micron thick benzocyclobutene (BCB) and soft baking the BCB to remove volatile components. After alignment, the wafer pair is transferred to an EVG wafer bonder and bonded together with a specified ambient, temperature and pressure cycle. After bonding, the top-side donor wafer is thinned by backside grinding, polishing and selective etching. The BCB-based bond has a critical adhesion energy between 25 and 35 J/m^2 depending upon bonding conditions [6, 7], well above the 5-10 J/m^2 required for IC processing.

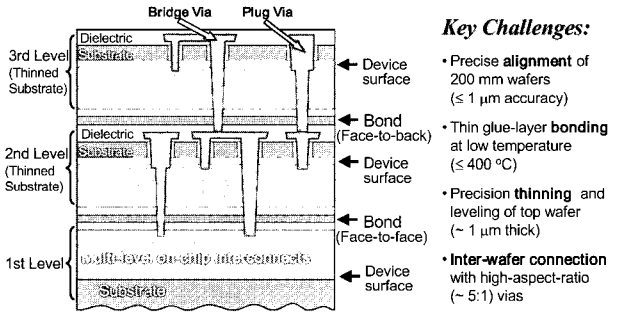
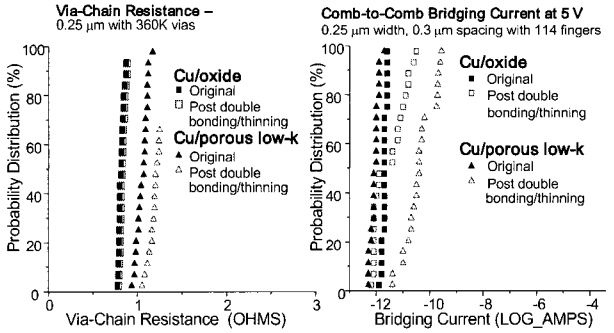


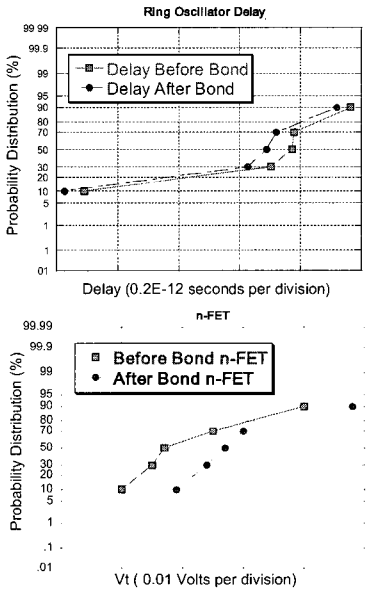
Fig. 1. Schematic of a 3D test vehicle using wafer bonding, showing bonding interface, vertical inter-wafer vias (plug- and bridge-type), and "face-to-face" and "face-to-back" bonding.

The impact of our bonding and thinning processes on IC interconnects (copper with oxide and copper with ultra-low k dielectric) has been investigated with International SEMATECH [8] and on 130 nm SOI CMOS devices and test circuits having four-level copper/ low k interconnects with Freescale [9]. The results before and after a double-bonding/thinning process described elsewhere [8] is shown for the interconnect structures in Figure 2 and for the CMOS devices and circuits in Figure 3. While the ultra-low k dielectric structure shows some change due to the fragile structure (critical adhesion energy is approximately 6 J/m^2), the changes in resistance and line-to-line leakage are small [8]. The CMOS devices and circuits have electrical change (threshold voltage, subthreshold leakage and ring oscillator delay) less than one-third of the original 10%-90% spread across the wafer [9]. A FIB-SEM cross-section of a SOI die BCB-bonded to a prime Si wafer after the double-bonding thinning process is shown in Figure 4 [9].



- Slight changes with Cu/oxide interconnects
- Larger changes with Cu/porous low-k interconnects, but within accepted limits

Fig. 2. Electrical tests of SEMATECH interconnect wafers before and after double bonding/thinning processing [8].



- Changes are less than one-third of the 10%-90% distribution spread
- No degradation after double bonding/thinning

Fig. 3. Electrical tests of Freescale CMOS SOI Cu/Low-k wafer [9].

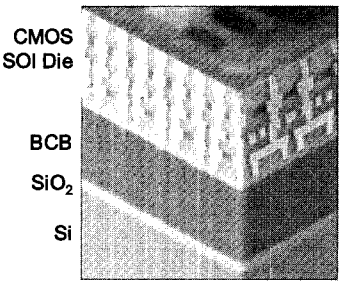
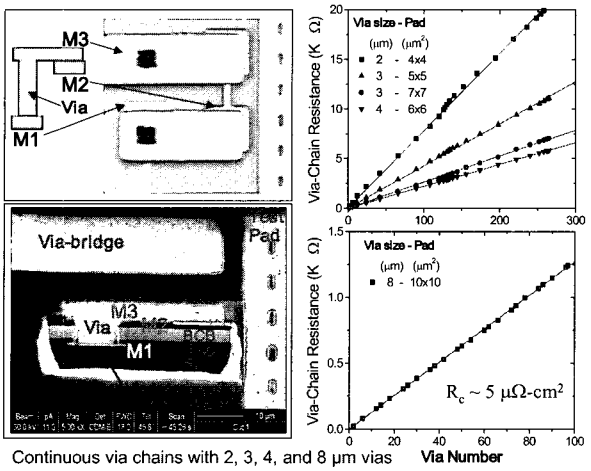


Fig. 4. FIB-SEM cross-section of SOI die BCB-bonded to a prime Si wafer after the double-bonding/thinning process [9].



• Continuous via chains with 2, 3, 4, and 8 μm vias

Fig. 5. 3D inter-wafer via-chain evaluation: optical micrograph, FIB-SEM cross section and via-chain resistance [10].

Figure 5 depicts results of an inter-wafer daisy-chain interconnect wafer pair. While the via chains have a high contact resistance due to use of a non-aggressive post-etch, pre-metal deposition clean and relatively thin interconnect lines, continuous via chains were obtained over a large percentage of the wafer. Two-to-three orders of magnitude reduction in specific contact resistivity can be expected with industrial-quality damascene patterning, thereby providing a sufficiently low via resistance for RF circuits. Wafer-to-wafer alignment is about 1 μm for the structures shown [10].

III. 3D Partitioning For Intelligent Wireless Terminals

Three-dimensional (3D) integration with micron-size, through-die vertical interconnection enables the highest volume density of signal functionality at the lowest high-manufacturing-volume cost. In order to achieve these desirable attributes, the 3D design must be partitioned to minimize fabrication costs of the individual wafers/dies, minimize power consumption and maximize 3D assembly yield. In wafer-level implementation, the partitioning is further constrained by the need for a common die size.

A few factors that impact our focus on the need for intelligent wireless terminals in the long term is the desire to integrate SiGe BiCMOS transceivers with Si CMOS memory-intensive digital processors and Si nMOS imagers. We consider a three-wafer/three-die stack for each in Figure 6. While neither have been completely designed, the performance advantage of 3D-implementation of a memory intensive architecture will be presented, as well as the design and capability of the SiGe BiCMOS operational transconductance amplifier (OTA) for a high-performance A/D converter compatible with a SiGe BiCMOS RF/microwave transceiver (possibly enabling future software radios).

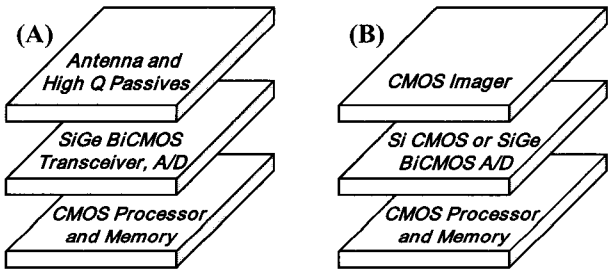


Fig. 6. Three-wafer/ three-die stack for (A) SiGe BiCMOS-based transceiver and (B) Si CMOS-based imager.

1. Memory-Intensive Architectures in 3D

The trend in microprocessor technology is an increased amount of chip area devoted to memory, particularly L2 cache. Because memory can be tolerant to isolated defects (high manufacturing yield), has low power dissipated relative to logic (heat sinking requirements minor) and needs to be located near the processor (reduced memory access time and cycle time), a through-die interconnected 3D stack is very attractive. We have developed a memory design tool, PRACTICS (Predictor of Access and Cycle Time for Cache Stack), to optimize the memory configuration for on-chip, direct-mapped and set-associative memories using analytical delay models and circuit models based upon Cadence simulations [11]. Both SRAM and DRAM models are included and the model predictions verified

for 130 nm node on-chip SRAM (for microprocessor L2 cache) and 180 nm embedded DRAM (for graphics applications). PRACTICS allows memory structure optimization in both conventional 2D ICs as well as 3D implementations with any number of memory levels in the stack. The impact of 3D implementation is summarized here, with the modeling framework more fully described elsewhere [11, 12].

We consider a 4MB memory requirement for a streaming video microprocessor with standard MPEG-2 decoding software for HDTV decoding. A conventional 2D implementation is compared to a two-wafer 3D implementation in Figure 7, both using 130 nm node technology. In the 3D implementation, the address-in channel and data-output channel between CPU and cache are connected through vertical vias instead of long wires as in the 2D implementation. PRACTICS simulation results show that the 3D implementation reduces the memory access time to 1.00 ns from 1.57 ns. Since PRACTICS sets five stages for the pipeline, the 3D implementation gives a more even delay distribution for both data and tag paths. Besides the improvement of the access speed, the 3D solution decreases the repeater number required, alleviates the wiring demand, reduces power consumption within the network interconnects and broadens the data bus width without requiring extra wafer area. From PRACTICS simulations of conventional 2D and two-wafer 3D implementations, a total of 96 repeaters have been saved in the critical path, 96 data I/O channel interconnects of 0.63 cm length have been replaced by 96 inter-wafer vias of 6 μm length, the interconnect power dissipation including the repeater power consumption has been reduced from 2.79 W to 2.13 W, and the bus width is broadened to 512 bits from 64 bits.

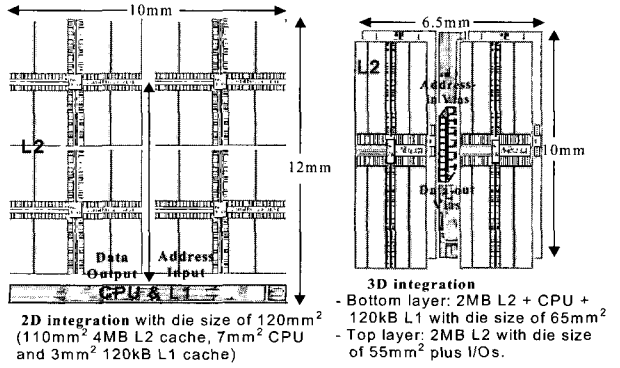


Fig. 7. Integration of streaming video processor with 4MB L2 cache at 130nm technology node [12].

With a manufacturing-robust 3D technology platform, the yield of the 3D implementation can be even higher than the 2D implementation, as the chip area is reduced. However, various manufacturing issues must be resolved as described elsewhere [5,6,12].

2. SiGe BiCMOS A/D Converters

The potential for a wafer-level 3D RF technology is discussed in this section. Two immediate applications are high-Q embedded passives (particularly for inductors) and high-performance analog-to-digital (A/D) converters with low parasitic interconnects. This section emphasizes the A/D converter since the impact of including an A/D converter with an RF transceiver IC in one wafer and combining with a digital processing IC in a second wafer is significant, particularly as higher speed A/Ds enable software radio implementations.

We believe that pipelined A/D converters implemented with a SiGe BiCMOS process as used for many Si RF ICs are desirable for high-performance, Si RF systems, implemented in either a SiP or 3D IC. In a 3D IC, embedded SiGe BiCMOS A/Ds using both SiGe heterojunction bipolar transistors (HBTs) and Si MOSFETs are attractive. A conventional pipelined A/D converter is envisioned, using gain-of-2 sample/hold (S/H) amplifiers realized with an operational transconductance amplifier (OTA) in a negative feedback loop using precise-value capacitors. High DC gain, fast settling, low noise OTAs capable of driving large sampling capacitors without sacrificing output swing are needed, as depicted in Figure 8.

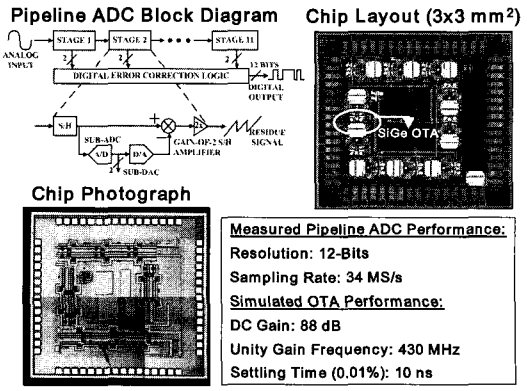


Fig. 8. SiGe BiCMOS pipeline A/D converter [13].

In recent work [13] an IBM 6HP process providing 47

GHz SiGe HBTs and 250 nm node CMOS was used to design and evaluate the necessary OTA. A cascode configuration using SiGe NPN HBTs in place of NFETs resulted in a wide-bandwidth, high-gain, fast-settling OTA shown in Figure 8. The 34 MS/s sampling rate with 12 bit resolution was limited by capacitor mismatch and the lack of self-calibration techniques.

An improved SiGe BiCMOS OTA depicted in Figure 9 uses a triple-cascode architecture and NMOS-NPN SiGe HBT Darlington inputs with cascode SiGe HBTs to achieve fast settling response, with a predicted 115 MS/s sampling rate with 12 bit resolution [14]; with digital self-calibration [15] using a 7-bit pipeline seed, 205 MS/s is predicted. The effective number of bits (ENOB) is estimated as 11.6 bits with a power consumption of 150 mW. Using the A/D figure-of-merit (FoM) from the ITRS 2003 document [16], namely

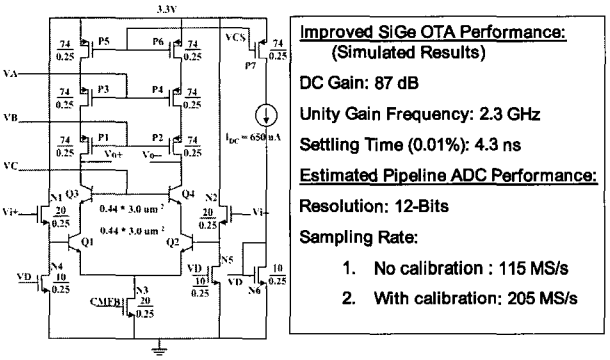


Fig. 9. Improved SiGe BiCMOS operational transconductance amplifier (OTA) with A/D FoM = 2.2×10^3 GHz/W [14].

$$FoM = \frac{2^{ENOB} \times f_{sample}}{P},$$

We obtain a conservative estimate of 2.2 x 10^3 GHz/W without self-calibration and 4.0 x 10^3 GHz/W with self-calibration, both using the 6HP process introduced in 2000. In comparison, the ITRS 2003 document predicts CMOS A/D converters to reach a FoM of 2.2 x 10^3 GHz/W in 2009 and 4.0 x 10^3 GHz/W in 2012 [16].

IV. Monolithic 3D Ic Compared To Soc And Sip Implementations

For intelligent wireless terminals, a 2D SoC seems only remotely feasible as the heterogeneous technologies needed for transceiver performance (SiGe BiCMOS), digital signal processing (Si CMOS), imaging (Si nMOS), and interface circuitry like A/D converters (Si CMOS or, as indicated in this research, SiGe BiCMOS) are very expensive to include in one process flow and on a single 2D chip. In comparison, a SiP solution, either in 2D with a multichip module or in 3D with die stacking and peripheral wire bonding, is more technologically realistic. The key limitations with SiP are potential performance reductions due to wire bonding inter-chip interconnects and manufacturing costs related to handling of individual die and passive components. While 3D die stacks with micron-size, through-wafer vias have comparable performance to wafer-level 3D implementation, the manufacturing cost will be higher due to the die handling and the die-by-die stack processing of the vertical interconnects.

Monolithic wafer-level 3D implementations are more challenging than SiP implementations initially. A viable manufacturing base is yet to be established, although recent evaluations of our technology platform indicate that the BCB bonding and thinning processes are compatible with thermal cycling to 400°C, standard autoclave environments and liquid-to-liquid thermal shock (LLTS) testing [17]. The performance advantages with short inter-wafer interconnects and low interconnectivity cost make monolithic 3D attractive for future intelligent wireless terminals, particularly as a manufacturing base becomes established for 3D integration of high density memory stacks, memory-intensive processors and smart imagers with pixel-by-pixel processing.

While the impact of such monolithic 3D technology is difficult to foresee, the possibility of software radio implementations enabled by high-speed A/D converters with high A/D FoM embedded in a RF/microwave transceiver and then stacked with a memory-intensive CMOS processor appears feasible. One can envision an intelligent wireless terminal with two 3D stacks: one with an antenna/passive, RF/microwave transceiver/A/D converter and signal processor; the other with an imager, interface circuitry and processor/memory. The information volume density of such an implementation is enormous, and the commercial realization is less than a decade away.

V. SUMMARY AND CONCLUSIONS

Three-dimensional (3D) integration with micron-size, through-die, vertical interconnectivity enables high performance heterogeneous integration of ICs with significant impact for intelligent wireless terminals of the future. A wafer-level 3D technology platform offers the lowest cost manufacturing option for high-volume products requiring high functionality. Our approach of using dielectric adhesives for bonding fully-functional, wafer-to-wafer aligned ICs, followed by top wafer thinning and copper damascene patterning for inter-wafer interconnection has been summarized with the process compatibility with 130 nm CMOS SOI devices and circuits emphasized. Performance predictions for memory intensive processors and SiGe BiCMOS pipelined A/D converters have been presented to illustrate the capability for RF IC systems in general and intelligent wireless terminals in particular. A software radio implementation is offered as a possible paradigm shift in RF IC systems, where antenna elements and integrated passives (particularly inductors) can be implemented in a TCE-matched glass wafer, with an RF transceiver and high-performance A/D converter implemented in a SiGe BiCMOS process, with a processor and memory in a Si CMOS process (maybe in two layers for memory-intensive applications).

ACKNOWLEDGEMENT

This research is partially supported through the Interconnect Focus Center for Hyperintegration, funded by MARCO, DARPA and NYSTAR.

REFERENCES

[1] K. Guarini, A. Topol, M. Ieong, R. Yu, L. Shi, D. Singh, G. Cohen, H. Pogge, S. Purushothaman, and W. Haensch, in *International Symposium on Thin Film Materials, Processes, and Reliability*, G.S. Mathad, T.S. Cale, D. Collins, M. Engelhardt, F. Leverd, and H.S. Rathore, Editors, PV2003-13, pp. 390-404, ECS (2003).

[2] A. Rahman, A. Fan, J. Chung, and R. Reif, in *1999 IEEE International Interconnect Technology Conference (IITC)*, pp. 233-235, IEEE (1999).

[3] http://www.tezzaron.com

[4] J.-Q. Lu, K.W. Lee, Y. Kwon, G. Rajagopalan, J. McMahon, B. Altemus, M. Gupta, E. Eisenbraun, B. Xu, A. Jindal, R.P. Kraft, J.F. McDonald, J. Castracane, T.S. Cale, A. Kaloyeros, and R.J. Gutmann, in *Advanced Metallization Conference in 2002 (AMC 2002)*, B.M. Melnick, T.S. Cale, S. Zaima, and T. Ohta,Editors, pp. 45-51, MRS (2003).

[5] J.-Q. Lu, Y. Kwon, J.J. McMahon, A. Jindal, B. Altemus, D. Cheng, E. Eisenbraun, T.S. Cale, and R.J. Gutmann, in *Proceedings of 20th International VLSI Multilevel Interconnection Conference*, T. Wade, Editor, pp. 227-236, IMIC (2003).

[6] Y. Kwon, J.-Q. Lu, R.J. Gutmann, R.P. Kraft, J.F. McDonald and T.S. Cale, in *Semiconductor Wafer Bonding Science: Technology and Applications*, H. Baumgart, C. E. Hunt, S. Bengtsson, and T. Abe, Editors, PV 2001-27, pp. 145-154, The Electrochemical Society, Inc.(2001).

[7] Y. Kwon, J. Yu, J.J. McMahon, J.-Q. Lu, T.S. Cale, and R.J. Gutmann, in 2004 MRS Spring Meeting, Sumposium F: *Materials, Technology, and Reliability for Advanced Interconnects and Low-k Dielectrics*, San Francisco, CA, April 12-16, 2004 (in press).

[8] J.-Q. Lu, A. Jindal, Y. Kwon, J.J. McMahon, M. Rasco, R. Augur, T.S. Cale, and R.J. Gutmann, in *2003 IEEE International Interconnect Technology Conference (IITC)*, pp. 74-76, IEEE (2003).

[9] R.J. Gutmann, J.-Q. Lu, S. Pozder, Y. Kwon, A. Jindal, M. Celik, J.J. McMahon, K. Yu and T.S. Cale, in *Advanced Metallization Conference in 2003 (AMC 2003)*, G.W. Ray, T. Smy, T. Ohta and M. Tsujimura, Editors, pp. 19-26, MRS (2004).

[10] J.-Q. Lu, A. Jindal, Y. Kwon, J.J. McMahon, K.-W. Lee, R.P. Kraft, B. Altemus, D. Cheng, E. Eisenbraun, T.S. Cale, and R.J. Gutmann, in *International Symposium on Thin Film Materials, Processes, and Reliability*, G.S. Mathad, T.S. Cale, D. Collins, M. Engelhardt, F. Leverd, and H.S. Rathore, Editors, PV2003-13, pp. 381-389, ECS (2003).

[11] A.Y. Zeng, K. Rose and R.J. Gutmann, in *International Conference on Computer Design*

(ICCD), 2004, (in press).

[12] A.Y. Zeng, J.-Q. Lu, R.J. Gutmann and K. Rose, in *Advanced Semiconductor Manufacturing Conference* (ASMC) 2004, pp. 247-251, IEEE, 2004.

[13] S. Devarajan, *M.S. Thesis*, Rensselaer Polytechnic Institute, 2003.

[14] S. Devarajan, R.J. Gutmann and K. Rose, in *IEEE International Symposium on Circuits and Systems*, May 2004 (in press).

[15] A. Karanicolas, *Ph.D. Thesis*, Massachusetts Institute of Technology, 1994.

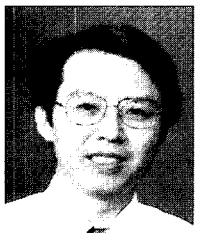
[16] *International Technology Roadmap for Semiconductors (ITRS)*: 2003 Edition, (Semiconductor Industry Association, 2003, http://public.itrs.net).

[17] S. Pozder, J.-Q. Lu, Y. Kwon, S. Zollner, J. Yu, J.J. McMahon, T.S. Cale, K. Yu and R.J. Gutmann, in *IEEE International Interconnect Technology Conference.* (IITC04), 2004 (in press).

Dr. Ronald J. Gutmann has been on the faculty at Rensselaer Polytechnic Institute since 1970, where he is currently a Professor in the Electrical, Computer, and Systems Engineering Department with teaching and research activities in the areas of semiconductor devices, monolithic microwave integrated circuit (MMIC) technology, and thin-film interconnection technology. He has authored over three hundred technical papers in these and related fields and is a Fellow of the IEEE *for contributions in microwave semiconductor technology.* He has coauthored three books on IC interconnect technology - "Chemical-Mechanical Planarization of Microelectronics Materials" (Wiley 1997), "Copper-Fundamentals for Microelectronic Applications" (Wiley, 2000), and "Chemical-Mechanical Polishing of Low Dielectric Constant Polymers and Organosilicate Glasses" (Kluwer 2002). His current research activities are in three-dimensional (3D) IC technology platforms, multilevel interconnect technology, thermophotovoltaic devices, thin-film packaging, SiC and GaN devices, and wireless communications technology.

A. Y. Zeng received the B.S. degree in electrical science with honors from Nankai University, Tianjin, China, in 1993 and Ph.D. degree in computer engineering from Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, in 1998. From 1998 to 2001, she worked in IBM China Research Lab, where she worked on human computer interaction and Chinese handwriting recognition. She is currently pursuing her second Ph.D. degree in Electrical Engineering at Rensselaer Polytechnic Institute, Troy, NY, working on wafer-level 3D cache architecture design with Prof. Gutmann and Prof. Rose.

Siddharth Devarajan received the Bachelor of Engineering (BE) degree in electrical engineering from the University of Madras, India, in 2001 and the MS degree is electrical engineering from Rensselaer Polytechnic Institute (RPI), NY, in 2003. Since 2003, he has been pursuing his Ph.D. degree at RPI, focusing on high-performance BiCMOS A/D converters. Mr. Devarajan's SiGe BiCMOS A/D converter was selected as one of the top 15 designs in the SRC SiGe Design Challenge 2002-03. During the summers of 2002 and 2004, he was an intern in the Design Modeling Group, Micron Technology, Boise, ID. He has been a student member of IEEE for over five years.



Dr. J.-Q. Lu ("James" JianQiang Lü) , received his B.S. degree from Shanxi Normal University in 1983, M.S. degree from Peking Normal University in 1986, and Dr. rer. nat. (Ph.D.) degree from Technical University of Munich in 1995. He has held research and faculty positions at a number of universities in China, Germany and the United States, the latest as Associate Research Professor in Departments of Electrical Engineer (ECSE) and Physics at Rensselaer Polytechnic Institute. He is a Senior Member of IEEE and a member of APS, MRS, and ISE. He was a Siemens Scholar in 1992-1996 and a scholar of the German Academic Exchange Program (DAAD) in 1990-

1992. He recently served as session chairs for international conferences and has been an invited speaker for many conferences, universities, and industrial organizations. He also serves as a reviewer for a number of journals. Dr. Lu's research interests are in the field of semiconductor technology including materials, devices, processing, and system integration. He has more than 90 publications in journals or conferences. Dr. Lu has worked in a broad range of fields, such as GaAs devices, GaN devices, Si bipolar device, novel field effect transistors, terahertz electronics, interconnects in Si ICs, advanced packaging, and high Tc superconductors. His current research focuses on novel electron devices, interconnect technology for gigascale integration, micro-system integration technology for microelectrical mechanical systems (MEMS), and thee-dimensional (3D) hyper-integration. Dr. Lu is one of the pioneers in the field of wafer-level 3D hyper-integration. He currently leads 3D processing technology research programs at Rensselaer, in collaborations with university colleagues, R&D institutions and industry partners.

Kenneth Rose received the B.S. degree in engineering physics in 1955 (Bronze Tablet) and M.S. and Ph.D. degrees in 1957 and 1961 from the University of Illinois, Urbana-Champaign. In 1965 he joined the faculty of Rensselaer Polytechnic Institute, Troy, N.Y., where he is Professor Emeritus in the Department of Electrical, Computer, and Systems Engineering and an active member of Rensselaer's Center for Integrated Electronics. He is a Senior Member of the IEEE and received Rensselaer's Distinguished Faculty Award in 1970. He is on the program committee of the IEEE/SEMI Advanced Semiconductor Manufacturing Conference where he and his students have presented several papers on yield and interconnect strategies. With Bibiche Geuskens he is co-author of the book, "Modeling Microprocessor Performance", published by Kluwer in 1998. Present interests include memory design modeling and mixed-signal BiCMOS design.