A Wafer Level Packaged Limiting Amplifier for 10Gbps Optical Transmission System

Chul-Won Ju, Byoung-Gue Min, Seong-Il Kim, Kyung-Ho Lee, Jong-Min Lee, and Young-il Kang

***Abstract*—A 10 Gb/s limiting amplifier IC with the emitter area of 1.5x10μm^2 for optical transmission system was designed and fabricated with a AlGaAs/GaAs HBTs technology. In this study, we evaluated fine pitch bump using WL-CSP (Wafer Level-Chip Scale Packaging) instead of conventional wire bonding for interconnection. For this we developed WL-CSP process and formed fine pitch solder bump with the 40μm diameter and 100μm pitch on bonding pad. To study the effect of WL-CSP, electrical performance was measured and analyzed in wafer and package module using WL-CSP. In a package module, clear and wide eye diagram openings were observed and the rise/fall times were about 100ps, and the output voltage swing was limited to 600mV$_{p-p}$ with input voltage ranging from 50 to 500mV. The Small signal gains in wafer and package module were 15.56dB and 14.99dB respectively. It was found that the difference of small signal gain in wafer and package module was less then 0.57dB up to 10GHz and the characteristics of return loss was improved by 5dB in package module. This is due to the short interconnection length by WL-CSP. So, WL-CSP process can be used for millimeter wave GaAs MMIC with the fine pitch pad.**

I. INTRODUCTION

High speed limiting amplifiers are widely used in optical transmission systems such as radar receiver systems, satellite communication systems. In optical transmission system application the limiting amplifier is frequently used as a main amplifier in receiver system. As a main amplifier, the limiting amplifier must have high gain and wide bandwidth with frequency response from DC range. Also low phase shift deviation and crossing point fluctuation must be insured over a wide input dynamic range to avoid degrading the sensitivity and phase margin of the receiver system including the decision circuit. The AlGaAs/GaAs HBTs were used for this application because of its high speed, high gain, uniform threshold voltage and high breakdown voltage [1-7].

In this paper, we fabricated a limiting amplifier with extremely high operation frequencies over 10GHz using AlGaAs/GaAs HBT. To assure the high performance of the GaAs MMIC, packaging design is very important. In general, MMICs are assembled on a ceramic substrate using a conventional wire bonding technique, but wire bonding technique leads to loss due to parasitic resistance and inductance of the bonding wire. Therefore the flip chip bump interconnection structure has become popular for microwave and millimeter wave IC packages [8-12]. In this paper, we interconnect 10Gbps Limiting Amplifier IC to a ceramic substrate by a flip chip WL-CSP technology. The size and pitch of pad are 70μmx100μm and 140μm respectively. So, we developed fine pitch WL-CSP process.

This paper describes the design and fabrication of 10Gbps limiting amplifier using AlGaAs/GaAs HBTs for the optical transmission system and the development of fine pitch WL-CSP process. Finally the frequency response and eye diagram of the limiting amplifier

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High Speed SoC Research Department, ETRI 161 Kajong-Dong, Yusong-Ku, Taejon 305-350, Korea
TEL: 82-42-860-5738, FAX: 82-42-860-6183
E-mail: cwju@etri.re.kr

package module are discussed.

II. CITCUIT DESIGN

A limiting amplifier must exhibit the low shift deviation between input and output signals and the constant output power over a wide input dynamic range at very high frequency. Key feature of the circuit design is a differential configuration with emitter peaking technique to achieve both low phase deviation and wide bandwidth. The block diagram of limiting amplifier is shown in Fig. 1. It is composed of a input buffer, two stage differential amplifiers for high gain, an output buffer and a feed back circuit for DC offset control. The input buffer includes an emitter follower with a 50Ω thin film resistor to ensure input impedance matching. The main amplifier employs a modified Cherry-Hopper(C-H) circuit to obtain high gain and wide bandwidth[13].

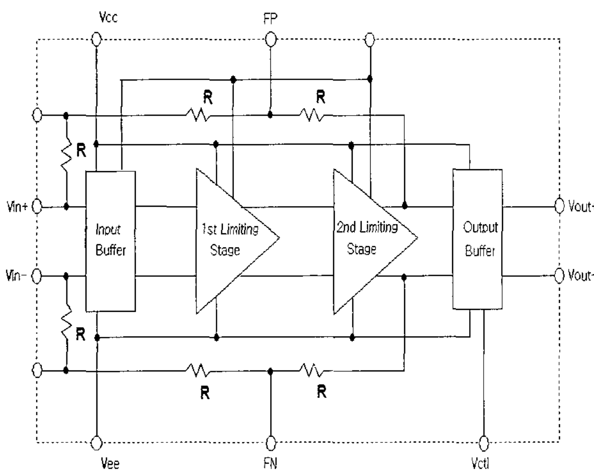


Fig. 1. Block diagram of limiting amplifier

The modified C-H circuits is basically composed of two stage differential amplifiers, output buffer and a feedback resistor, where the feedback resistor is connected to the second amplifier through an emitter follower. To increase the bandwidth and reduce the phase deviation, the output buffer uses an emitter peaking circuit which consists of series resistor and capɛ itor at the emitter. Each circuit operates with its own reference current source to reduce the crosstalk. Single power supply is used with the maximum power consumption of 1.5W. This circuit was optimized by SPICE to determine the bias points at each circuit block.

III. IC FABRICATION AND PACKAGING

The limiting amplifier with the emitter area of 1.5x10 μm^2 was fabricated using NPN GaAs IC fabrication process. The epitaxial wafer structure grown by MOCVD on a 3 inch GaAs substrate include an InGaAs emitter cap layer(800Å), an AlGaAs emitter layer (2000Å), a GaAs base layer(700Å) and GaAs collector layer(4000Å). HBTs were fabricated by self alignment process, where the spacing between emitter and base was 0.25μm. Ti/Pt/Au were deposited by electron beam evaporator for the ohmic contact of base and emitter. Ni/Ge/Au/Ti/Au were deposited by electron beam evaporator for the ohmic contact of collector. These ohmic metals were alloyed simultaneously at 375°C for 10 seconds in H_2/N_2 atmosphere after metal deposition. The fabrication process employs a mesa structure with semi-self alignment process. NiCr thin film resistors with 20Ω/sq and metal- insulator-metal capacitor were used.

The size and pitch of pad are 70μm x100μm and 140 μm respectively. So, we developed fine pitch WL-CSP process. The process sequence was as follows.

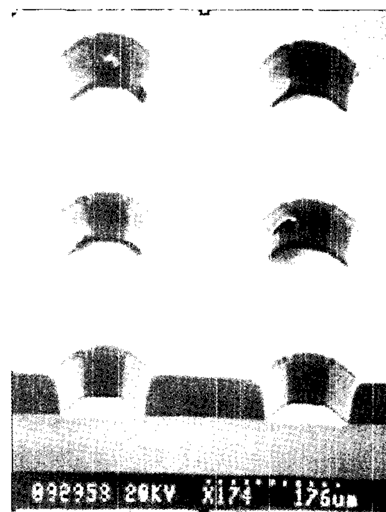


Fig. 2. Cross sectional SEM showing via

The 0.1μm thick layer of Ti was sputtered as the adhesion and barrier layer, followed by a 0.2μm of Cu, seeding layer for electroplating. A photoresist was spin

coated to a thickness of 60μm and patterned by a contact aligner with an I-line source. This exposure process yielded a steep walled via opening. After exposure, oxygen plasma was used to remove the resist residues inside the via openings.

Figure 2 shows a SEM photograph of vias.

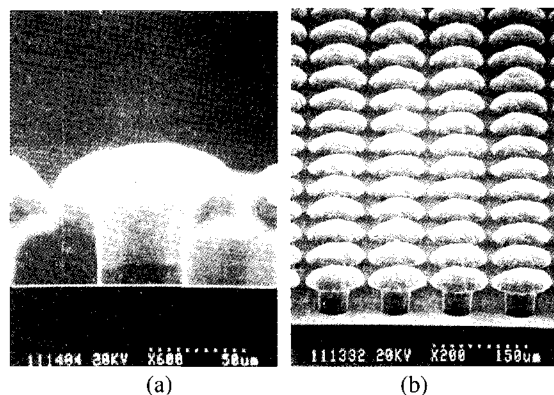
Prior to electroplating, the wafer surface was treated with a copper plating solution in a plating system to remove any copper oxide. The 5μm thick layer of Cu was electroplated in a Cu bath, then the eutectic solder bump was plated in a solder bath. The temperature of the plating solution was controlled at 25°C. The bumping plating process was performed in two consecutive steps to increase thickness uniformity. In the first step, plating was conducted at a low current density of $10mA/cm^2$, then the current density was increased to $50mA/cm^2$. At a low current density, the plating rate was low, so a thin layer was uniformly plated over the entire surface of the wafer to achieve plating uniformity.

After plating, the photoresist was striped off and the Ti/Cu seed layer was etched with diluted HF and Cu etchant, respectively.

A mushroom bump formed when the resist thickness was lower than the desired bump height. Fig. 3 shows a SEM photograph of a mushroom-shaped solder bump with a 40/100μm diameter/pitch, which was plated at a current density of $50mA/cm^2$ for 30 min. Fig. 3(a) shows that the bump length over-plated laterally and the bump height over-plated vertically were the same. The bump height, which was measured with α-step, was 70μm, so it was over-plated by about 32%. Fig. 3(b) shows a SEM photograph of a solder bump array with relatively uniform bump heights and there was no touching between nearest bumps.

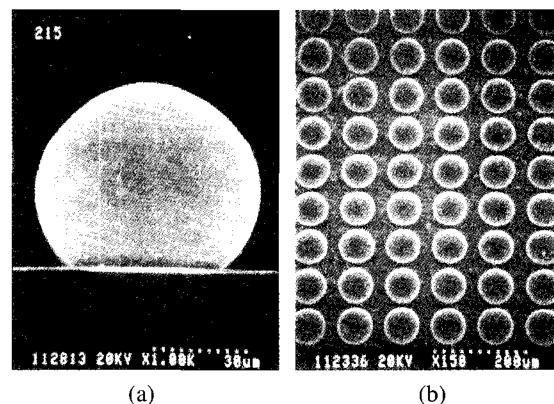
Before the reflow process, a Ti/Cu seed layer was etched with diluted HF and Cu etchant respectively, then the flux was coated over the solder bumps. A reflow process was performed at 220°C on the eutectic solder bump of Fig. 3(a). The solder bump shape after the reflow process depends on the bump size and height due to surface tension and capillary attraction during reflow. The flux was removed after the reflow.

Figure 4 shows a SEM photograph of the ball-shaped bump after reflow, where the spherical solder bump has a uniform bump height and the spherical solder bump has a symmetrical structure. In Fig.4 (a), the diameter of the reflowed solder bump increased from 44μm to 46μm and the height of the reflowed solder bump decreased from 70μm to 53μm. From this, we know that there is no difference in the bump bottom diameter, but there is a considerable reduction in height.



(a) (b)

Fig. 3. SEM showing eutectic solder bump with 40μm diameter/100μm pitch (a) Cross section (b) Plane surface



(a) (b)

Fig. 4. SEM showing eutectic solder bump with 40μm diameter/100μm pitch after reflow (a) Cross section (b) Plane surface

In Fig.4 (b), the solder bumps after the reflow process are spherical, their size is uniform and there is no touching between nearest bumps. From Figs. 3 and 4, we can estimate that to obtain high density bumps, we can decrease the bump pitch, but it can result in touching between the nearest bumps.

The touching between the nearest bumps can occur during the over-plating procedure rather than the reflowing procedure because the mushroom diameter formed by over-plating is larger than the reflowed bump diameter.

Fig. 5 shows the microphotograph of limiting amplifier IC with eutectic solder bump electroplated on

pad. In this photograph, solder bumps look like dark balls. Clearly, the solder bump doesn't collapse beyond the pad bottom area during the reflow process.

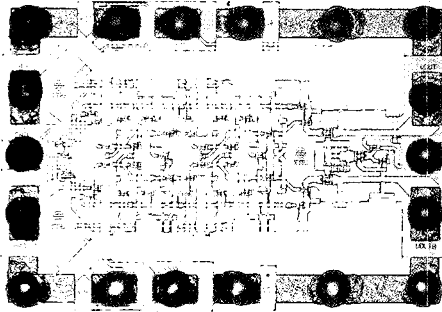


Fig. 5. Microphotography of wafer level packaged limiting amplifier IC

Figure 6 shows the cross sectional microphotograph of limiting amplifier IC with eutectic solder bumps electroplated on pad. The average height of bump was about 60μm and the uniformity was 3%. Fig. 7 shows the limiting amplifier module with IC mounted on ceramic substrate using flip chip bump interconnection.

Fig. 6. The cross sectional microphotograph of limiting amplifier IC with eutectic solder bumps electroplated on pad

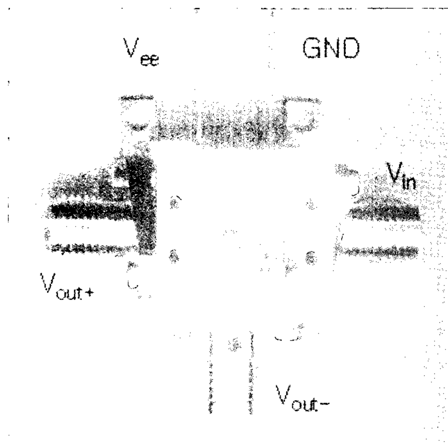
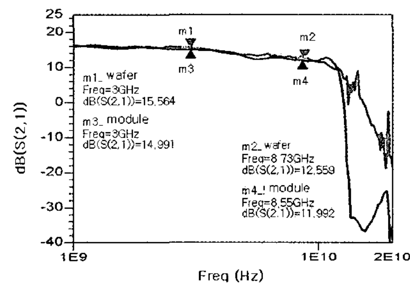


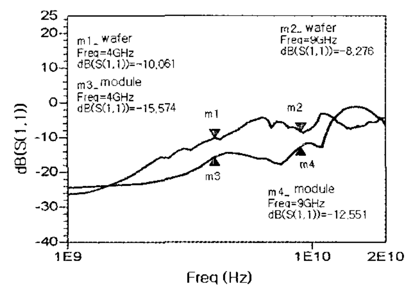
Fig. 7. 10Gbps limiting amplifier module

IV. Electrical Performance

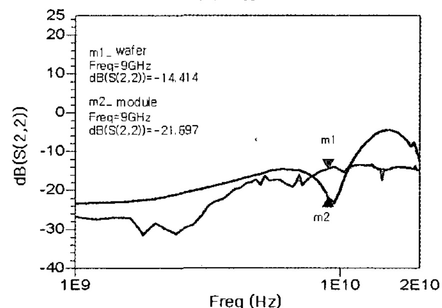
Prior to the packaging, the limiting amplifier ICs are tested on wafer with RF proves. Corresponding RF characteristics are shown in Fig. 8. In Fig. 8(a), the small signal gain on wafer is about 15.56dB and f_{-3dB} is about 8.73GHz. With increasing frequency, the gain decreases slowly with broadening bandwidth up to 10GHz. Limiting amplifier chip is packaged by wafer level packaging technology and mounted on ceramic substrate. The amplifier module with SMA connectors is tested for frequency response and limiting performance. Fig. 8(a) shows the frequency dependence of the limiting amplifier package module. The small signal gain on module is about 14.99dB and f_{-3dB} is about 8.55GHz. With increasing frequency, the gain decreases slowly with broadening bandwidth up to 10GHz.



(a) S_{21}



(b) S_{11}



(c) S_{22}

Fig. 8. S-parameter of 10Gbps limiting amplifier

It is found that the small signal gain difference between wafer and package module is 0.57dB and it is kept up to f_{-3dB}. But, the characteristics of return loss was improved in package module.

Reflection characteristics is improved by matching in the substrate. S_{11} was improved more than 5dB up to f_{3dB}. S_{22} was improved by 5 dB between 8GHz and 10GHz. It is known that the characteristics of IC is degraded by 15~25% in packaging process. But, there was small difference in the small signal gain between chip and package module. The improvement of electrical characteristics was due to the impedance matching and the short interconnection length by WL-CSP. It was assumed there was small impedance mismatching in chips, so transmission lines of ceramic substrate were designed with tapered GCPW (Grounded Coplanar Waveguide) structure for impedance matching.

Fig. 9 shows a eye diagram of the limiting amplifier package module. Eye patterns of the limiting amplifier was measured using a Anritsu Pulse Pattern Generator and a HP Sampling Oscilloscope. Clear and wide eye diagram openings were observed and the rise/fall times were about 100ps. The output voltage swing was limited to $600mV_{p-p}$ with input voltage ranging from 50 to 500mV.

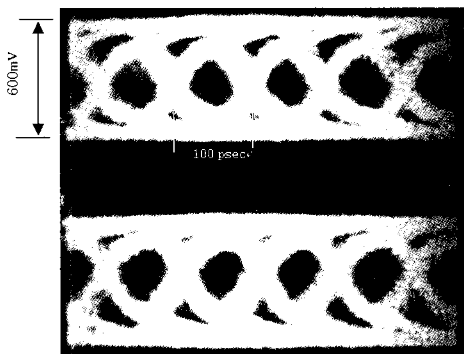


Fig. 9. Eye diagram of the limiting amplifier package module

V. CONCLUSIONS

10Gb/s AlGaAs/GaAs HBT limiting amplifier was designed and fabricated. In this study, we developed WL-CSP process and could get fine pitch bumps with the 40μm diameter and 100μm pitch. For packaging, thin film ceramic substrate was manufactured and chips were interconnected on the ceramic substrate using flip chip interconnection instead of conventional wire bonding. The Small signal gains in wafer and package module were 15.56dB and 14.99dB respectively. It was found that the difference of small signal gain in wafer and package module was less then 0.57dB up to 10GHz and the characteristics of return loss was improved by 5dB in package module. This is due to the short interconnection length by WL-CSP. Therefore WL-CSP process can be widely used to packaging of the millimeter wave devices with fine pitch pad less than 100μm.

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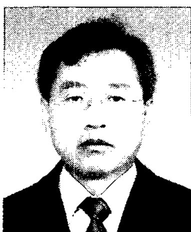
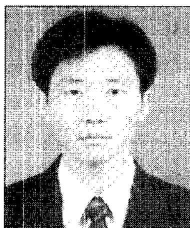


Chul-Won Ju received the B.S degree in chemical engineering and M.S. degree in electronics engineering from the Pusan National University, Korea in 1977 and 1989, respectively, and Ph. D degree in electrical engineering from the Chonbuk National University, Korea in 2003. From 1979 to 1982, he was with the institute of Gold Star Precision Company as researcher. In 1982, he joined the ETRI(Electronics and Telecommunications Research Institute), Taejeon, Korea, where he is currently principal member of engineering staff. His current research activities are focused on high performance packaging and interconnection technologies. His main research interests include thin film, WLP (Wafer Level Package), MCM(Multichip Module), flip chip and reliability of semiconductor.

Byoung-Gue Min received his B. S. and M. S. degrees in Metallurgical Engineering from Yonsei University in Seoul, Korea, in 1991 and 1993, respectively. He earned his PhD degree in Materials Science and Engineering from Yonsei University in Seoul, Korea, in 1998. He is with Electronics and Telecommunications Research Institute (ETRI), Korea, as a member of Senior Research Staff, where he has been engaged in research on compound semiconductor MMIC developments for wireless telecommunications and THz optical communications systems, from 1998.

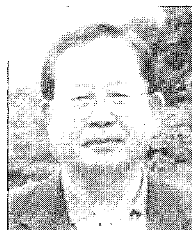
Seong-Il Kim was born in Kangkyeong, Korea, in 1970. He received the B. S. degrees in electrical engineering from Hanyang University, and M. S. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Korea, in 1998 and 2000, respectively.
From 2000, he was with Electronics and Telecommunications Research Institute (ETRI), Korea, as a member of Research Staff, where he has been engaged in research on opto-electronic and high-speed digital IC designs.



Kyung Ho Lee received his B. S. and M. S. degrees in Metallurgical Engineering from Seoul National University in Seoul, Korea, in 1980 and 1982, respectively. He earned his PhD degree in Materials Science and Engineering from Stanford University in Stanford, USA, in 1989. From 1989 to 1996, he was with Electronics and Telecommunications Research Institute (ETRI), Korea, as a member of Senior Research Staff, where he has been engaged in research on advanced compound semiconductor device fabrication. From 1996 to 1998, he was with Eaton Semiconductor

Korea, where he has been the Director of Applications heading troubleshooting and development of Eaton ion implanter-related processes and hardware. Since 1998, he rejoined ETRI as a member of Principal Research Staff of Compound Semiconductor Department to manage national research projects on micro-/millimeter-wave MMIC developments for wireless telecommunications and THz optical communications systems. He also headed in establishing the basis of foundry service of ETRI's 4" compound semiconductor fabrication facility. He is currently leading up the InP IC team. His research interests are on the development of advanced compound semiconductor devices and IC's fabrication their system applications.

Jong-Min Lee has been a senior researcher at Electronic Telecommunications Research Institute (ETRI) since 2001. He is responsible for the research and development of InP/InGaAs HBT and broadband MMIC. He received the B.S. degree in material science and engineering from Korea University, Seoul, Korea, in 1995. And he received the M.S. and Ph.D. degrees in material science from Korea University, Seoul, Korea, in 1997 and 2001, respectively. His research interests include GaAs- and InP-based HBT device and MMIC.



Young Il, Kang He was born at Seoul, Korea and his educational backgrounds consist of B.S. degree of Electrical Engineering from the Seoul National University in 1966 , M.S. degree of Electrical Engineering from the Fairleigh Dickinson University in 1991 and Ph.D. degree of Computer Science from the Korea University in 1996. He started his professional carrier at the Fairchild Semiconductor (Korea) in 1969 and worked as a product engineer until he moved to ETRI in 1979. Developed the wafer fabrication process for 32k/64k PROM at the early stage of ETRI and continued his work for the development of various ICs for the telecommunication industry up to now.