MOSFET Model HiSIM Based on Surface-Potential Description for Enabling Accurate RF-CMOS Design

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Abstract — **The origin of the phenomena, obstructing circuit performance in the RF operating regime, as well as their modeling will be discussed. The applied surface-potential-based modeling allows self-consistent description of all phenomena important for accurate circuit simulation, as demonstrated with the MOSFET model HiSIM.**

Index Terms — **MOSFETs, High-Frequency Operation, Circuit Simulation Model, HiSIM, Surface Potential**

I. INTRODUCTION

Though RF MOSFET circuits are becoming realistic, the RF-circuit simulation is still a challenge due to many reasons. One serious reason is that the development of the appropriate tools for RF designs is still behind the demand [1]. Another important reason is the lack of model accuracy required for the simulation [2]. Demand for accurate prediction of non-linear device characteristics is also a tough requirement due to deficiency of sufficient understanding for advanced MOSFETs including measurements. A lot of progress has been made to catch up to the requirements in both the modeling aspect and in providing simulation tools. Here our discussion focuses on the modeling aspect.

A better circuit model has less model parameters, without compromising accuracy. The model parameters should be connected to device parameters and should be measurable independently. To realize these requirements model development trends to follow device physics, namely to describe device performances with the potential distribution along the channel instead of applied voltages as conventionally done [3], [4], [5]. The self-consistent charge-based model with the surface-potential description will be demonstrated to offer the basis for successfully performing the foreseeable challenges as for example with HiSIM (Hiroshima-university STARC IGFET Model), the MOSFET model developed according to this concept for the first time [6], [7]. Here phenomena to be modeled and their modeling approaches are described in three aspects. First, modeling of basic MOSFET characteristics, including normal DC and AC characteristics, is briefly summarized. Next, modeling for small-signal analysis is discussed on the basis of an equivalent circuit model. A newly developed non-quasi-static model for large-signal analysis will be demonstrated in the third part, where the most efforts are given for deriving the analytical description suitable for circuit simulation without increasing simulation expense.

Sepecial emphasis is given to clarify that the accurate modeling of the DC characteristics and their parameter extraction are key prerequists for all RF-specific modeling approaches.

II. MODELING OF BASIC MOSFET CHARACTERISTICS

Under high-frequency operation, non-linear phenomena such as harmonic distortion as well as carrier response delay become serious for reliable circuit performance prediction [8]. Here all such device phenomena are demonstrated to be determined by the carrier dynamics under equilibrium condition, which are in principle observed in the normal I-V characteristics [3]. Thus a good model for describing I-V characteristics is a prerequisite for all device modeling. In the surface-potential-based modeling all equations describing device characteristics are functions of the surface potential instead of applied voltages as in the conventional models. To derive an anayltical description for the potential distribution along the channel induced by applied voltages, we introduce two approximations. One is the charge-sheet approximation assuming zero thickness of the inversion charge, and the other is the gradual-channel approximation assuming smooth potential increase along the channel [10], [9]. These approximations allow to derive an analytical formulation for all device performances as a function of surface potentials at the source side ϕ_{S0} and the drain side ϕ_{SL} [6]. The surface potentials are obtained by solving the Poisson equation iteratively. In spite of the iteration in HiSIM, calculation time is not longer than with BSIM3v3 [11]. The reason is that a single equation is valid for all applied bias conditions, which keeps the HiSIM model equations simple. Fig. 1 shows the surface potential calculated by HiSIM as a functions of applied voltages. These surface-potential values are very sensitive to device parameters

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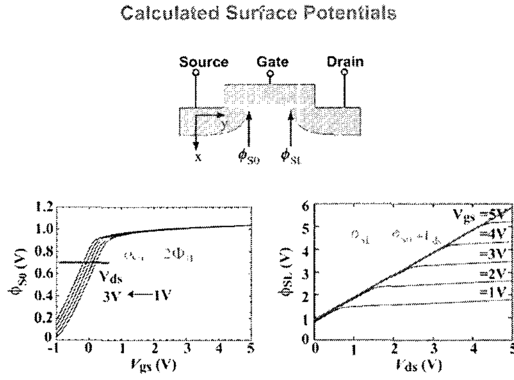

Fig. 1. Calculated surface potentials by HiSIM at the source side ϕ_{S0} and at the drain side ϕ_{SL} are also depicted.

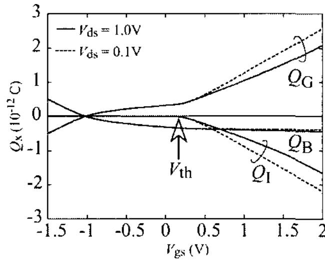

Fig. 2. Calculated charges induced in the gate (Q_G), in the bulk (Q_B), and in the inversion layer (Q_I) as a function of the gate voltage V_{gs}.

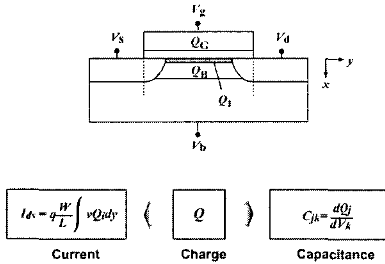

Fig. 3. Concept of the charge-based model.

such as the substrate impurity concentration. Calculated charges on MOSFET nodes are shown in Fig. 2. These charges are origin of all device characteristics. By integrating the channel charge Q_I with the velocity v the current equations are derived. The derivatives of these charges yield the capacitances as depicted in Fig. 3. The gradual-channel approximation is valid only for the non-saturative region. Beyond ϕ_{SL} the potentail increases steeply, forming the pinch-off condition. Beyond the pinch-off region the channel is practically treated as shortened by ΔL, referred to as the channel-length modulation [12]. The whole potential distribution from ϕ_{S0} to $\phi_{S0}+V_{\rm ds}$ via ϕ_{SL} and $\phi(\Delta L)$ is the measure applied in the modeling instead of applied voltages, as schmatically shown in Fig. 4. The unknown surface potential value at the junction between the channel and the drain contact $\phi(\Delta L)$ is extracted with measured channel conductance $g_{\rm ds}$ as a function of $V_{\rm ds}$ [7].

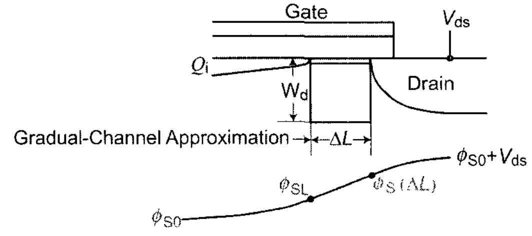

Fig. 4. Schematics depicting correlations among physical quantities in the pinch-off region.

1. I-V Characterisitcs & Their Derivatives

The final drain current ($I_{\rm ds}$) is written as

$$I_{\rm ds} = \frac{W_{\rm eff}}{L_{\rm eff} - \Delta L}\frac{\mu}{\beta}\Bigg\{ C_{\rm ox}(\beta V'_G + 1)(\phi_{SL} - \phi_{S0}) - \frac{\beta}{2}C_{\rm ox}({\phi_{SL}}^2 - {\phi_{S0}}^2) - \frac{2}{3}\sqrt{\frac{2\epsilon_{\rm Si} q N_{\rm sub}}{\beta}}\Big[\{\beta(\phi_{SL} - V_{\rm bs}) - 1\}^{\frac{3}{2}} - \{\beta(\phi_{S0} - V_{\rm bs}) - 1\}^{\frac{3}{2}}\Big] + \sqrt{\frac{2\epsilon_{\rm Si} q N_{\rm sub}}{\beta}}\Big[\{\beta(\phi_{SL} - V_{\rm bs}) - 1\}^{\frac{1}{2}} - \{\beta(\phi_{S0} - V_{\rm bs}) - 1\}^{\frac{1}{2}}\Big]\Bigg\} \quad (1)$$

$$V'_G = V_{gs} - V_{fb} + \Delta V_{th} \quad (2)$$

where $W_{\rm eff}$, $L_{\rm eff}$, μ, β, $C_{\rm ox}$, $\epsilon_{\rm Si}$, q, and $N_{\rm sub}$ are the channel width, the channel length, the carrier mobility, the inverse of the thermal voltage, the gate capacitance, the silicon permittivity, the electron charge, and the bulk impurity concentration, respectively. The term V'_G includes the flat-band voltage (V_{fb}) and the threshold voltage shift from a long-channel transistor ΔV_{th}, which accounts for the short-channel effect $\Delta V_{th,SC}$ as well as the reverse-short-channel effect $\Delta V_{th,RSC}$. If $\phi_{S0} = 2\Phi_B$ and $\phi_{SL} = 2\Phi_B + V_{\rm ds}$ are assumed, the $I_{\rm ds}$ equation reduces to the conventional description as a function of applied voltages. Calculated $I_{\rm ds}$ and their derivatives are shown in Fig. 5 in comparison with measurements. Since the surface potential description includes both the drift and diffusion contributions, a natural transition from the subthreshold region to the inverison region is achieved. In the subthreshold region, where the diffusion contribution dominates, the device parameters such as the substrate impurity concentration mostly determine the device characteristics. Under the inversion condition, where the drift component dominates, the carrier mobility governs the characteristics. In Fig. 6, calculated output resistances $R_{\rm out}$ are compared with measurements.

The short-channel effect $\Delta V_{th,SC}$ in Eq. (2) is caused by the lateral electric field increase along the channel. The Gauss law leads to the relation [13]

$$E_x + W_d\frac{dE_y}{dy} = -\frac{Q_s}{\epsilon_{\rm Si}} \quad (3)$$

where y is the direction parallel to the channel, E_y is the lateral electric field, and $Q_S = (Q_B + Q_I)$ is the total charge den-

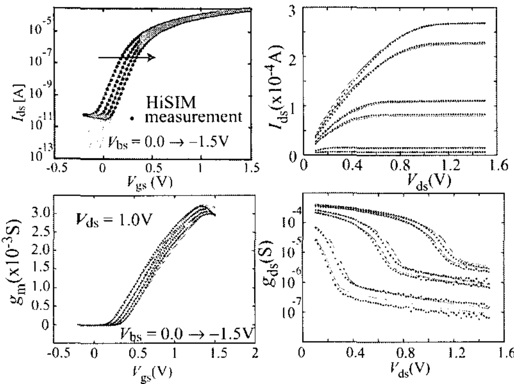

Fig. 5. Comparison of calculated I-V characteristics and their drivatives with measurements. The gate length is fixed to $10\mu m$.

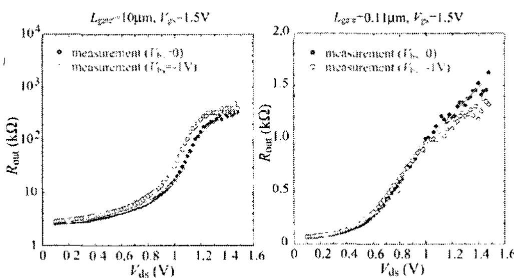

Fig. 6. Comparison of calculated R_{out} characteristics for $L_{\rm gate} = 0.11\mu m$ and $L_{\rm gate} = 10\mu m$.

sity induced in the substrate. W_d is the depletion-layer thickness. For preserving the same amount of Q_S, fulfilling threshold condition, smaller vertical fields (E_x) are sufficient due to the additional contribution of the E_y gradient. The magnitude of dE_y/dy is extracted from the measured $V_{\rm th}$ shift $\Delta V_{\rm th,SC}$ in comparison to a long-channel device.

In Fig. 7, the $V_{\rm th}$-$L_{\rm gate}$ characteristics shows $V_{\rm th}$ increases as $L_{\rm gate}$ is reduced. This threshold voltage shift $\Delta V_{\rm th,RSC}$ is included in $\Delta V_{\rm th}$ in Eq. (2). One important origin of the reverse-short-channel effect is the pocket implantation. By approximating a linearly changing lateral pocket profile along the channel, an analytical $V_{\rm th}$ equation is derived by determining the threshold condition from the entire carrier concentration in the channel [14]. Length of extention into the channel and maximum concentration of the pocket profile are extracted from the measured $V_{\rm th}$-$L_{\rm gate}$ dependence. Calculated $V_{\rm th}$ values are compared with measurement in Fig. 7. The surface-potential based model does in particular not require a $V_{\rm th}$ parameter in the MOSFET descriptions as can be seen in Eq. (1). For consistency, $\Delta V_{\rm th}$ ($\Delta V_{\rm th,SC}$+$\Delta V_{\rm th,RSC}$) is included in the Poisson equation to calculate the surface potential change due to the short-channel effect. This causes the $V_{\rm ds}$ dependence of ϕ_{S0} and ϕ_{SL}. It has to be emphasized that the impurity concentration is the model parameter, which influences all device characteristics such as the mobility through the surface potential values.

The carrier mobility plays an important role in accurate simulation of the $I - V$ characteristics beyond threshold condition. The universality in the low field mobility has been proved even for advanced MOSFET technologies [15]. The high field mobility has been developed by Caughey and Thomas empirically in [16] as

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_y}{V_{\rm sat}}\right)^{BB}\right)^{\frac{1}{BB}}} \quad (4)$$

where V_{sat} is the maximum velocity, which has been measured to be 6.5×10^6cm/s [17], and BB is a model parameter (BB=2 for electrons and BB=1 for holes). However, the value is exceeded with reduced $L_{\rm gate}$, an effect called the velocity overshoot. In advanced MOSFETs the quantum mechnical effect and the poly-gate depletion effect are becoming obvious in capacitance measurements [18]. Including all such phenomena in a self-consistent way is a key for accurate simulation of $I - V$ characteristic with reduced number of model parameters [7].

2. Harmonic Distortion

If the model is consistent and all model parameters are accurately extracted from measurements, other measured quantities should be reproduced without any additional model parameters. The harmonic distortion is one subject for verification of this statement.

Fig. 8 proves that the low frequency harmonic distortion is indeed correctly reproduced without additional parameters or adjustments [19]. The symbols are measurements and dashed lines are calculated result with a parameter set extracted only from normal measured I-V characteristics. The solid lines show the result with a tuned molibity value by 3%, which has an unobservable influence on the I-V characteristics.

3. Noise Characteristics

In RF systems, noise is a major issue obstructing circuit performance. Usually small unwanted signals in a system are caused in a different operating region, e. g. the low-frequency $1/f$ noise cause changes in high-frequency characteristics through upconversion [1]. We focus on the noise induced in the MOSFET device. Here two important noise mechanism have to be considered for advanced MOSFETs; the $1/f$ noise and the thermal noise induced by the drain current. The origin of the $1/f$ noise has been understood theoretically as the fluctua-

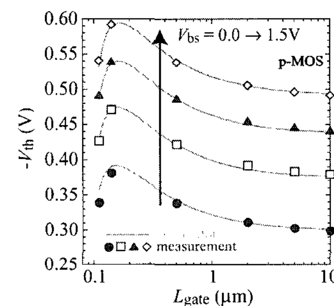

Fig. 7. Pocket implanted threshold voltage V_{th}-L_{gate} characteristics. Calculated V_{th} with HiSIM in comparison to measurements.

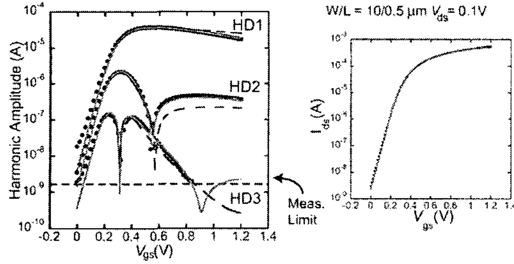

Fig. 8. Comparison of calculated harmonic distortion with measurements (dotted). The dashed lines are results with a parameter set extracted from measured I-V characteristics and the solid lines are with a 3% tuned mobility parameter. The difference of the parameter values cannot be seen in the I-V characteristics.

tion in the number of channel carriers due to trapping/detrapping processes at the gate-oxide interface, as well as by the mobility fluctuation. The description of the $1/f$ noise spectrum density $S_{I_{\rm ds}}$ for the drift-diffusion model is obatined by integrating the noise source, namely the carrier density, along the channel [20]. For this purpose two model paremters are introduced, which represent the contribution of the mobility fluctuation and the ratio of the trap density to the gate-oxide attenuation coefficient. The $1/f$ noise is mainly determined by the trap density and the carrier density along the channel. Fig. 9 compares calculated $1/f$ noise characteristics with measurements at f = 100Hz. Good agreement of the calculated $1/f$ noise to measurements for any applied voltage and any channel length demonstrates that the characteristics of the $1/f$ noise is indeed reproduced by above described modeling on the basis of the carrier concentration along the channel, which can be extracted again from measured I-V characteristics.

Accurate thermal noise measurements are very difficult. Only recently sufficiently accurate measurements have been reported [21], [22]. The applied thermal-noise model in HiSIM is based on the channel conductance [23]. Thus additional model parameters are not needed also in this case. The origin of the thermal noise enhancement observed for short-channel transistors is explained differently by different authors. The HiSIM approach is to consider the potential distribution along the channel explicitly [22]. Corresponding simulated noise coefficients are shown in Fig. 10, which justifies the modeling approach and proves the consistency of the HiSIM model. Our simulation results demonstrate that the thermal noise is still governed by the equilibrium carrier transport.

4. Intrinsic Capacitances

In addition to the current, capacitances play also important roles under high-frequency operation. Thus accuracy of intrinsic capacitances as well as extrinsic capacitances has to be guaranteed. Intrinsic capacitances are derived directly from the terminal charges as depicted in Fig. 3. Explicit equations as functions of the surface potentials are obtained by the derivatives of charges with respect to node voltages. Thus intrinsic capacitances require no additional model parameter, and device parameter values extracted with normal I-V measurements determine

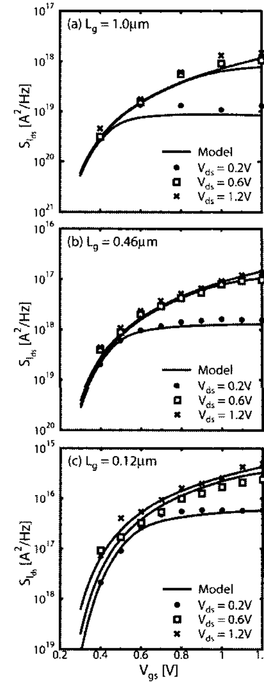

Fig. 9. Calculated $1/f$ noise characteristics in comparison with measurements. Only the trap density is required as model parameter, to obtain validity for all gate lengths [20].

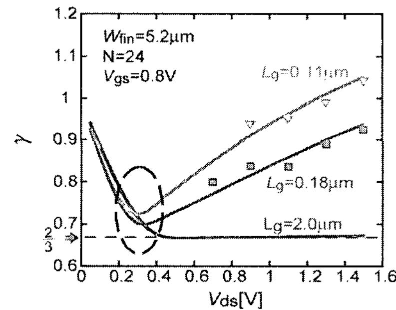

Fig. 10. Calculated thermal noise coefficients γ and measurements as a function of the drain voltage $V_{\rm ds}$ for various gate lengths $L_{\rm g}$ [22].

the capacitance values as well. In addition to the 9 normal intrinsic capacitances two capacitances play important roles in advanced MOSFETs. One is the gate overlap capacitance to the source and drain. Especially the voltage dependent overlap capacitance at the drain, which is also derived as a function of surface potentials [7], strongly influences the RF performances. For short-channel transistors the lateral electric field at the drain induces an additional intrinsic capacitances C_{Q_y} as shown in Fig. 11 [24]. The model equation of the capacitance C_{Q_y} is also written as a function of surface potentials.

Fig. 12 summarizes the model-parameter set required for circuit simulation with HiSIM.

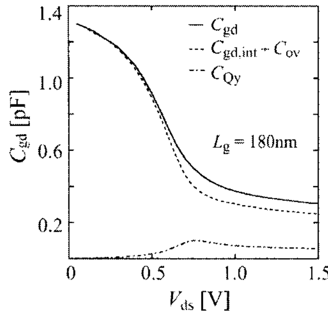

Fig. 11. Calculated lateral-field-induced capacitance, induced in the region where the high lateral electric field occurs [24].

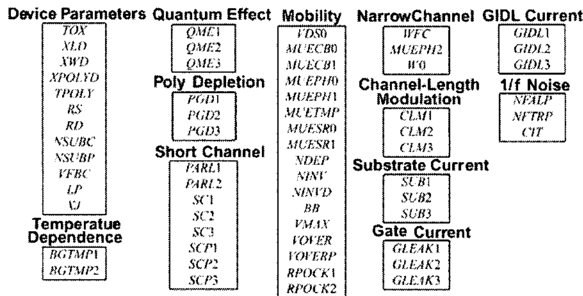

Fig. 12. Summary of basic model parameters of HiSIM required for circuit simulation.

III. Small-Signal Analysis

The small-signal analysis considers the case where input sinusoidal voltage variation is sufficiently small so that the small output current variations can be expressed by a linear relation

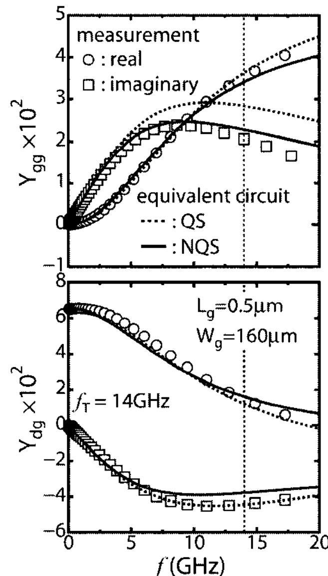

Fig. 13. Measured (open symbols) and calculated y parameters with the non-quasi-static model (solid curves) and the quasi-static model (dashed curves) for the gate length of 0.5μm [27]. The vertical dotted lines denote the cut-off frequency of the device studied.

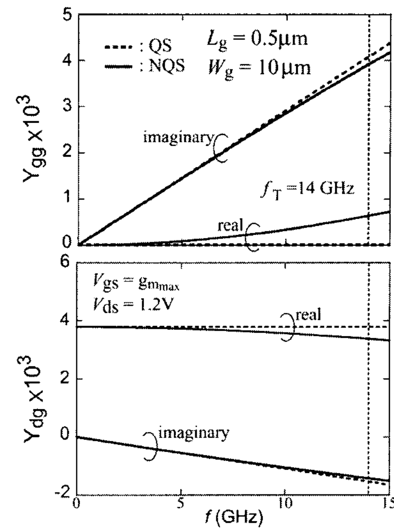

Fig. 14. Comparison of calculated intrinsic y parameter values with the quasi-static model and the non-quasi-static model. The vertical solid lines denote the cut-off frequency.

as [8]

$$\Delta I_{ds} = g_m \Delta V_{gs} + g_{mb} \Delta V_{bs} + g_{ds} \Delta V_{ds} \quad (5)$$

where conductances g_x are derivatives of I_{ds} with respect to corresponding node voltages. The small-signal analysis, investigating the high frequency characteristics, is characterized with a two-port analysis, where a 2×2 admittance matrix represents the carrier response. The matrix elements are called Y-parameters, and analytical descriptions have been derived under low frequency f as

$$Y_{gg} = jfC_{gg} \quad (6)$$

$$Y_{dg} = g_m - jfC_{gd} \quad (7)$$

where R_g is the gate resistance, C_{ij}s are capacitances, and g_m is the transconductance. The real part is expected to be zero and the gradient of the imaginary part as a function of f to be the gate capacitance C_{gg} for Y_{gg}, as well as the gradient to g_m and C_{gd} for Y_{dg}. Thus, it can be stressed from the equations that the accurate modeling of DC and AC characteristics and their parameter extraction are keys even for accurate calculation of the Y parameter characteristics. Calculated Y parameters are compared with measurements in Fig. 13. For the calculation, the gate resistance was fitted to reproduce the measurements. The calculations done under the quasi-static (QS) approximation, ignoring the carrier transit delay, show clear deviations in the high-frequency regime in spite of accurate DC and AC modeling.

An explicit non-quasi-static MOSFET model for the small-signal analysis has been developed by solving the continuity equation in an analytical way in connection with HiSIM [25]. The model based on the surface-potential description enables to predict the high-frequency response for any bias conditions precisely. The model enables to calculate the Y-parameter values under the QS condition. Fig. 14 compares the calculation results under the QS and NQS conditions. It is clearly seen that

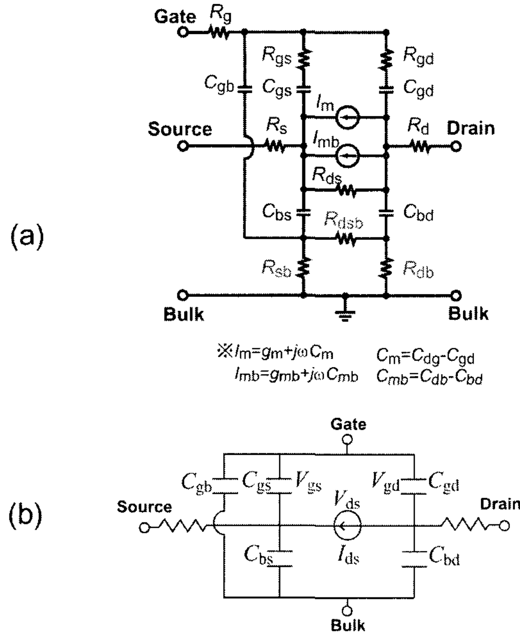

Fig. 15. (a) Improved equivalent circuit for high-frequency applications. The Elmore resistances R_{gs} & R_{gd} and the bulk resistance R_b are introduced. (b) Basic equivalent circuit of a MOSFET originally developed by Meyer.

$R_{\rm g}$ plays important roles under the high-frequency operation. It is also seen that the NQS contribution becomes obvious only beyond the frequency of 1/3 of cut-off frequency, and that the contribution is much smaller than believed previously.

To improve the simulation accuracy caused by the NQS effect for circuit simulation, additional elements are introduced in the equivalent circuit as shown in Fig. 15a together with the original Meyer model in Fig. 15b. The high Elmore resistance at the drain side $R_{\rm gd}$ describes the carrier delay [26], and the bulk resistance $R_{\rm b}$ describes the extrinsic capacitive coupling [27]. Calculation results with the improved equivalent circuit are included in Fig. 13. Since the NQS effect is not drastical up to 1/3 of the cut-off frequency, the additional elements included in the equivalent circuit are verified to be sufficient to reproduce the measured Y parameters.

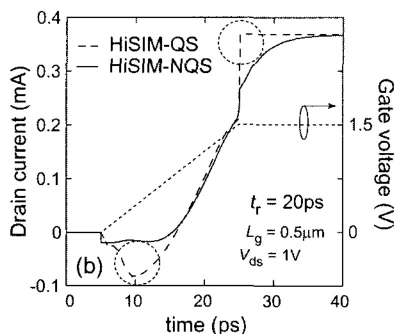

Fig. 16. Comparison of the HiSIM calculated transient $I_{\rm ds}$ behavior to the 2D simulation result under high-frequency switching operation [28].

IV. Large-Signal Analysis

Circuit simulators solve transient characterisitcs of cirucits in the form written as

$$I_a(t) = I_a(0) - \frac{dQ_a}{dt} \tag{8}$$

derived under the quasi-static approximation, ignoring the carrier transit delay along the channel. $I_a(0)$ denotes the spontaneous current response to the applied voltage on node a without delay. Till now the incorporation of the delay is carried out mostly phenomenologically by segmenting the channel into n quasi-statically described pieces, and recombining each segmented MOSFET. This NQS model for the large-signal analysis is shown to give a suitable prediction of the high-frequency behavior of the intrinsic device response [21]. Shortcomings are simulation time and simulation is not straightforward due to the segmentation of the channel. A more exact model has been developed including the real transit time τ as demonstrated in Fig. 16 [28]. The delay τ is again a function of surface potentials. The main effort is given to modify Q_a in Eq. (13) including the carrier transit delay [29]. Thus even the carrier deficit in the channel can be represented, which occurs at the initial stage of the switching-on without suffering from an increase of the simulation time [28].

V. Summary And Conclusions

Observed phenomena obstructing RF-circuit application of MOSFETs and their modeling are discussed. Modeling based on the surface potential description preserves self-consistency among models of different device characteristics. Thus the conventional parameter extraction from measured I-V characteristics results in accurate simulation results up to 1/3 of the cut-off frequency without inclusion of high-speed non-quasi-static effects.

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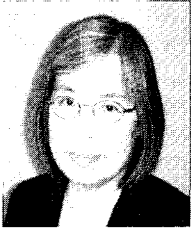

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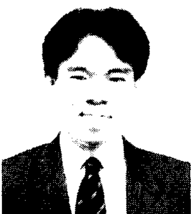

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