High f_T 30nm Triple-Gate $In_{0.7}GaAs$ HEMTs with Damage-Free SiO_2/SiN_X Sidewall Process and BCB Planarization

Dae-Hyun Kim, Seong-Jin Yeon, Saegn-Sub Song, Jae-Hak Lee*, and Kwang-Seok Seo

Abstract—**A 30 nm $In_{0.7}GaAs$ High Electron Mobility Transistor (HEMT) with triple-gate has been successfully fabricated using the SiO_2/SiN_x sidewall process and BCB planarization. The sidewall gate process was used to obtain finer lines, and the width of the initial line could be lessened to half by this process. To fill the Schottky metal effectively to a narrow gate line after applying the developed sidewall process, the sputtered tungsten (W) metal was utilized instead of conventional e-beam evaporated metal. To reduce the parasitic capacitance through dielectric layers and the gate metal resistance (R_g), the etched-back BCB with a low dielectric constant was used as the supporting layer of a wide gate head, which also offered extremely low R_g of 1.7 Ohm for a total gate width (W_g) of 2x100 m. The fabricated 30nm $In_{0.7}GaAs$ HEMTs showed V_{th} of -0.4V, $G_{m,max}$ of 1.7S/mm, and f_T of 421GHz. These results indicate that InGaAs nano-HEMT with excellent device performance could be successfully fabricated through a reproducible and damage-free sidewall process without the aid of state-of-the-art lithography equipment. We also believe that the developed process will be directly applicable to the fabrication of deep sub-50nm InGaAs HEMTs if the initial line length can be reduced to below 50nm order.**

Index Terms—**InP, HEMT, InGaAs/InAlAs, nanometer, sidewall, triple-gate, BCB, f_T**

Manuscript received May 30, 2004; revised June 15, 2004.
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I. INTRODUCTION

An InGaAs/InAlAs high electron mobility transistor (HEMT) on an InP substrate has shown excellent frequency characteristics due to enhanced electron mobility and an increased conduction band discontinuity (ΔE_c) [1-3]. Recently, the device microwave characteristics have been improved considerably by reducing the gate length (L_g) to the nanometer scale, by adopting a highly strained In_XGaAs channel ($x>0.53$) and two-step recess etching technology [4, 5]. According to the recent work by the Fusitsu group, the current gain cut-off frequency (f_T) of 562GHz with L_g of 25nm and the strained $In_XGa_{1-X}As$ ($X=0.7$) channel was reported [6].

The conventional e-beam lithography equipment with an acceleration voltage of 30 kV and a Tungsten (W) or LaB_6 filament would offer a minimum feature scale of about 100nm. To reduce the device gate length (L_g) to the sub-100nm scale, the state-of-the-art e-beam lithography equipment with high resolution will be needed. The side-wall process has been widely used to overcome these lithography limitations, particularly in CMOS device fabrications[7]. The fine pattern is obtained by the formation of a side-wall spacer through the sequence of dielectric etching, dielectric redeposition and dielectric etch-back. Among the various process parameters, the percentage of overetching in the etch-back step predominantly affects the shape of the final side-wall spacer. Due to the step coverage problem in dielectric redeposition, precise control of the overetching time is impossible, and thus the ambiguity of the shape of the final side-wall spacer would be problematic in this process.

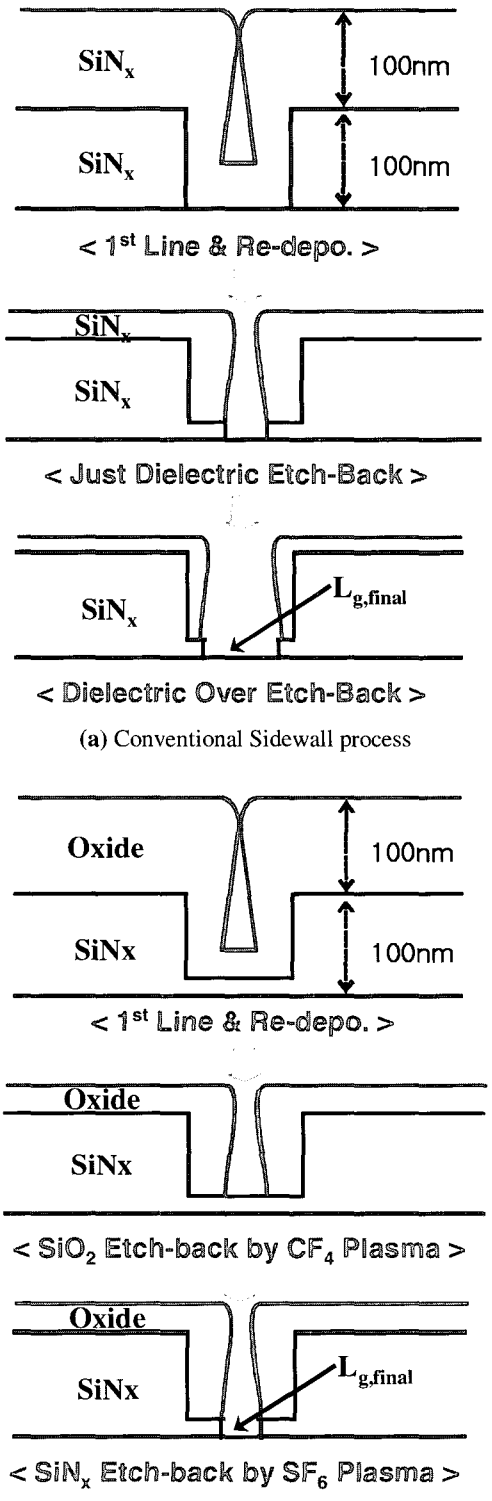
In this study, a highly reproducible side-wall gate process was developed in order to overcome the lithography limitation. The ambiguity of the shape of the final side-wall spacer was resolved by using SiN_x/SiO_2 dual dielectric layers and appropriate etching gas [8]. Using the developed sidewall gate process, a 30nm gate could be obtained reproducibly. To fill the Schottky gate metal effectively in the narrow line opening having a high aspect ratio of above 3, sputtered tungsten (W) metal was used instead of conventional e-beam evaporated metal. With the newly developed process features, 30nm $In_{0.7}GaAs$ HEMT's were successfully fabricated and characterized.

II. Damage-Free And Reproducible SiO2/SiNx Sidewall Gate Process

Figure 1(a) shows the procedure of the conventional sidewall gate process which includes first line definition, dielectric redeposition and dielectric etch-back. The final gate length (L_g) is reduced according to the dimensions of the two sidewall spacers. Because the shape of the final sidewall spacer easily changes with the duration time of dielectric etch-back, the fine control of the final gate length (L_g) is very difficult.

Figure 1(b) represents our new sidewall process, which utilizes two dielectric layers of SiN_x and SiO_2, and two plasma gas sources for the purpose of dielectric dry etching. After the redeposited SiO_2 was etched by CF_4-based plasma, the residual SiN_x was etched by SF_6-based plasma. **Figure 2** shows typical SF_6 based plasma etching characteristics for PECVD grown SiO_2 and SiN_x. Here, the SF_6-based plasma has a high etching selectivity for the SiO_2 layer, which prevents the shape of the final side-wall spacer from being reduced during overetching. This feature does ensure the reproducibility of the proposed side-wall gate process. The actual etch selectivity for the oxide layer by the SF_6 plasma was over 20 in this process.

Figure 3 shows the over-all SEM images of the proposed side-wall gate process in detail. After applying the newly developed sidewall process, the initial line could be reduced to a half scale. In addition, SF_6 gas has the advantage of little plasma-induced damage during the etching process, which can allow enough overetching time without any degradation of the carrier transport property [8].



(a) Conventional Sidewall process

(b) Newly developed sidewall Process

Fig. 1. Procedure of Sidewall process

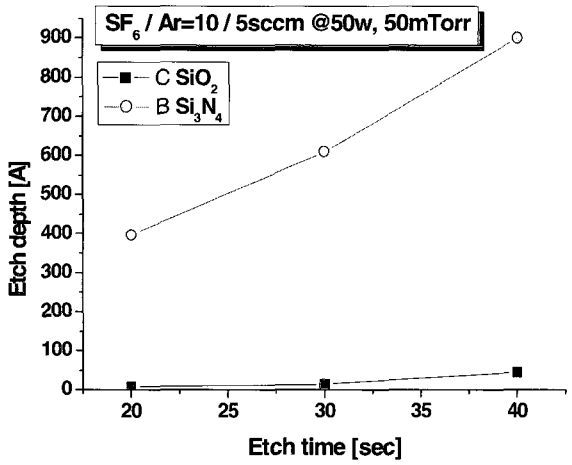
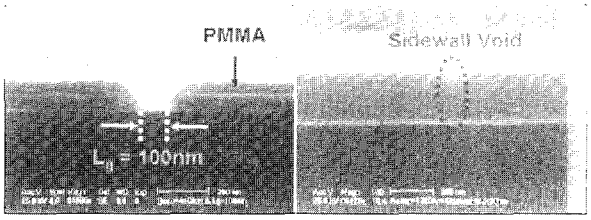


Fig. 2. SiO_2 and SiN_x etch results by SF_6 based plasma



(a) 1st line Definition **(b)** SiO_2 Re-deposition

(c) SiO_2 Etch-back **(d)** Final SiN_x Etch-back

Fig. 3. The over-all SEM Photograph of Sidewall process

III. Novel 30nm Triple-Gate Technology

To reduce the final line length after the sidewall process, it is much more effective to lessen the initial line length. To achieve this goal, thin PMMA with the thickness of 500Å was used. In accordance with the reduction of the e-beam resist thickness, it is possible to reduce the quantity of e-beam dose, which results in the resolution of finer line length through dose optimization. **Figure 4** shows the over-all SEM images for the 30nm sidewall gate process in detail. Using thin PMMA and the dose optimization method, the initial line length with the thickness of 60 to 70nm could be obtained. In addition to the decrease of the initial line length, a sloped etching profile with anisotropy of 75 degrees also aids in conformal second oxide deposition, which resulted in more greatly reduced final line length after etch-back of the re-deposited dielectric layer. With the above sidewall gate process, the obtained final gate length after dielectric etch-back was 30nm.

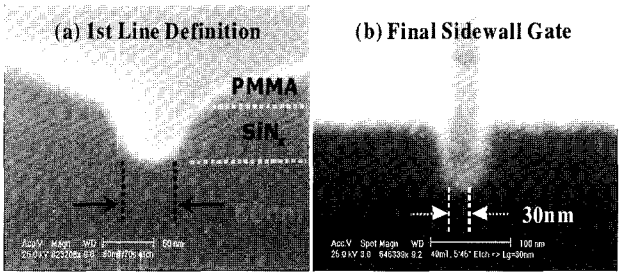


Fig. 4. SEM for 30nm SiO_2/SiN_x Sidewall Process

The procedure for the fabrication of the triple-gate structure is shown in **Fig. 5**. After filling the sputtered tungsten (W) metal in the narrow gate line, a second gate metal (Ti/Au) with the thickness of 1500Å was evaporated and lifted off, and then unnecessary tungsten metal was removed by SF_6-based RIE. Here, SF_6-based RIE also has etching selectivity for oxide over tungsten, thus it is possible to do some degree of overetching. Next, planarization using a BCB layer with a low dielectric constant (ε_r) of 2.75 was carried out. Finally, the third gate layer, typically wide gate head, was defined using a bilayer of PMMA and copolymer, and then Ti/Au with a metal thickness of 5000Å was evaporated and lifted off. **Figure 6** shows the SEM images of the fabricated 30nm triple-gate structure.

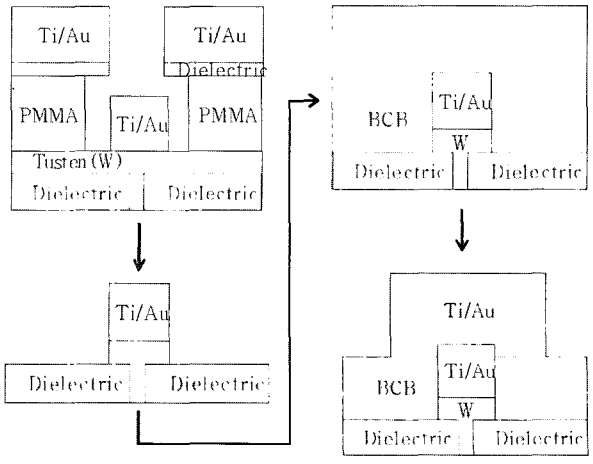


Fig. 5. Schematic procedures for BCB-assisted triple-gate process

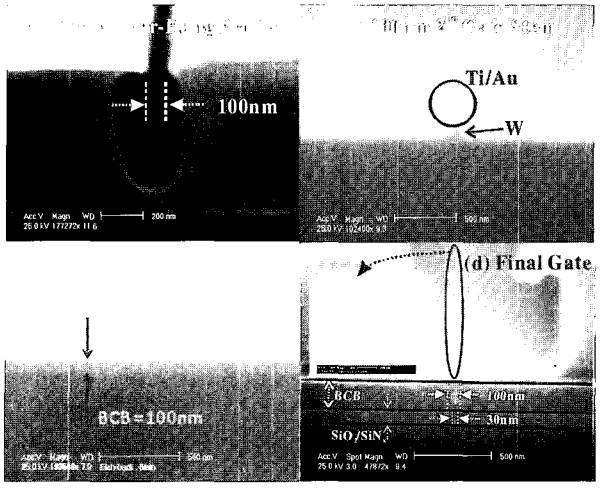


Fig. 6. SEM images for triple-gate metal process

IV. FABRICATION OF 30NM IN0.7GAAS HEMTS

Pseudomorphic InGaAs/InAlAs HEMT epitaxial layers with an InP etch-stopper were grown by solid-source molecular beam epitaxy on 3-inch semi-insulating InP substrates. The detailed structures are shown in **Fig. 7**. An 8nm strained $In_{0.7}GaAs$ channel was adopted to enhance the carrier transport property, and a 4nm undoped InP layer acted as an etch-stopper in the selective gate recess etching process. The results of Hall measurement indicated a 2-DEG (two dimensional electron gas) density of 3 × 10^{12} /cm^2 with a low field Hall mobility of 11,000 cm^2/V-s at room temperature.

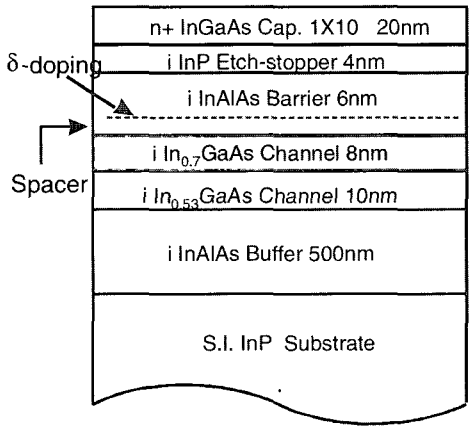


Fig. 7. Cross Section of InGaAs/InAlAs HEMTs

Device fabrication began with mesa isolation down to the InAlAs buffer layer by wet chemical etching using a H_3PO_4 : H_2O_2 : H_2O mixture. For the S/D ohmic contacts, an image reversal photoresist was used to achieve a well-defined overhang profile for lift-off, and then ohmic contacts were formed by Ni/Ge/Au metallization through e-beam evaporation and alloyed in H_2 ambient after passivation of the remote PECVD (R-PECVD) grown 70nm SiN_x pre-passivation.

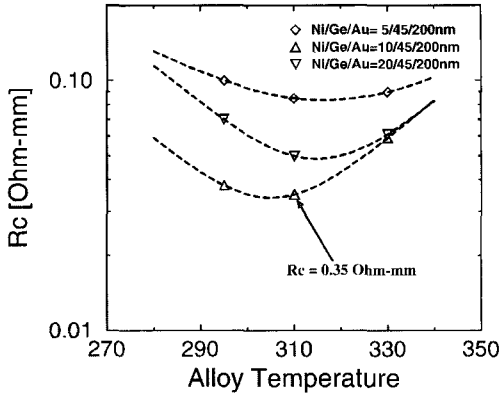


Fig. 8. Ohmic Contact Resistance (R_c) versus the ally temperature for various Ni/Ge/Au metal systems

Figure 8 shows the optimization results of S/D ohmic contact for various metal systems. The ohmic metal system of Ni/Ge/Au(10/45/160nm) had a significantly reduced contact resistance (R_c) of below 0.035Ω-mm, which is acceptable for the sub-50nm gate device. The developed SiN_x/SiO_2 side-wall process was applied to define a 30nm gate foot, and then selective gate recess etching using a mixture of citric acid and H_2O_2 was performed. The developed BCB-assisted triple-gate process was applied to form a 30nm gate structure. The overall device fabrication procedures are summarized in **Fig. 9** [9].

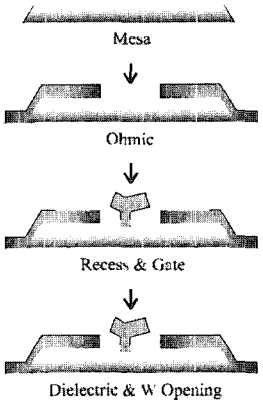


Fig. 9. The over-all HEMT fabrication procedures

V. DC AND MICROWAVE CHARACTERISTICS

Two types of 30nm InGaAs HEMT devices such as an InP-Schottky barrier device and an InAlAs-Schottky barrier device by means of Ar-based RIE etching with low plasma-induced damage characteristics were fabricated. The fabricated 30 nm HEMTs were characterized by on-wafer measurement for their DC and microwave performances. The output I-V transfer curves for the two HEMT devices were plotted in **Fig. 10**. The 30nm HEMTs with an InP-Schottky barrier exhibit V_{th} of -0.85V and $G_{m,max}$ of 1.75S/mm. The 40nm HEMTs with an InAlAs-Schottky barrier show somewhat higher $G_{m,max}$ of 1.69S/mm and lower V_{th} of -0.3V due to the etching of the InP etch-stopper by Ar plasma. On comparing the performance of these two devices, the short channel effect was found to be considerably suppressed for the InAlAs-Schottky barrier device. This was due to the improvement of the aspect ratio, namely, the ratio of the device gate length to the distance between the channel and the Schottky contact. Quantitatively, 40% improvement of the aspect ratio led to an approximately 2.7-fold increase of voltage gain (G_m/G_o).

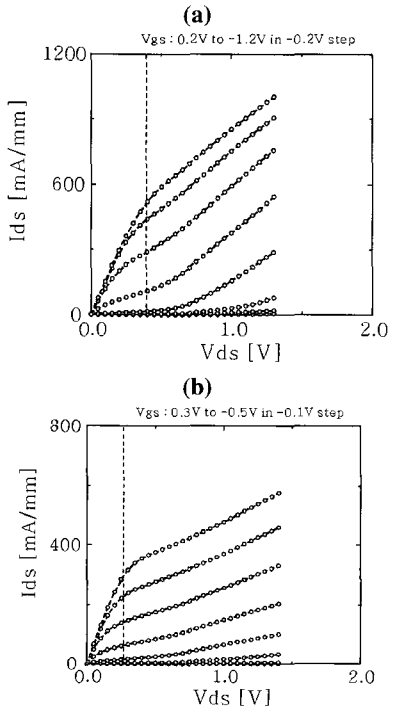


Fig. 10. (a) *I-V* transfer curve for a device with InP-Schottky gate and (b) *I-V* transfer curve for a device with InAlAs-Schottky gate.

Figure 11 shows the reverse and forward Schottky-gate characteristics for the two types of HEMT devices. Because the InP layer has a low Schottky barrier height (SBH) of typically 0.35 eV compared with the $In_{0.52}AlAs$ layer which has SBH of about 0.6 eV, a similar behavior of the off-state breakdown characteristics was appeared. These can also be explained by the increase of the forward turn-on voltage (V_{on}) of the InAlAs-Schottky device.

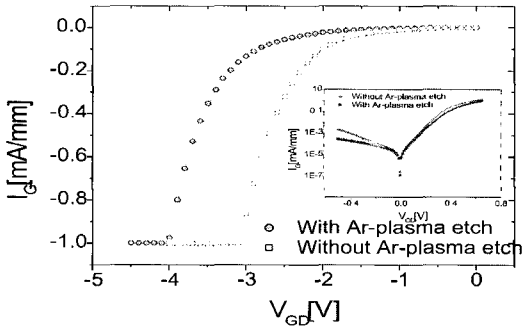


Fig. 11. The Schottky Gate Characteristics. A device with InAlAs schottky shows BV_{GD} of – 4.0V and gate turn-on voltage (V_{on}) of + 0.45V

The small signal scattering parameters (S-parameters) of 2×50μm InGaAs HEMTs were measured using on-wafer probing and the 8510C network analyzer (1~40GHz). Shown in **Fig. 12** was the plot of H_{21} versus the frequency biased near the maximum transconductance ($G_{m,max}$) region. Extrapolating H_{21} to zero gain with a -6 dB/octave slope, an estimation of 421 GHz was obtained for f_T. We believe that this result indicates an excellent sub-100nm InGaAs HEMTs with little short channel effects without the aid of state-of-the-art e-beam lithography equipment.

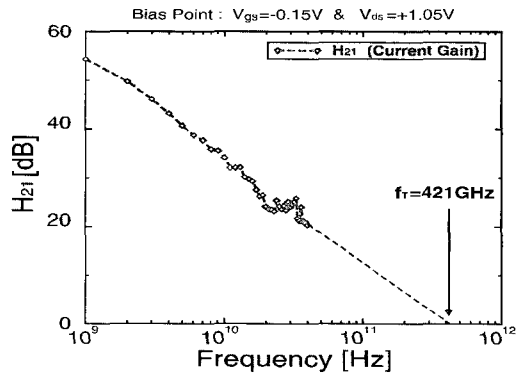


Fig. 12. Typcial Current gain H_{21} versus measured frequency for the 30nm InGaAs HEMT's biased near the peak transconductance ($G_{m,max}$)

VI. Conclusion

We have fabricated a 30nm $In_{0.7}GaAs$ HEMT with triple-gate metal using the sidewall process and BCB planarization. Fine lines measuring 30nm could be obtained by the dual SiO_2/SiN_x sidewall processes and the triple-gate metal process assisted by the BCB layer with low dielectric constant (ε_r) did result in a good metal-filling property in the narrow gate line with a high aspect ratio, a stable metal structure stability and a reduced gate fringing parasitic effect. The developed process was applied to fabricate 30nm InGaAs HEMTs which exhibited $G_{m,max}$ of 1.7S/mm and f_T of 421GHz. We demonstrated that 30nm InGaAs HEMTs could be successfully fabricated reproducibly through our damage-free sidewall process without the aid of state-of-the-art lithography equipment.

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Acknowledgments

This work was financially supported by the National Program for Tera-level Nano-devices of the Ministry of Science & Technology of Korea as one of the 21-Century Frontier Programs. The authors would like to thank Dr. Jiang Jian at MBE Technology for the epitaxial-layer growth of InGaAs/InAlAs HEMTs

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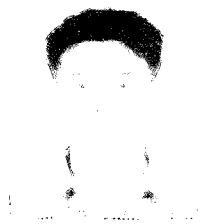

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