Analysis of Process Parameters to Improve On-Chip Linewidth Variation

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Abstract—**The influencing factors on the OPC (optical proximity correction) results are quantitatively analyzed using OPCed L/S patterns. 3σ values of proximity variations are measured to be 9.3 nm and 15.2 nm for PR-A and PR-B, respectively. The effect of post exposure bake condition is assessed. 16.2 nm and 13.8 nm of variations are observed. Proximity variations of 11.6 nm and 15.2 nm are measured by changing the illumination condition. In order not to seriously deteriorate the OPC, these factors should be fixed after the OPC rules are extracted. Proximity variations of 11.4, 13.9, and 15.2 nm are observed for the mask mean-to-targets of 0, 2 and 4 nm, respectively. The decrease the OPC grid size from 1 nm to 0.5 nm enhances the correction resolution and the OCV is reduced from 14.6 nm to 11.4 nm. The enhancement amount of proximity variations are 9.2 nm corresponding to 39% improvement. The critical dimension (CD) uniformity improvement for adopting the small grid size is confirmed by measuring the CD uniformity on real SRAM pattern. CD uniformities are measured 9.9 nm and 8.7 nm for grid size of 1 nm and 0.5 nm, respectively. 22% improvement of the CD uniformity is achieved. The decrease of OPC grid size is shown to improve not only the proximity correction, but also the uniformity.**

Keywords: proximity, OCV, OPC, grid size

I. INTRODUCTION

The shrinkage strategy to obtain the high speed performance and the low production cost in semiconductor devices has accelerated the reduction rate of design rules. The optical resolution limit of the lithography technology is confronted by this behavior. In order to overcome this limit, the resolution enhancement techniques (RETs) are introduced but the small photolithographic margin is unavoidable. [1-4]Hence, the process variations constituting the total photolithographic margin are required to be analyzed and tightly controlled. It is commonly known that the critical dimension (CD) uniformity of the in-field is induced by the variations of process dependent factors such as mask, exposure tool, CD measurement tool, and so forth.[5] Recently, it is reported that the portion of each process variation of intra field CD uniformity is analyzed in a 90 nm node device using the Monte Carlo method.[6]

While several pitches are permitted in memory devices, arbitrary pitch sizes are used in logic devices. The CD uniformity characterizes the process margin in memory devices. In logic device, the on-chip linewidth variation (OCV) including CD uniformity and optical proximity effect is introduced because the CD control over arbitrary feature and pitch sizes are required. The optical proximity correction (OPC) is necessary to compensate the CD variation for arbitrary pitch sizes.[7-9] The OPC is mainly influenced by the optical and the material conditions. If these external parameters were fixed, the factors contributing to the correction accuracy need to be analyzed. These elements include the accurate model generation, the proper model selection, mean to target (MTT), and the measurement, *etc.*

Manuscript received May 30, 2004; revised June 21, 2004.

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The grid size used to generate the OPC rule is one of the critical factors to be controlled. The minimum resolution inherent to the model is limited by the grid size. The resolution could be enhanced by reducing the grid size. In a 90 nm node device, the error portion contributed to in-field CD uniformity is approximately calculated to be 10% at 1 nm grid size. On the other hand, the error portion for an 80 nm node device is anticipated to be larger than 20%.[6] Considering the occupied portion of the grid size effect, OPC grid size below 1 nm-grid size is required in an 80 nm node device. The wafer CD variation could be decreased by adopting the smaller grid size and the error portion be reduced. The OPC using the reduced grid size can more elaborately correct the CD variation by enhancing the resolution and is expected to improve the CD uniformity.

In this paper, the proximity dependencies on the process parameters such as photoresist (PR), post exposure bake (PEB), illumination, MTT, and OPC grid size will be assessed and discussed for L/S patterns.

II. EXPERIMENTS

An attenuated phase shift mask of 6% transmittance is exposed using ArF scanner at the numerical aperture of 0.75 and annular illumination condition. The data needed to extract the model is obtained using line and space (L/S) patterns with assist features (AFs) inserted. These sub-resolution AFs are introduced to minimize the proximity effect by densifying patterns for large pitch sizes. In addition, the forbidden area could be avoided and the overall process margin can be improved. [10]

Figure 1 represents the schematic diagram for the AF generating rule and CD behavior curves as a function of the pitch size. No AFs are generated for the pitch size less than 320 nm and one AF is introduced at the center of the lines between the pitch sizes of 320 nm and 500 nm. Two AFs are inserted for the pitch size larger than 500 nm but the constant interval of 110 nm is maintained between AF and line. AF sizes used in this experiment are 40 nm and determined by considering pattering and masks manufacturing issues. The placements of AFs are optimized by analyzing MEEF and the overall process window. Swelling peaks observed in CD curves are the points in which the AF starts to be inserted.

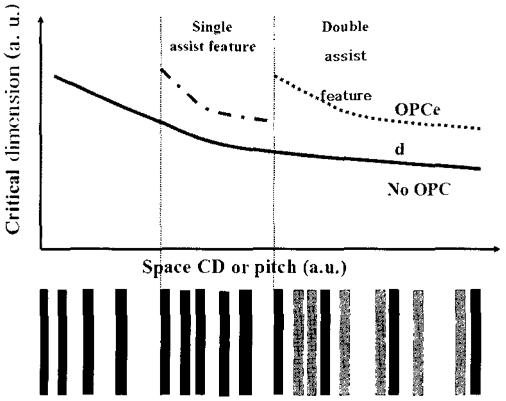


Fig. 1. Schematic diagram for the AF generating rule and CD behavior curves as a function of the pitch size.

By measuring CDs through pitch sizes, parameters needed to generate the simulation model are obtained. After AFs are implemented, selective bias rules are applied using the simulator, Calibre (Mentor Graphics). The OPCed CDs are measured according to pitch sizes and the correction accuracy for the optical proximity variation is assessed.

The iso-dense (I-D) bias is different for PR species due to different light sensitivity and the acid diffusion characteristics. Figure 2 shows the measured results of the linearity deviation for 1:1 L/S patterns. The dotted, light solid and deep solid curves represent PR-A, PR-B, and designed CD, respectively. The measured CDs are largely deviated from their designed CDs when the pitch sizes are increased. PR-A shows the small I-D CD variation comparing to PR-B.

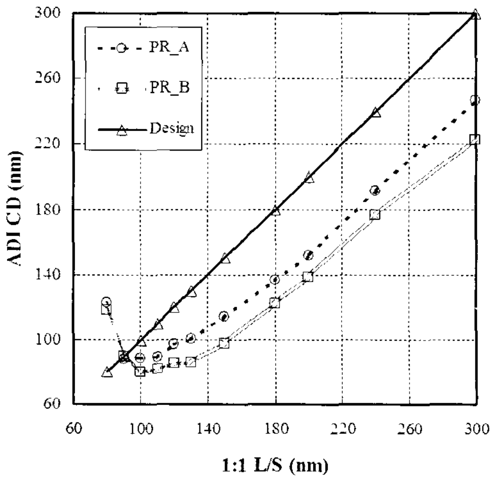


Fig. 2. Linearity deviation for 1:1 L/S patterns.

The proximity dependence on PR species is assessed. Figure 3 shows the 3σ values of proximity variation for PR-A and PR-B. The OPC rules are extracted using PR-B. The average CD of OPCed patterns are measured to be 77 nm. The white and gray bars correspond to 3σ values of proximity variation for PR-A and PR-B, respectively. The black bar is the difference of 3σ values between PR-A and PR-B. The 3σ value of the PR-A is 15.1 nm, while that of the PR-B is 9.3 nm. The difference between two PRs is calculated to be 12 nm which is very large considering the 90 nm design rule. The proximity property proves to be critically dependent on PR species.

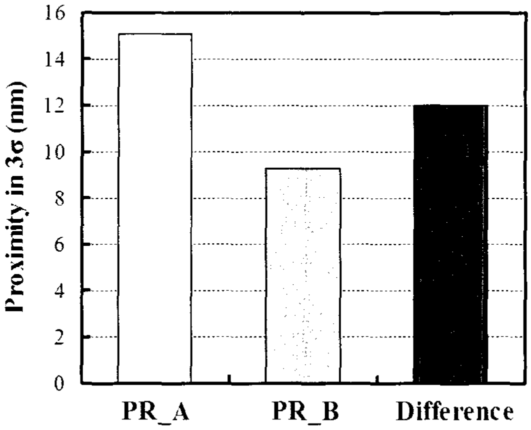


Fig. 3. Proximity results according to PR species.

Figure 4 shows the proximity results according to the change of PEB condition. The 3σ of the proximity effect is measured to be 16.2 nm for the PEB condition of 120℃/60s, and 13.8 nm is obtained for 115℃/90s. The difference between two conditions calculated to be 8.3 nm. The proximity property critically depends on the PEB condition. The temperature and time of the post exposure bake (PEB) affect the acid diffusion characteristics. The acid diffusion according to temperature and time shows the different behavior. So, proximity trends show different properties when different PEB conditions are used at the same PR. The PR species and PEB condition should not be changed after the OPC rule is extracted in order not to critically deteriorate the OCV.

One of factors that severely affect the proximity property is the change of the illumination condition. Figure 5 represents the measured proximity variations according to illumination conditions. Annular condition of inner and out sigma of 0.89 and 0.5 (0.89/0.5) is compared with that of 0.9 and 0.6 (0.9/0.6) at the NA of 0.75. The 3σ values measured are 15.2 nm and 11.6 nm for 0.89/0.5 and 0.9/0.6, respectively. The difference value between two conditions is 9.8 nm corresponding to 84% of degradation. Also, the illumination condition must be fixed once the OPC rule was extracted.

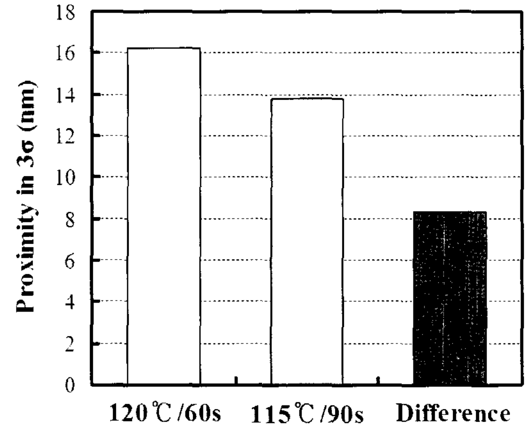


Fig. 4. Proximity results according to PEB conditions.

An actual mask has the CD offset from its nominal CD due to process variations in mask manufacturing. This mask mean-to-target (MTT) is known to produce the I-D CD differences.[11] Figure 6 shows proximity variation results according to MTTs. 3σ values for CD variations are measured to be 11.4, 13.9, and 15.2 nm for 0, 2, and 4 nm, respectively. The degradation amount for 4 nm MTT comparing with 0 nm is calculated to be 10 nm corresponding to 43.6% of the optical proximity. The contributed effect of the mask MTT to total proximity is required to be analyzed in order to control OCV within a tolerance range.

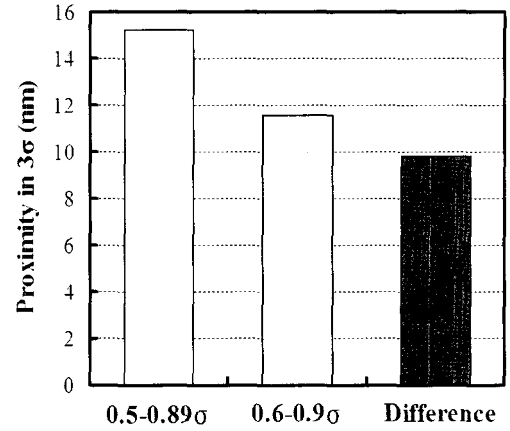


Fig. 5. Proximity results according to illumination conditions.

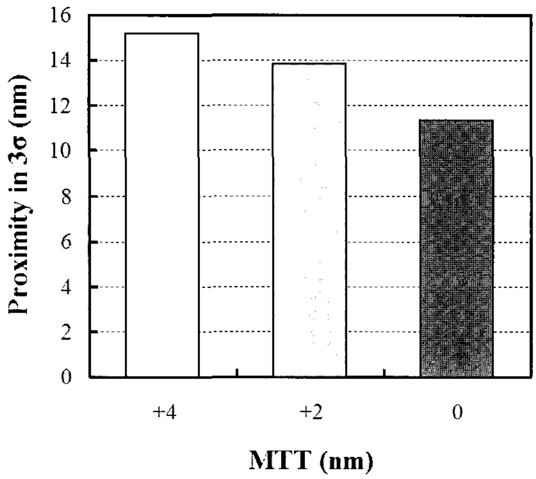


Fig 6. Proximity results according to mask MTTs.

The reduction of the OPC grid size enhances the resolution of printed images. By employing a small grid size the optical proximity is elaborately corrected and the CD variation is reduced. Figure 7 represents the measured CDs of the OPCed L/S patterns generated by using 1 nm and 0.5 nm grid sizes. Nominal CDs are 87 nm. The 3σ values for CD variations are measured to be 14.6 nm and 11.4 nm for 1 nm and 0.5 nm grid sizes, respectively. The improved amount is calculated to be 9.2 nm, corresponding to nearly 39% enhancement. The CD curve of 0.5 nm is shown to pass through that of 1 nm, and the detailed CD correction is shown to be performed.

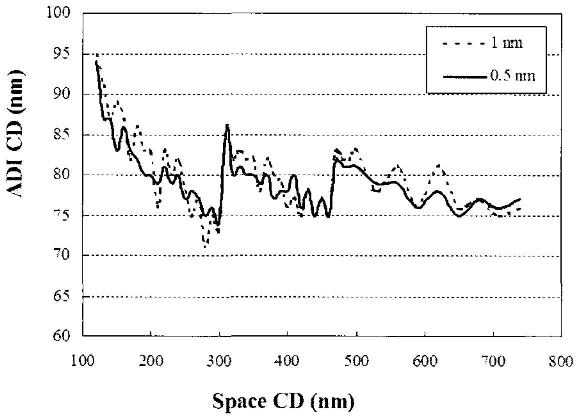


Fig 7. CD variations as a function of space CDs applied with grid sizes of 1 nm and 0.5 nm.

To verify an effect of the grid size on in-field CD uniformity, OPC rules with 1 nm and 0.5 nm grid sizes are simultaneously employed into the SRAM pattern of the 90 nm logic device. Figure 8 shows the in-line SEM image of the unit cell pattern used. The nominal CD marked in this figure is 80 nm. Figure 9 represents the in-field CD uniformity maps measured by in-line SEM. The average values are 72 nm. 3σ values of CD uniformities are 9.9 nm and 8.7 nm for the grid size of 1 nm and 0.5 nm, respectively. Decreasing the grid size improves the CD uniformity of 4.7 nm, corresponding to 22% improvement. The MEEF in this layer is 3.2, and the CD uniformity improvement is expected to be 3.2 nm which value is smaller than 4.7 nm. The CD uniformity improvement does not completely ascribe to the fine OPC grid size. By adopting the grid size of 0.5 nm rather than 1 nm, the mask pattern fidelity is improved. The corner rounding effect and the line edge roughness in mask is supposed to be decreased considerably, which improves the local mask CD uniformity. And this improved mask fidelity delivers the fine printing image and the measurement error using the in-line SEM is fairly reduced.

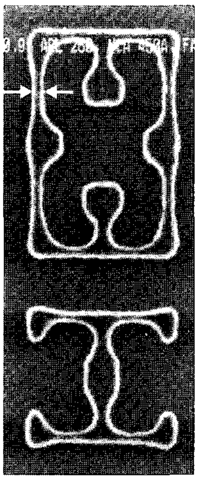
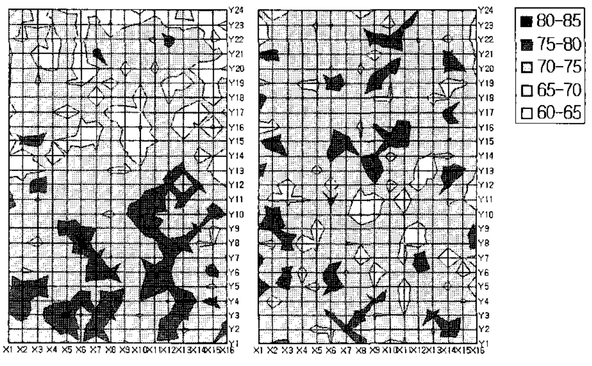


Fig 8. SEM image of monitoring pattern for estimating the CD uniformity.



<1 nm-grid> <0.5 nm-grid>

Fig 9. In-field uniformity maps of the SRAM cell applyin g for 1 nm and 0.5 nm grid size.

III. CONCLUSIONS

The influencing factors on the OPC results are quantitatively analyzed using OPCed L/S patterns. In this experiment the analysis are focused to the optical proximity effects, because the mask uniformity cannot be compensated by the OPC treatment. The OCV which is mainly consisting of the mask uniformity and the optical proximity effect is assumed to be controlled within the tolerance range through OPC.

The proximity property is severely deteriorated by variations of optical and PR conditions. The data needed to generate the model should be newly gathered and another rule be created if these conditions were changed. With these conditions fixed, the efforts are focused to improve the accuracy of OPCed results. For the MTT of 4 nm, deterioration of OPC result is observed to be 43.6%. The mask MTT is proved to affect OPC results and is the critical factor to be controlled. Moreover, the specification of the mask MTT is required to be studied to obtain accurate OCV results. The grid size is also reduced to more accurate control of OCV. Not only the OPC is more elaborately corrected, but also the CD uniformity is improved. Improved mask pattern fidelity enhances patterned images and reduces the measurement errors. Besides, it is necessary to avoid grid mismatches in DRAM which employs the shrinkage strategy of the cell size in each generation. The 0.5 nm grid size adopted in this paper is restricted by the data handling. In order to apply the more accurate OPC and to maintain the process margin possible, the grid size less than 0.5nm needs to be introduced.

REREFENCES

[1] M. D. Levenson, N. S. Viswanathan, and R. A. Simpson, IEEE Trasactions on Electric Devices. **ED-29**, 1828 (1982).

[2] K. K. Toh, G. T. Dao, R. R. Singh, and H. T. Gaw, Proc. SPIE. **1496**, 27 (1991).

[3] S. W. Lee, D. H. Chung, I. G. Shin, Y. H. Kim, S. W. Choi, W. S. Han, and J. M. Shon, Proc. SPIE. **4346**, 762 (2001).

[4] A. Suzuki, K. Saitoh, and M. Yoshii, Proc. SPIE. **3679**, 396 (1999).

[5] S. Y. Zinn, S. W. Lee, S. W. Choi, and J. M. Sohn, J. Vac. Sci. Technol. B **20**(6), 2606 (2002).

[6] S. W. Lee, G. S. Yeo, J. H. Lee, H. K. Cho and W. S. Han, J. Vac. Sci. Technol. B **21**(6), 3120 (2003).

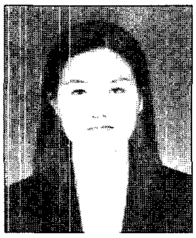
[7] W. S. Han and K. S. Chung, J. Korean Phys. Soc. **30**, 557 (1997).

[8] Y. H. Oh, J.C.Lee and S. Lim, J. Korean Phys. Soc. **33**, S63 (1998).

[9] J. S. Kim, K. C. Park, Y. D. Kim, Y. H. Oh, J. C. Lee, C. S. Goo and S.Lim, J. Korean Phys. Soc. **40**, 163 (2002).

[10] B. W. Smith, Proc. SPIE, **5040**, 399 (2003).

[11] S. W. Lee, D. Y. Lee, H. K. Cho and W. S. Han, Appl. Phys. Lett. **84**(16), to be publishe



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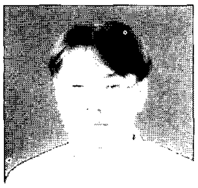

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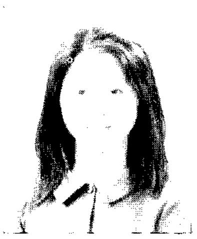

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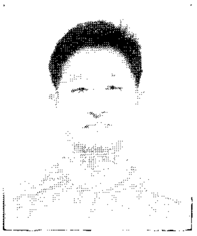

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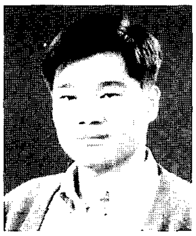

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