Accurate Extraction of Crosstalk Induced Dynamic Variation of Coupling Capacitance for Interconnect Lines of CMOSFETs

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Abstract—**We, for the first time, present novel test patterns and conclusive on-chip data indicating that the variation of coupling capacitance, $\triangle C_C$ by crosstalk can be larger than static coupling capacitance, C_C. The test chip is fabricated using a generic 150 nm CMOS technology with 7 level metallization. It is also shown that $\triangle C_C$ is strongly dependent on the phase of aggressive lines. For anti-phase crosstalk $\triangle C_C$ is always larger than C_C while for in-phase crosstalk $\triangle C_C$ is smaller than C_C.**

I. INTRODUCTION

Interconnect time delay and crosstalk have become key issues for ULSI circuit performance and exact modeling of interconnect line is highly necessary [1-6]. In general there are two major concerns for interconnect lines. One is interconnect line induced delay time which drastically degrade chip performance because interconnect line induced delay time of several millimeters is more than several hundred times larger than pure gate delay time.[3] The other is crosstalk of signal line induced by switching of adjacent aggressive lines. Crosstalk can result in the abnormal switching of victim line and even mal function of operating chip due to crosstalk-induced noise voltage [4-5]. Crosstalk can also severely change the interconnect line induced delay time. That is, concurrent switching of signal line and aggressive line from the same voltage level to the other voltage level (In-phase crosstalk) reduce the interconnect-line induced delay time while different voltage change (Anti-phase crosstalk) increases the delay time drastically. The increase/decrease of delay time, T_D by crosstalk is attributed to the increase/decrease of effective coupling capacitance between signal and aggressive lines due to the crosstalk. It has been generally believed that the maximum variation of coupling capacitance, $\triangle C_C$ is the static coupling capacitance, C_C [4]. And there was a recent theoretical report that $\triangle C_C$ can be larger than C_C [7]. However, there is no experimental evidence that $\triangle C_C$ can be larger than C_C up to now. The exact extraction of $\triangle C_C$ is highly necessary because coupling capacitance comprises almost of interconnect capacitance, i.e., interconnect delay time is strongly dependent on the coupling capacitance.

We present herein novel test patterns and the on-chip data indicating that $\triangle C_C$ can be larger than C_C, for the first time. Interconnect line is designed that only interconnect capacitances dominate interconnect delay time. Therefore, change of coupling capacitance can be directly obtained from the increase/decrease of interconnect delay time as the interconnect delay time is linear function of interconnect capacitance.

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II. EXPERIMENTAL

Test structure for measuring T_D under crosstalk is shown in Fig. 1. The coupling capacitance, C_C between signal line and aggressive lines is altered by crosstalk of aggressive lines as shown in Fig. 2 which represents the cross-section cut along B-B' of Fig. 1. The crosstalk induced delay time variation can be measured using ring oscillators, i.e., successive connection of the basic circuit of A-A' of Fig. 1 constitutes a ring oscillator. Therefore, the oscillation frequency or delay time of ring oscillator is dependent on the interconnect capacitance or crosstalk. When there is no crosstalk, only static coupling capacitance, C_C plays role between signal line and aggressive lines and the delay time is dominated by C_C + C_f + C_a, where C_f is fringe and C_a is area capacitance components of interconnect line. If there happens crosstalk, the coupling capacitance will be altered by $\triangle C_C$ and it can be expressed as $C_{C.eff}$ (= C_C + $\triangle C_C$). The details will be explained later.

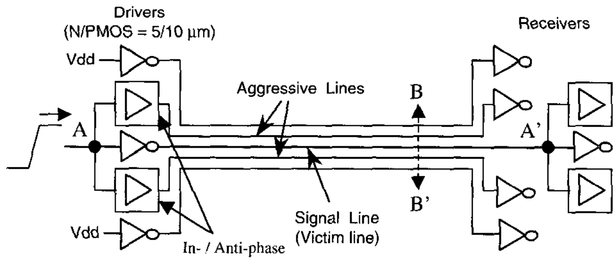

Fig. 1. Test circuit for on-chip measurement of crosstalk induced delay time. Propagation delay time of signal line (victim line) is altered by in- or anti-phase switching of aggressive lines. Successive connect of A-A' constitute a ring oscillator.

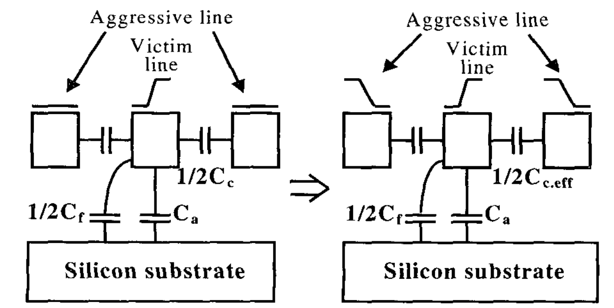

Fig. 2. Area (C_a), fringing (C_f), and coupling (C_c) capacitances and effective coupling ($C_{c.eff}$) capacitance under crosstalk. $C_{c.eff}$ is C_C + $\triangle C_C$.

Three kinds of interconnect test patterns (A-A' of Fig. 1) are designed to evaluate the variation of coupling capacitance, $\triangle C_C$ by crosstalk as shown in Fig. 3. Fig. 3(a) is a reference structure without crosstalk. The main advantage of the proposed test structure is that interconnect line resistance, R_{INT} is much smaller than transistor ON resistance, R_{ON}, i.e., interconnect delay time is only dominated by interconnect capacitance rather than RC delay time of normal interconnect lines. Fig. 3(b) represents in-phase crosstalk because voltage level and switching time of signal line and aggressive line is the same, while Fig. 3(c) represents anti-phase crosstalk because the voltage level is the opposite.

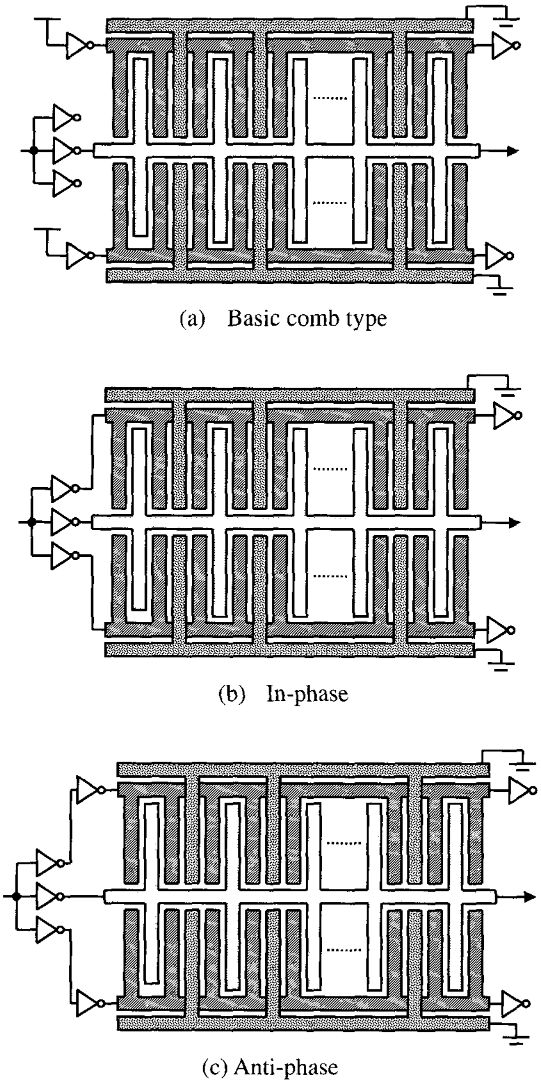

Fig. 3. Test interconnect patterns (A-A' of Fig. 1) consisting of a ring oscillator for measuring the delay time induced by crosstalk. (a) Reference structures without crosstalk, (b) for in-phase and (c) for anti-phase crosstalk.

The test chips were fabricated using a 150 nm CMOS technology [8-10]. Key process flow is as follows. Shallow trench isolation (STI), retrograde twin well, 26 Å and 70 Å dual gate oxide for core and I/O devices, respectively, LDD and halo implantation, sidewall formation, n^+ and p^+ implantation and novel Ti-capped two-step cobalt salicide are applied sequentially [5], [12]. Then, advanced back end of line processes with 7 metal layers and low-k IMD layer of Fluorinated Silicate Glass (FSG, k=3.7) were used. IMD with HSQ (k=3.1) was also fabricated for comparison. The key parameters of used CMOS technology with 7 metal layers are summarized in Table 1.

Table 1. Interconnect and key device parameters of used 150 nm CMOS technology.

M1 Line width/space	0.22/0.22 μm
M2 Line width/space	0.24/0.24 μm
Thickness of Metal	0.53 μm
ILD/IMD thickness	0.70/0.80 μm
Dielectric constant	3.1 / 3.7
Id.sat / Ioff (μA/μm) / (nA/μm)	N : 670 / 1.65 P : 280 / 0.35
Operating voltage	1.5 V

III. RESULTS AND DISCUSSIONS

Fig. 4 shows the interconnect line induced delay time versus gate length for extraction of the ratio of coupling capacitance to total interconnect capacitance. Here, T_D was measured from test structures detailed in Ref. [3]. The slopes in Fig. 4 represents the contribution of involved capacitance components to delay time. It is shown that C_C of interconnect line for 0.15 μm CMOS technology comprises about 78.8 and 82.4 % of the total capacitance for HSQ and FSG IMD layers, respectively, which means that relative ratio of coupling capacitance to total interconnect capacitance is 0.788 and 0.824 (The relative ratio is defined as C1 and its usage will be explained later.). Fig. 5 shows the interconnect delay time, T_D, measured from the proposed test structures of Figs. 1 and 3. Indeed, T_D varies widely, depending on the phase of aggressive lines and it increases linearly with interconnect length, *L*, that is, the increase or decrease of T_D by crosstalk is proportional to the variation of coupling capacitance, $\triangle C_C$ and interconnect delay time is only dominated by interconnect capacitance. Therefore, $\triangle C_C$ is obtained by dividing the difference of delay times between basic (Fig. 3(a)) and in-phase (Fig. 3(b)) or anti-phase (Fig. 3(c)) cases by the delay time purely due to the static coupling capacitance component. Therefore, $\triangle C_C$ or $C_{C.eff}$ can be readily extracted from Fig. 5, using simple equation as described in Table 2. The procedure for extraction of equations in Table II is explained as follows.

Table 2. Delay time definitions and equation for extraction of coupling capacitance, $\triangle$Cc.

T_0	Delay time of ring oscillator without interconnect load
T_D	Delay time of ring oscillator with interconnect load
$T_{D.Cross}$	Delay time with crosstalk
C1	Percent of Cc to total capacitance (Fig. 4)
$\triangle$Cc (× Cc)	$\mid T_{D.Cross} - T_D \mid / ((T_D - T_0) \times C1)$
$C_{C.eff}$	$C_C - \triangle C_C$ for in-phase crosstalk $C_C + \triangle C_C$ for anti-phase crosstalk

T_D for interconnect line is generally expressed as (1) [3] and (1) can be simplified as (2) for the proposed interconnect structures because interconnect line resistance, R_{INT} is negligible. A in (2) is constant and exact value of A is not needed because the coupling capacitance variation will be extracted as a function of relative ratio of C_C. Then, under crosstalk, (2) can be modified as (3) due to the variation of coupling capacitance. Next, the subtracted delay time of (3) by (2) is divided by (2) ×C1, where C1 is the percent contribution of coupling capacitance to total interconnect capacitance and C1 was already extracted from Fig. 4.

$$T_D = 0.4\, R_{INT}\, C_{INT}\, L^2 + 0.7\, R_{ON}\, C_{INT}\, L + 0.7\, R_{INT}\, C_{TR}\, L \quad (1)$$

$$T_D = A\, C_{INT}\, L \quad (2)$$

$$T_{D.Cross} = A\,(C_{INT} + \triangle C_C)L \quad (3)$$

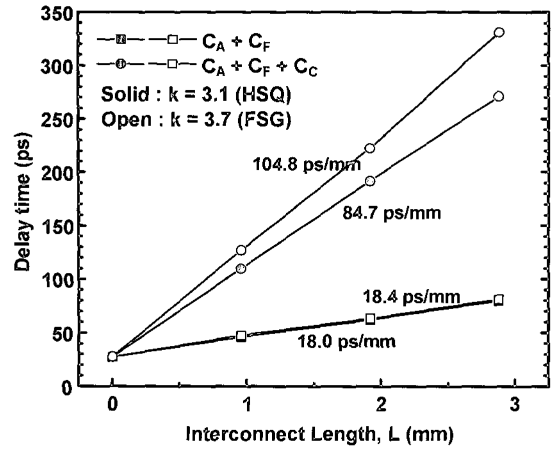

Fig. 4. Delay time vs. interconnect length, L for comb type interconnects [3]. Percent of C_C to total capacitance (C1) is 0.788 and 0.824 for HSQ and FSG IMD, respectively.

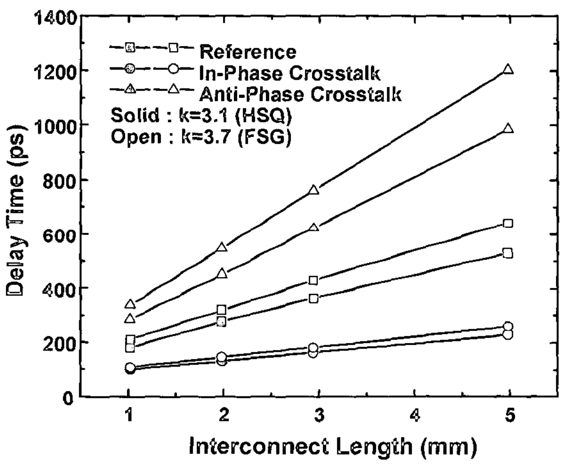

Fig. 5. Delay time variation ($T_{D\,Cross}$) by crosstalk. Delay time is only dominated by interconnect capacitance because the delay time is linearly proportional to the interconnect length regardless of crosstalk.

Fig. 6 shows the extracted $\triangle C_C$ or $C_{C.eff}$ using proposed interconnect structures. Clearly, $\triangle C_C$ of anti-phase crosstalk is larger than C_C which has been considered maximum limit under crosstalk. $\triangle C_C$ larger than C_C means $C_{C.eff}$ is larger than $2\times C_C$ for anti-phase and smaller than 0 for in-phase. In this experiment, in case of in-phase crosstalk $\triangle C_C$ was smaller than C_C.

To verify the results, HSPICE simulation is performed for FSG IMD case as shown in Fig. 7. First, delay time of the proposed interconnect structures is simulated. Then, basic structures of Fig. 3(a) with only split of the coupling capacitance as $2\times C_C$ and 0, representing anti-phase and in-phase crosstalk, respectively, is simulated to compare the delay time with crosstalk. As shown in Fig. 7, the delay time with anti-phase crosstalk is larger than delay time with coupling capacitance of $2\times C_C$ without crosstalk, which shows clear agreement with Fig. 6. In case of in-phase crosstalk, the delay time with crosstalk is larger than $C_C = 0$ without crosstalk case and this also shows the same result as in Fig. 6. Therefore, the absolute variation of coupling capacitance by crosstalk is successfully obtained using the proposed test structures. The exact extraction of $\triangle C_C$ enables the accurate prediction of the circuit performance.

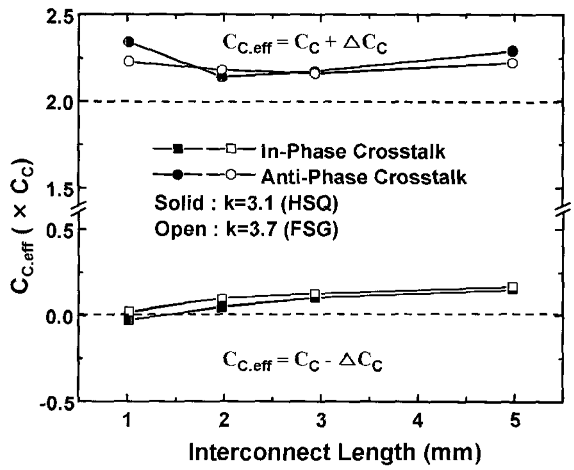

Fig. 6. Effective coupling capacitance, $C_{C.eff}$ with in- and anti-phase crosstalks. The variation of coupling capacitance, $\triangle C_C$ is clearly larger than C_C for anti-phase crosstalk.

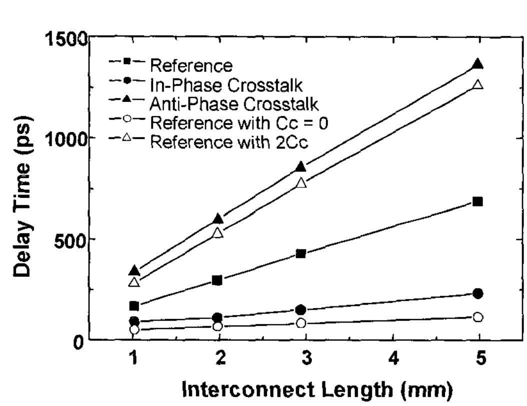

Fig. 7. HSPICE simulation with and without crosstalk as well as only split of coupling capacitance without crosstalk. Simulation result shows good agreement with the measured data of Fig. 6.

IV. CONCLUSIONS

Dynamic on-chip characterization of the variation of coupling capacitance by crosstalk has been performed in depth using novel test patterns. The test patterns were implemented using a 150 nm CMOS technology with 7-level metallization. It is shown that $\triangle C_C$ is always larger than C_C for anti-phase crosstalk and a little smaller than C_C for in-phase crosstalk. It is the first time to experimentally prove that the variation of coupling capacitance under crosstalk can be larger than $2 \times C_C$. HSPICE simulation is performed to validate the extracted variation of coupling capacitance using measured data. Exact extraction of $\triangle C_C$ is crucial for accurate prediction of circuit performance in GHz range.

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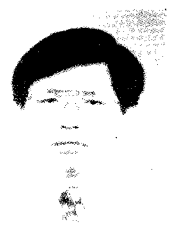

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