An On-Chip Differential Inductor and Its Use to RF VCO for 2 GHz Applications

Je-Kwang Cho, Kyung-Suc Nah, and Byeong-Ha Park

Abstract—**Phase noise performance and current consumption of Radio Frequency (RF) Voltage-Controlled Oscillator (VCO) are largely dependent on the Quality (Q) factor of inductor-capacitor (LC) tank. Because the Q-factor of LC tank is determined by on-chip spiral inductor, we designed, analyzed, and modeled on-chip differential inductor to enhance differential Q-factor, reduce current consumption and save silicon area. The simulated inductance is 3.3 nH and Q-factor is 15 at 2 GHz. Self-resonance frequency is as high as 13 GHz. To verify its use to RF applications, we designed 2 GHz differential LC VCO. The measurement result of phase noise is –112 dBc/Hz at an offset frequency of 100 kHz from a 2 GHz carrier frequency. Tuning range is about 500 MHz (25%), and current consumption varies from 5 mA to 8.4 mA using bias control technique. Implemented in 0.35-μm SiGe BiCMOS technology, the VCO occupies 400 um x 800 um of silicon area.**

I. INTRODUCTION

The recent remarkable increase of wireless communications systems has driven RF integrated circuits to much more integration, while maintaining low power, high performance, and low cost [1-3]. Among those, an integrated RF VCO is one of the most difficult building blocks due to stringent phase noise requirement of modern wireless communications. In order to achieve low phase noise performance, LC-based VCOs have been widely used in RF applications because of its higher Q characteristic than ring-oscillator architecture [4-6]. If the required phase noise specifications are to be achieved, the Q-factor of on-chip spiral inductor should be maximized since VCO phase noise performance is highly dependent on the Q-factor of the LC tank. For that reason, on-chip spiral inductor has been the main subject of numerous researches [7]-[8].

In this paper, we present the modeling of an optimized on-chip differential spiral inductor and its use to 2GHz differential VCO in a 0.35-μm SiGe BiCMOS technology. The LC tank consists of on-chip differential spiral inductor, 6-bit digitally controlled switched-capacitors bank for coarse and wide tuning, and two p-n junction diodes for fine tuning. A bias current control technique is employed to guarantee stable phase noise characteristic for the entire frequency band [9]. The measurement results show well how the inductor improves VCO performance and saves die area.

II. ON-CHIP DIFFERENTIAL INDUCTOR

The Q-factor of differential inductor is same as that of single-ended inductor at low frequency. However, a shorted inductor self-resonates fundamentally at the quarter-wavelength frequency whereas a differential transmission line self-resonates at the half-wavelength frequency. This means that differential inductor self-resonates at approximately two times higher frequency

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than single-ended inductor [10]. Therefore, Q-factor difference between the two inductors increases as operating frequency goes up. In addition, another advantage is a reduction of chip area because of the mutual magnetic coupling, which results in less substrate loss at high frequency.

The layout and its equivalent model of octagonal differential inductor are shown in Fig. 1 and Fig. 2, respectively. Because spiral inductor dominates the Q-factor of the LC tank, special care should be taken to achieve high Q-factor inductor [11]. The unloaded Q-factor of inductor is highly dependent on the series resistance, so the metal width of the inductor is as wide as 20 um. Inner diameter of the inductor should be large not to generate eddy current on the inner metal traces.

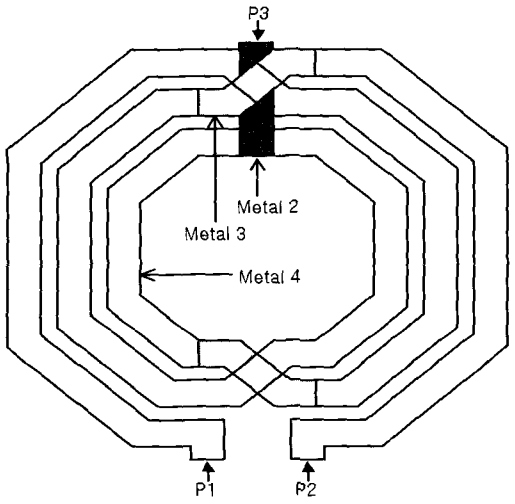


Fig. 1. Differential inductor layout.

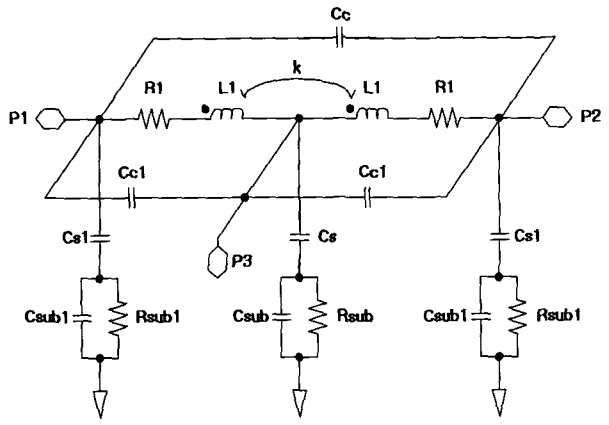


Fig. 2. Equivalent model of differential inductor

The inductor uses 3um thick aluminum top metal and has the Q-factor of 15 at 2 GHz operating frequency differentially. The differential inductance value is 3.3 nH. Summary of the geometry and EM-simulated equivalent model are listed in Table 1 and Table 2, respectively. To verify the superiority of differential characteristics to single-ended counterparts, both Q-factor and self-resonance frequency (SRF) are simulated, compared, and shown in Fig. 3. The extent of Q-factor improvement is about 36 % (from 11 to 15) at 2 GHz and SRF increases from 11 GHz to 13 GHz.

Table 1. Geometry of the differential inductor

Outer diameter	Metal width	Line spacing	Metal thickness	# of turns
300um	20um	2um	3um	3

Table 2. EM-simulated results of the inductor

Q@2GHz	k	L1	R1	Cc	Cc1
15	0.57	1.03 nH	1.2 Ω	33 fF	1.6 fF
Cs	Csub	Rsub	Cs1	Csub1	Rsub1
327 fF	43 fF	497 Ω	70 fF	19fF	661 Ω

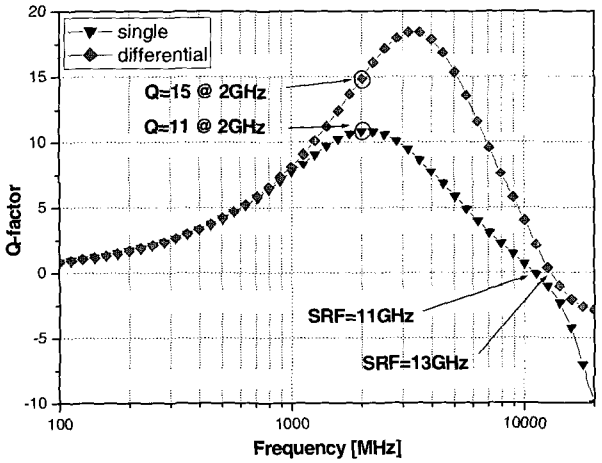


Fig. 3. Comparison of Q-factor and self-resonance frequency (SRF) between single-ended and differential inductor.

III. Voltage-Controlled Oscillator Design

To demonstrate the usefulness of the modeled differential inductor, we designed a simple 2GHz differential LC VCO as shown in Fig. 4. The Cap. Bank block in the schematic consists of digitally-controlled, binary-weighted switched capacitors for coarse tuning,

and PN junction diodes for fine tuning. Q1, Q2 provide negative resistance for stable oscillation. The center port of the differential inductor is connected to supply voltage.

The schematic of switched-capacitors bank and varactor diodes is shown in Fig. 4 in detail. Analog control signal, Vc, varies reverse bias voltage of the varactor diodes so as to achieve fine tuning. The other voltage signals are digital signals that turn on or off binary-weighted N-MOSFET switches. When using switched-capacitors in the LC tank, on-resistance, which is connected to capacitor in series equivalently in on state, must be small enough not to degrade the loaded Q of the LC tank.

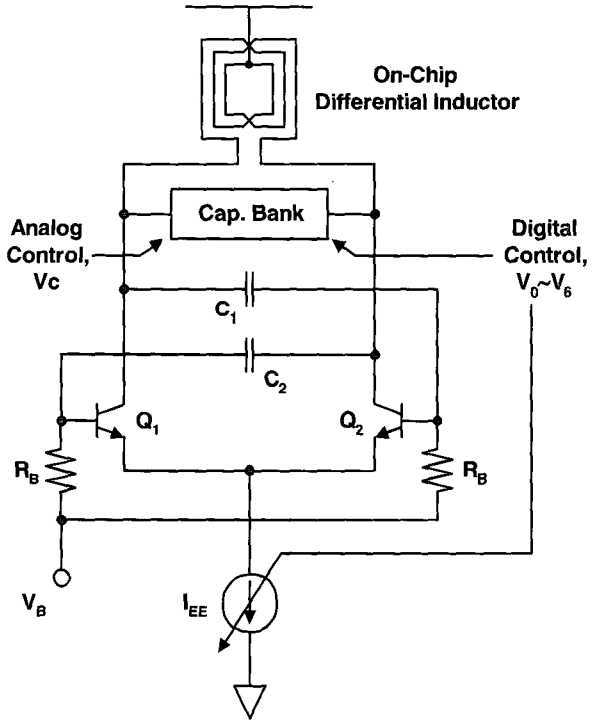


Fig. 4. Schematic of the VCO

In the case of wide band VCO, oscillation amplitude level varies because of the change of the Q-factor of the LC tank. 6 bit digital signals, which control switched-capacitors bank, also change the amount of tail current of the VCO to obtain constant amplitude level across the LC tank regardless of the operating frequency as shown in Fig. 6. We designed VCO tail current to vary from 5 mA to 8.4 mA and unit current variation to be 53 uA. Single-ended oscillation amplitude level is 1 V (zero-to-peak), which is the optimum amplitude for low phase noise under the condition of 2.8 V supply voltage.

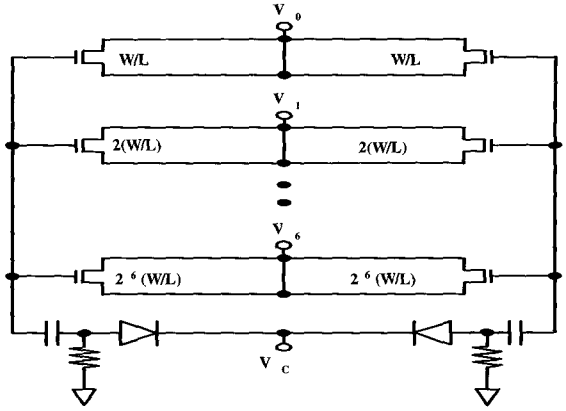


Fig. 5. Schematic of the Cap. Bank block

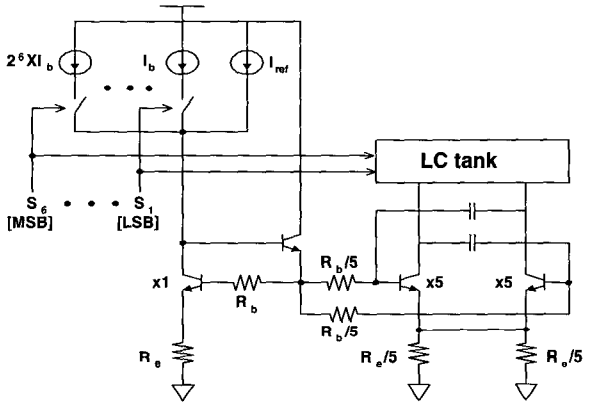


Fig. 6. Bias current control scheme

IV. Measurement Results

The VCO was fabricated using Samsung's 0.35um BiCMOS technology and the microphotograph is shown in Fig. 7.

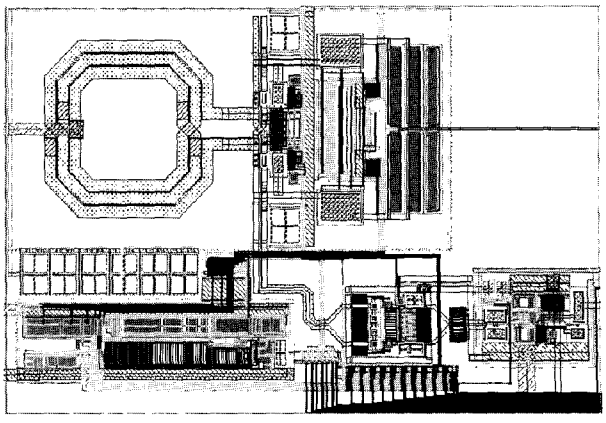


Fig. 7. Microphotograph of the VCO

The operating frequency is varied by 6-bit digitally controlled switched-capacitor bank for coarse tuning and varactor diodes for fine tuning as shown in Fig. 8. Total operating frequency is from 1.68 GHz to 2.18 GHz and tuning range is as wide as 500 MHz (25%). The VCO gain of bottom curve is much lower than that of top curve. This is because the contribution of the varactor capacitance to the total capacitance reduces as switched-capacitors are turned on one by one. The VCO gain of top curve is 25 MHz/V and that of bottom curve is 12 MHz/V. Center frequency spacing between adjacent frequency curves is also different with respect to the digital code because of the same reason.

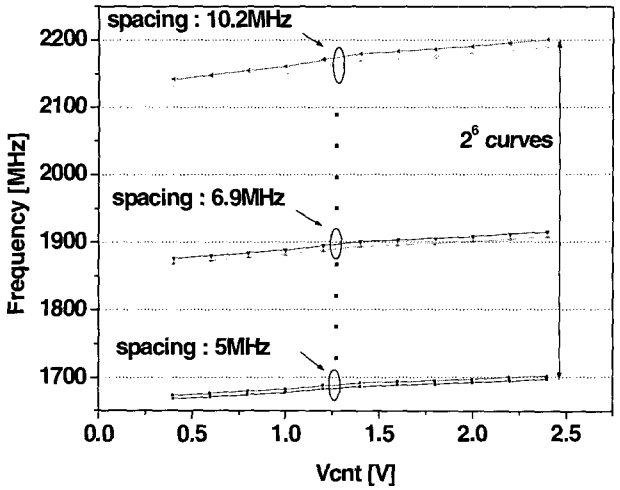
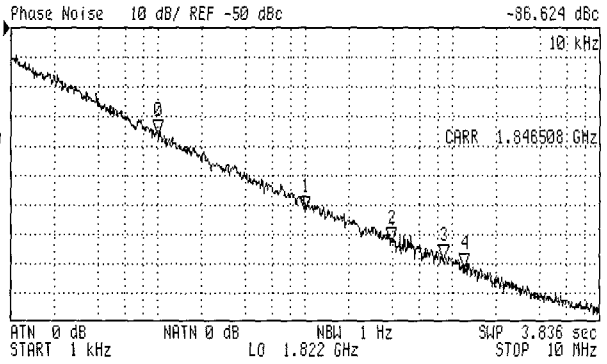


Fig. 8. Measured frequency characteristic



N	SWP PARAM	VAL
0	10 kHz	-86.624 dBc
1	100 kHz	-112.88 dBc
2	400 kHz	-123.22 dBc
3	900 kHz	-129.32 dBc
4	1.25 MHz	-132.25 dBc

Fig. 9. Phase noise measurement

The measured phase noise of the VCO is –112 dBc/Hz at an offset frequency of 100 kHz from a 1.8 GHz carrier frequency as shown in Fig. 9. Out-band noise floor is much lower than –140 dBc/Hz. Current consumption varies from 5mA to 8.4mA. The active area of the VCO core is 400um × 800um.

Table 3 summarizes the measurement results.

Table 3. VCO measurement summary

Item	Measured Result
Operating Freq.	1.68GHz ~ 2.18GHz
Tuning Range	500MHz (25%)
VCO Gain	12MHz/V ~ 25MHz/V
Phase Noise	-112dBc/Hz @ 100kHz
Output Power	-3dBm ~ -4dBm
Current Consumption	5mA ~ 8.4mA

V. CONCLUSION

As a building block of a single chip RF transceiver IC, a 2-GHz low noise VCO is designed, implemented, and measured. To achieve low phase noise performance, an on-chip differential inductor for the use of LC tank is designed, analyzed and modeled. The simulated inductance is 3.3nH and Q-factor is as high as 15 at 2GHz. The measured phase noise is as low as –112 dBc/Hz at an offset frequency of 100 kHz from a 2 GHz carrier frequency and tuning range is about 500 MHz (25%). These results show the feasibility of true single chip multi-band multi-mode RF transceiver IC on silicon.

REREFENCES

[1] Ickjin Kwon and Hyungcheol Shin, J. Korean Phys. Soc. 40, 4 (2002).

[2] Ju-Ho Son and Dong-Yong Kim, J. Korean Phys. Soc. 43, L1 (2003).

[3] S. Tadjpour, E. Cijvat, E. Hegazi, and A. A. Abidi, "A 900-MHz Dual-Conversion Low-IF GSM Receiver in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1992-2002, Dec. 2001.

[4] Joonho Gil, Ickjin Kwon and Hyungchel Shin, J.

Korean Phys. Soc. 42, 241 (2003).
[5] A. Hajimiri, and T. H. Lee, "Design Issues in CMOS Differential LC Oscillator," *IEEE J. Solid-State Circuits*, vol. 34, pp. 717-724, May. 1999.
[6] A. Kral, F. Behbahani, and A. A. Abidi, "RF-CMOS Oscillators with switched Tuning," in *Proc. IEEE Custom Integrated Circuits Conference*, pp. 555 – 558, May. 1998.
[7] Joachim N. Burghartz, D. C. Edelstein, Mehmet Soyuer, H. A. Ainspan, and Keith A. Jenkins, "RF Circuit Design Aspects of Spiral Inductors on Silicon," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2028-2034, Dec. 1998.
[8] Chia-Hsin Wu, Chih-Chun Tang, and Shen-Iuan Liu, "Analysis of On-Chip Spiral Inductors Using the Distributed Capacitance Model," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1040-1044, Jun. 2003.
[9] Je-Kwang Cho. Han-Il. Lee, Kyung-Suc Nah, and Byeong-Ha Park, "A 2GHz Wide Band Low Phase Noise Voltage-Controlled Oscillator with On-Chip LC Tank," in *Proc. IEEE Custom Integrated Circuits Conference*, 2003, pp. 559-562.
[10] Ali. M. Niknejad, "Analysis, Simulation, and Applications of Passive Devices on Conductive Substrates," PhD dissertation, UC Berkeley, 2000
[11] J. Craninckx, and M. S. J. Steyaert, "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," *IEEE J. Solid-State Circuits*, vol. 32, pp. 736-744, May. 1997.

Je-Kwang Cho was born in Taegu, Korea, in 1975. He received the B.S and the M.S degrees in electronics engineering from the Korea University in 1998, 2000, respectively.

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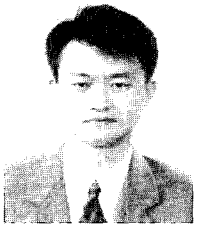

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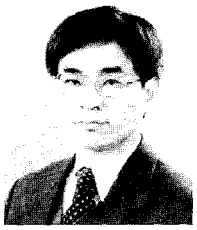

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