Design Consideration of Body-Tied FinFETs (Ω MOSFETs) Implemented on Bulk Si Wafers

Kyoung-Rok Han, Byung-Gil Choi, and Jong-Ho Lee

Abstract—**The body-tied FinFETs (bulk FinFETs) implemented on bulk Si substrate were characterized through 3-dimensional device simulation. By controlling the doping profile along the vertical fin body, the bulk FinFETs can be scaled down to sub-30 nm. Device characteristics with the body shape were also shown. At a contact resistivity of 1×10^{-7} Ωcm^2, the device with side metal contact of fin source/drain showed higher drain current by about two. The C-V results were also shown for the first time.**

Index Terms—**FinFET, Omega, C-V, bulk, 3-D Simulation**

I. Introduction

Double/Triple-gate MOSFETs have been considered the device structures having excellent scale-down characteristics and performance. The family of the double/triple-gate device structure includes FinFETs [1], triple-gate MOSFETs [2], Pi-gate MOSFETs [3], and Omega gate MOSFETs [4]. All these devices have been implemented on SOI wafers. The Omega gate MOSFETs have the best scaling-down characteristics, but may suffer from more severe corner effects and process difficulty due to polysilicon gate residue under the bottom corners of the body. It needs to be noted that the gate all-around MOSFET [5] has the best scaling down characteristics but the process steps are very difficult. Body-Tied FinFETs (bulk FinFETs) built on bulk Si wafers have been demonstrated experimentally [6]-[9] by our group, and have shown several advantages over SOI FinFETs while keeping nearly the same scaling-down characteristics [10]. It has many advantage of lower cost and defect density, less body bias effect, and higher heat transfer rate over SOI FinFET. The bulk FinFETs have a very good process compatibility with the conventional planar channel CMOSFETs. However, it is strongly required to understand the device characteristics of the bulk FinFET before device design since the device design of the bulk FinFETs is clearly different from those of SOI FinFETs and conventional planar gate MOSFETs.

In this paper, the bulk FinFETs are characterized through 3-Dimensional (3-D) simulation, and brief design guideline is suggested. And we call also the device Ω MOSFET, because the body shape look likes Greek letter Omega(Ω).

II. Device Structure

Fig. 1 shows 3-D schematic view of triple-gate bulk FinFET. The body is directly connected to the silicon substrate, which removes any floating body effects and gives much higher heat transfer rate to the substrate [10]. The H_{Fin} and W_{Fin} represent fin channel height and width, respectively. The x_{jSDE} stands for junction depth of source/drain extensions (SDE). The junction depth is defined as the depth from the top of the body. The LDD concentration is 6×10^{19} cm^{-3} and has the profile of about dec/5nm. The corner regions of the fin were rounded to remove any possible leakage path. In Fig. 1, the top gate oxide can be thick so that the device operates as a double-

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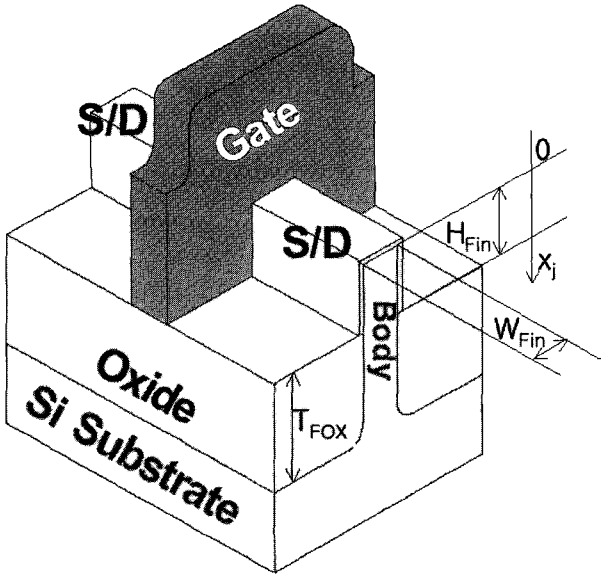


Fig. 1. 3-dimensional schematic view of body-tied FinFET. HFin and WFin represent fin height and width, respectively. T_{FOX} and x_j stand for the field oxide thickness and the source/drain junction depth, respectively.

gate bulk FinFET, otherwise the device acts as a triple-gate bulk FinFET. In this work, we normally focus on the double-gate bulk FinFETs. The gate material is n^+ polysilicon. Drift-diffusion (DD) model was adopted in physical model because the DD model reflects well device characteristics in subthreshold region.

III. Device Simulation Results

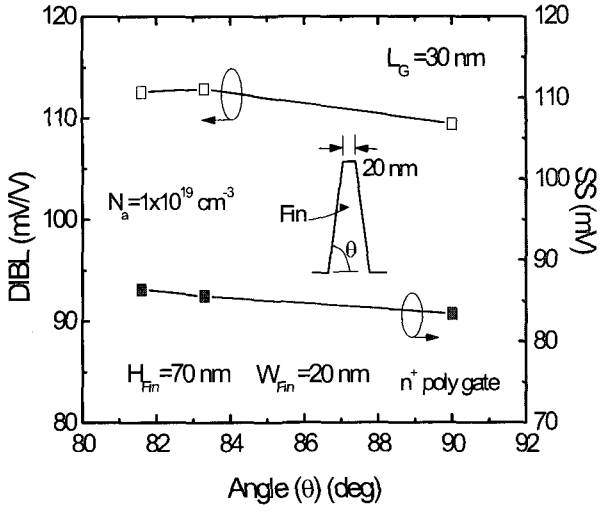


Fig. 2. DIBL and SS characteristics with the angle of fin body. The body doping is 1×10^{19} cm^{-3} and n^+ poly gate was used. The small insert represents the schematic of the fin body.

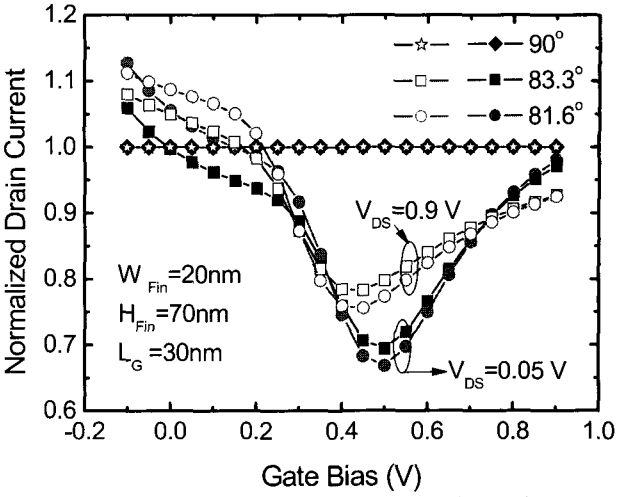


Fig. 3. Normalized drain current versus gate bias as functions of drain bias and fin body angle. Drain currents for each drain bias are normalized to that of the device with the fin body of right angle.

In the device simulation using ATLAS [11], the bulk FinFET has the gate height of 70 nm, fin width of the top of 20 nm, and physical gate length of 30 nm, respectively. The gate oxide thickness (T_{ox}) is 1.5 nm. The body doping is 1×10^{19} cm^{-3} and n^+ poly gate was used. Figs. 2 and 3 show device characteristics with the fin body shape. The small insert in figure 2 represents the schematic of the fin body. The angle θ represents the side surface slope of the fin body. An angle of 90° (right-angle) means the body shape with vertical side surfaces. The angle was changed from 81.5° to 90°. Drain-Induced Barrier-Lowering (DIBL) and Subthreshold Swing (SS) characteristics are degraded slightly with the decrease of the body angle.

In Fig. 3, normalized drain current versus gate bias as functions of drain bias and fin body angle is shown. Drain currents for each drain bias are normalized to that of the device with the fin body of the right-angle. As the body angle decreases, the off-current increases and the on-current decreases. For example, the device with an angle of 81.5° shows 10% higher off-current compared to the device with the right-angle body shape at V_{GS} of 0 V and V_{DS} of 0.9 V. At given V_{DS}=V_{GS}=0.9 V, the device with the right-angle body shape shows about 10% higher on-current. The devices with the non-right-angle body show significant current degradation around the V_T's. We can improve device characteristics by keeping the angle to 90° as possible.

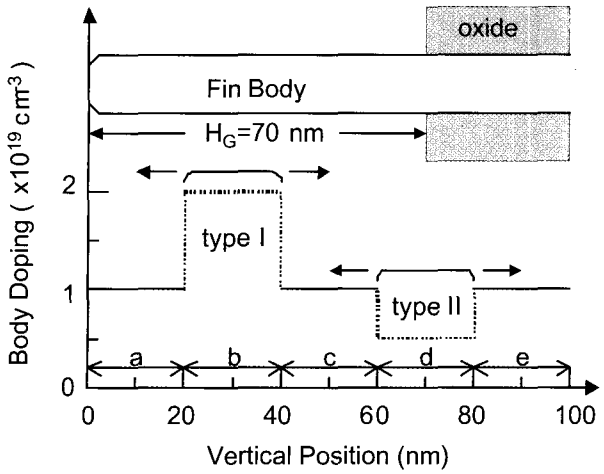
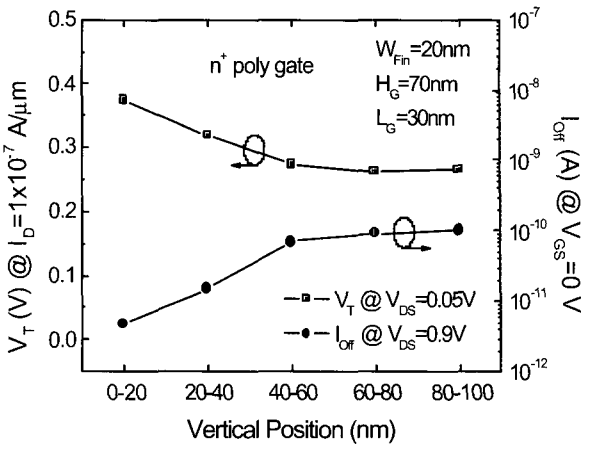


Fig. 4. Schematic representation of 90° rotated fin body and doping types along the fin body. In type I doping, additive doping region over a 20 nm distance is moved from the top of the fin to deep into the body. Subtractive doping region in type II doping is moved as the same way as in type I.

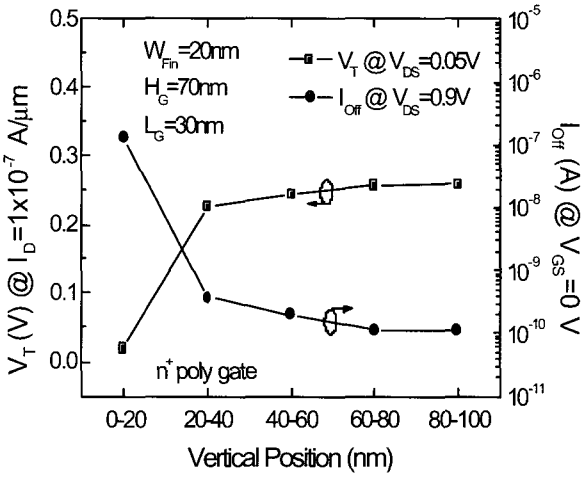
In Fig. 4, additive or subtractive doping to the uniform body doping was checked to see the doping effect by changing the doping in the fin body vertically. Schematic representation of 90° rotated fin body and doping types along the fin body is shown in the upper part of the figure. The fin height (H_G) and the fin width are 70 nm and 20 nm, respectively. In type I doping of 2×10^{19} cm^{-3}, additive doping region over a 20 nm distance is moved from the top of the fin to deep into the body. Subtractive doping region in type II doping of 5×10^{18} cm^{-3} is moved as the same way mentioned above.

Fig. 5 shows V_T and I_{OFF} characteristics with selectively increased type I doping (a) and decreased type II doping (b) in vertical direction of the fin body. The V_T was defined as the gate bias when the drain current is 1×10^{-7} μA/μm. The doping control near the fin top position gives the most significant effect on the V_T and I_{OFF} because of the top corner region. Therefore, in actual device design, the doping around fin top region carefully considered. It is recommended that the doping level around the top region of the fin body needs to be increased by about 1.5 times higher than the uniform body doping level when we adopt n$^+$ polysilicon gate for NMOS transistors.

Source/drain metal contact structure gives an important role in contact resistance. Fig. 6 shows drain current versus contact resistivity as a parameter of metal contact structure on source/drain region. The small inserts stand



(a) Type I



(b) Type II

Fig. 5. V_T and I_{off} characteristics with selectively increased type I doping (a) and decreased type II doping (b) in vertical direction of the fin body. Doping change around top region of the fin gives significant change and carefully considered in the device design.

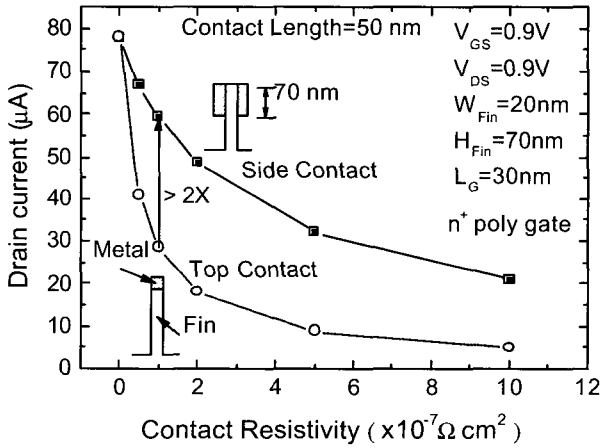


Fig. 6. Drain current versus contact resistivity as a parameter of metal contact structure on source/drain region. The small inserts stand for the metal contact structure on the fin body.

for the metal contact structure formed on the source/drain region in the fin body. Dark regions represent the Al metal regions. The contact length is 50 nm. The contact widths of the side contact (upper) and the top contact (lower) are 70 nm on both side surfaces and 20 nm on top of the body, respectively. As the contact resistivtity increases, the drain current decreases. Especially, the current degrades significantly in the device (lower) with the contact on top of the source/drain region. The device with the side metal contact shown in the upper insert gives two times higher drain current than that with the top metal contact at a contact resistivity of 1×10^{-7} $\Omega\mu m^2$. In nano-scale double/triple gate devices, it is very effective to use the side metal contact together with the top contact simultaneously without increasing tow-dimensional area.

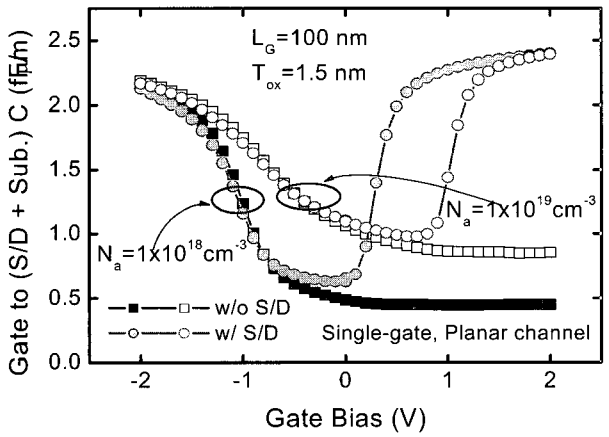


Fig. 7. Simulated quantum C-V characteristics of single-gate planar channel NMOSFETs as a function of the channel doping. The n^+ poly-Si gate was used.

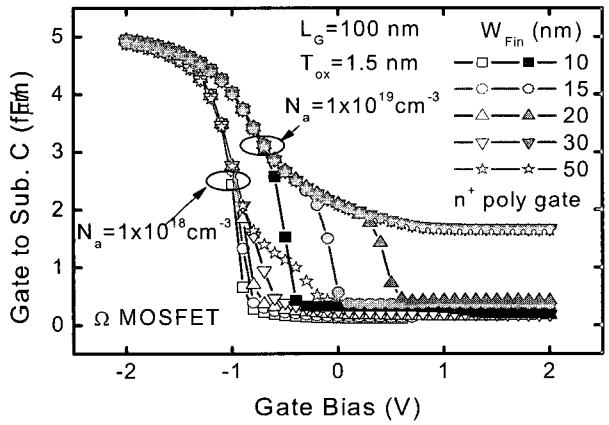


Fig. 8. Comparison of classical and quantum mechanical C-V characteristics of Ω MOSFET as a function of the body doping concentration at a fixed fin width of 20 nm.

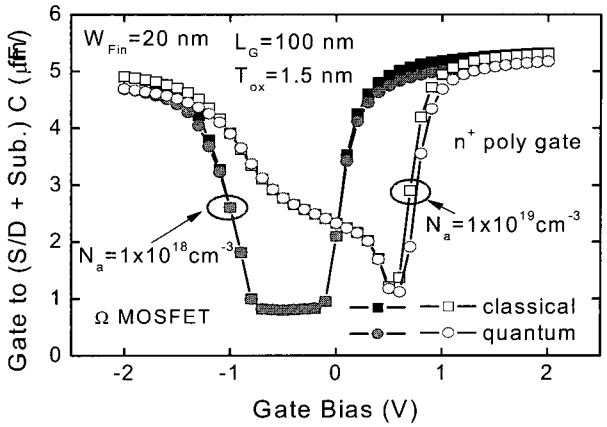


Fig. 9. Simulated C-V characteristics as functions of the fin width and body doping concentration. These results were obtained by considering quantum effect in the channel.

The capacitance-voltage (C-V) characteristics of the double/triple body-tied Ω MOSFETs have not been reported. The C-V characteristics with the doping and the thickness of the fin body are shown here. Then devices have n^+ poly-Si gate and the channel length of 100 nm. In Figs. 7, 8, and 9, high frequency C-V characteristics are shown. Fig. 7 shows the data of the single-gate planar channel MOSFET (conventional) for comparison as a function of the channel doping concentration. Quantum mechanical phenomenon was taken into account in the simulation. The C-V data with and without grounded source/drain are reasonable and compared with those of the double gate Ω MOSFET.

In Fig. 8, the C-V characteristics of double-gate MOSFET with the fin body width of 20 nm. The capacitance per unit width in the accumulation and the inversion are nearly twice due to the two gates. By the quantum mechanical effect in the channel, threshold voltage increases slightly and the inversion capacitance decreases slightly. The behavior at the doping level of 1×10^{19} cm^{-3} is clearly different from that of planar channel MOSFETs. The abrupt decrease near V_{GS} of 0.5 V is due to the full depletion of the 20 nm thick body, which may lead to lower depletion capacitance for a given same area.

The C-V characteristics with the body doping concentration and fin width are shown in Fig. 9. Here shown are gate to substrate capacitance characteristics. These results were obtained by considering quantum effect in the channel. The gate capacitance in depletion region is reduced by reducing body doping and/or fin

width. From these data, we can determine the gate voltage that depletes the body fully. For example, the 50 nm with body doped with 1×10^{18} cm^{-3} is depleted fully at a V_{GS} of about −0.2 V. The V_{GS} for the 20 nm width body doped with 1×10^{19} cm^{-3} is about 0.6 V. The body which has width wider than 30 nm at a doping concentration of doped 1×10^{19} cm^{-3} does not deplete fully for the given V_{GS} up to 2 V.

IV. Conclusion

Extensive 3-dimemsional device simulations have been performed to give the design guide of the body-tied FinFETs (Ω MOSFETs). The fin body shape with right-angle vertical surfaces gives higher I_{on}/I_{off} ratio and lower DIBL. The control of the doping around top region of the fin body gives significant effect on the leakage and the threshold voltage. The source/drain contact resistance in the Ω MOSFETs can be reduced by making the contact on the vertical surfaces and the top of the fin body. Finally, C-V of the Ω MOSFETs was checked and gave some information on the complete body depletion.

Acknowledgment

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