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ASG(Amorphous Silicon TFT Gate driver circuit)Technology for Mobile TFT-LCD Panel

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Abstract

We developed an a-Si TFT-LCD panel with integrated gate driver circuit using a standard 5-MASK process. To minimize the effect of the a-Si TFT current and LC's capacitance variation with temperature, we developed a new a-Si TFT circuit structure and minimized coupling capacitance by changing vertical architecture above gate driver circuit. Integration of gate driver circuit on glass substrate enables single chip and 3-side free panel structure in a-Si TFT-LCD of QVGA (240 × 320) resolution. And using double ASG structure the dead space of TFT-LCD panel could be further decreased.

Keywords : TFT-LCD, Amorphous Silicon, Capacitance, Gate Structure, Deal Space

1. Introduction

In resent years, LCD displays for mobile application such as cellular phone and PDA are being developed rapidly in points of resolution, PPI, number of color and brightness. Furthermore, as the appearance of camera phone, the need of high resolution displays is much more increased so that QVGA (240×RGB×320) resolution LCD panel is now used as a main display for some advanced mobile phones. In AMLCD, there are two types of TFT technology, which are a-Si and LTPS(Low Temperature Poly Si). Until now a-Si TFT process have been main stream in TFT-LCD for mobile applications because of the cost merits due to simple process and high yield. But as the resolution increase over QVGA, standard a-Si TFT-LCD panel has more than 1000 external connection. On the other hand LTPS technology enables to integrate driver IC on glass substrate, so LTPS technology is expected to be main stream for high-resolution mobile display [1]. But in this paper we can implement a QVGA a-Si TFT-LCD panel with 1-chip, 3 side free architecture by integrating gate driver circuits on glass. In the previous paper [2,3], a-Si TFT-LCD panel with integrated gate and data driver circuits as like LTPS was already implemented, but could not be commercialized. The reason could be guessed that temperature reliability could not be guaranteed because of a-Si TFT on-current and LC capacitance variation with temperature. To overcome a-Si TFT and LC characteristic variation with temperature, we invented a new circuit structure and vertical architecture.

2. a-Si TFT Characteristic Variation with Temperature

As shown in Fig. 1 on-current of a-Si TFT is proportional to temperature. The on-current of TFT at -20 ℃ is only half of on-current at 25 ℃. So if gate driver circuit can be made with a-Si TFTs, it must have

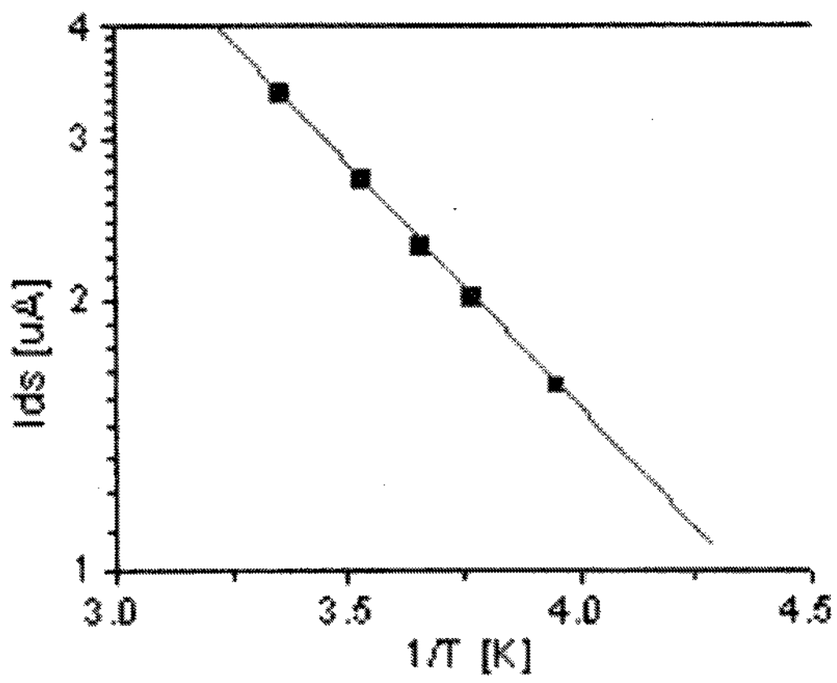

Fig. 1. a-Si TFT On-current Variation with Temperature.

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enough operation margin with TFT on-current to guarantee circuit operation in wide temperature range. But the mobility of a-Si TFT is generally limited to only 0.4~1 cm/Vsec at room temperature and even lower at low temperature range. To improve gate circuit operation in low-temperature range, we have to minimize parasitic capacitance around gate driver circuit area, gate circuit output load capacitance, and also improve gate circuit architecture.

3. Liquid Crystal Capacitance Variation with Temperature

Generally, it is well known that LC's dielectric constant increases with decreasing temperature. But as shown in Fig. 2 LC's dielectric constant have peak around 0°C at the frequency of several KHz which is the driving frequency of gate driver circuit. Between the area of built-in gate circuit fabricated by amorphous silicon TFT process and ITO electrode of color filter, there is LC layer acting as RC delay component of gate driver circuit. So considering the fact that the on-current of a-Si TFT decreases and LC's dielectric constant increase with temperature going down, the malfunction of gate circuit around 0 °C can be explained because the gate line delay increases with temperature going down.

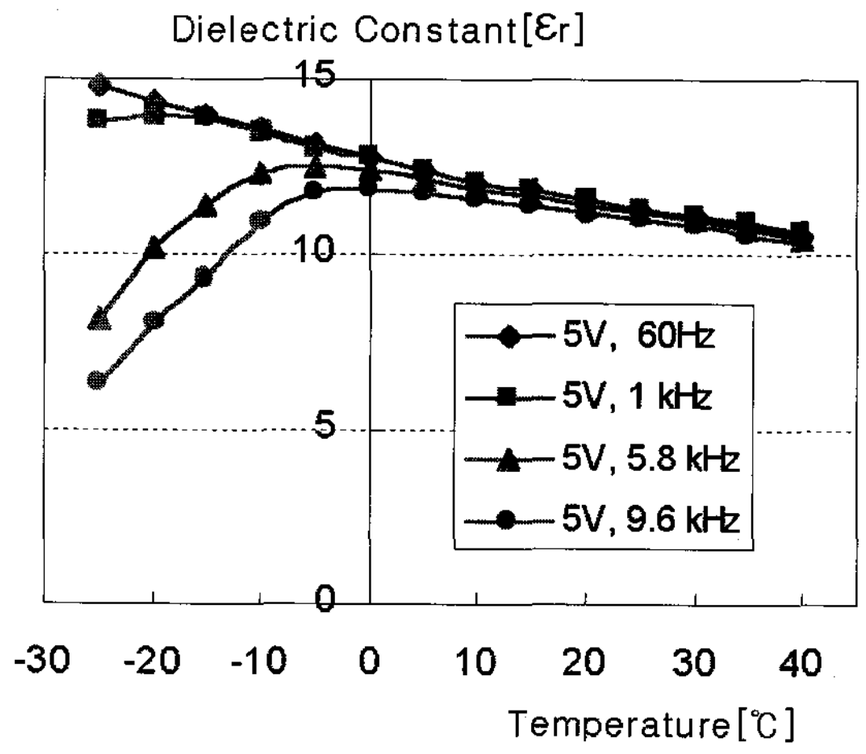

Fig. 2. LC Dielectric constant variation with temperature.

4. The effect of Liquid Crystal Capacitance on Gate Driver Circuit

In the first working sample, Liquid Crystal is located on the gate driver circuit area as shown in Fig. 4(a). So the LC above gate circuit forms capacitor with color filter ITO electrode. Dielectric constant of LC on gate driver circuit is over 10 in high electric field as explained earlier, so the big capacitor formed by LC can make delay in gate circuit operation. To prove out that theory, we eliminate color filter ITO electrode on gate circuit and the results are shown in Fig. 3. The rising delay time of gate output pulse with color filter ITO electrode is 15 us but only 3 us without color filter ITO electrode. With the experimental result, we must reduce LC coupling capacitance between gate circuit and color filter ITO electrode to improve gate circuit operation. By locating seal material, whose dielectric constant is 3, on gate circuit, we can reduce 70 % of total coupling capacitance as shown in Fig. 3.

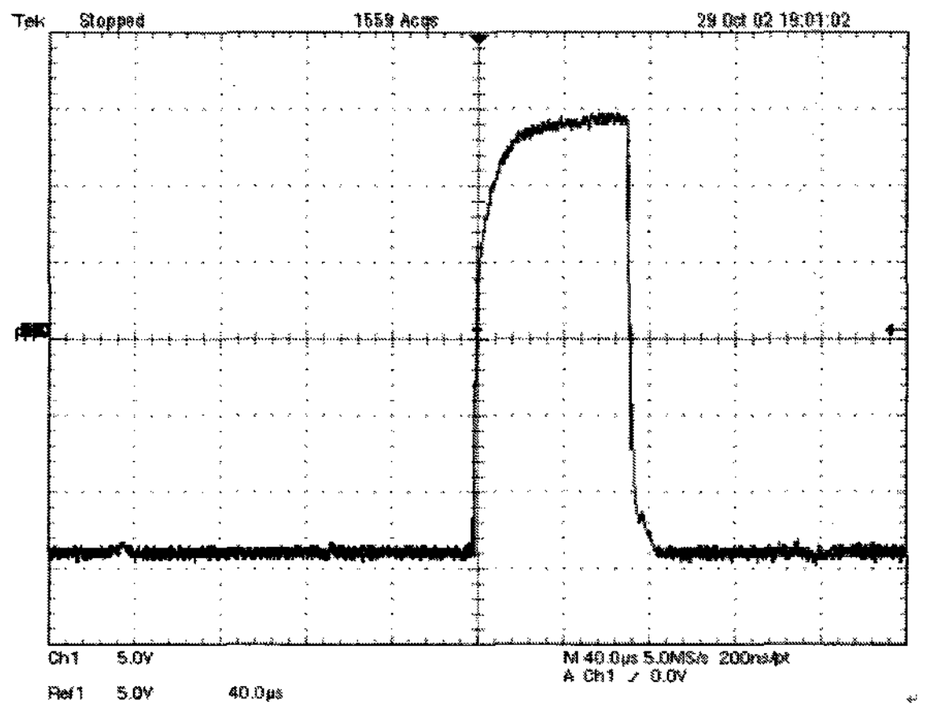

Fig. 3. Gate output pulse waveform, (a) With color filter ITO electrode, (b) Without color filter ITO electrode

5. Improving Gate Driver Circuit Structure

Gate driver circuit output is connected to gate line of panel. Gate line is electrically consisting of capacitor and resistor. So the gate circuit output connected to a gate line has RC delayed waveform and delay time is proportional to RC of the gate line. Usually gate circuit output is also connected to next gate circuit block and functions as carry signal. If the delayed gate output pulse is transferred to next gate circuit, the delay can be accumulated as the number of gate circuit block is increased. Especially at the low temperature operation, on-current of a-Si TFT is decreased, so those delay accumulation is much more increased and gate circuit operation can be stopped in worst case.

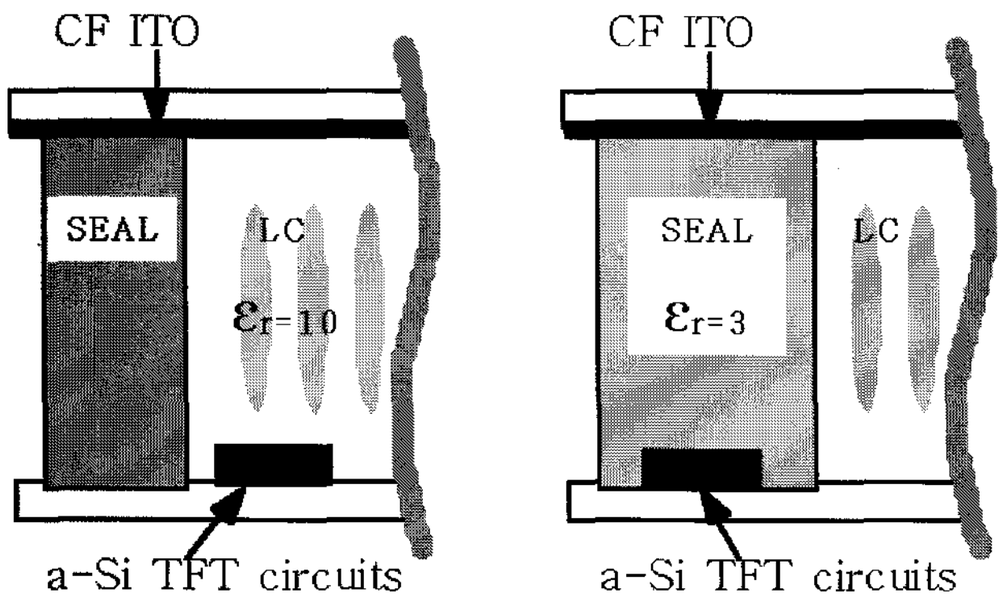

Fig. 4. Vertical structure on a-Si TFT Gate circuits; (a) Liquid crustal on gate circuits, (b) Seal material on gate circuits.

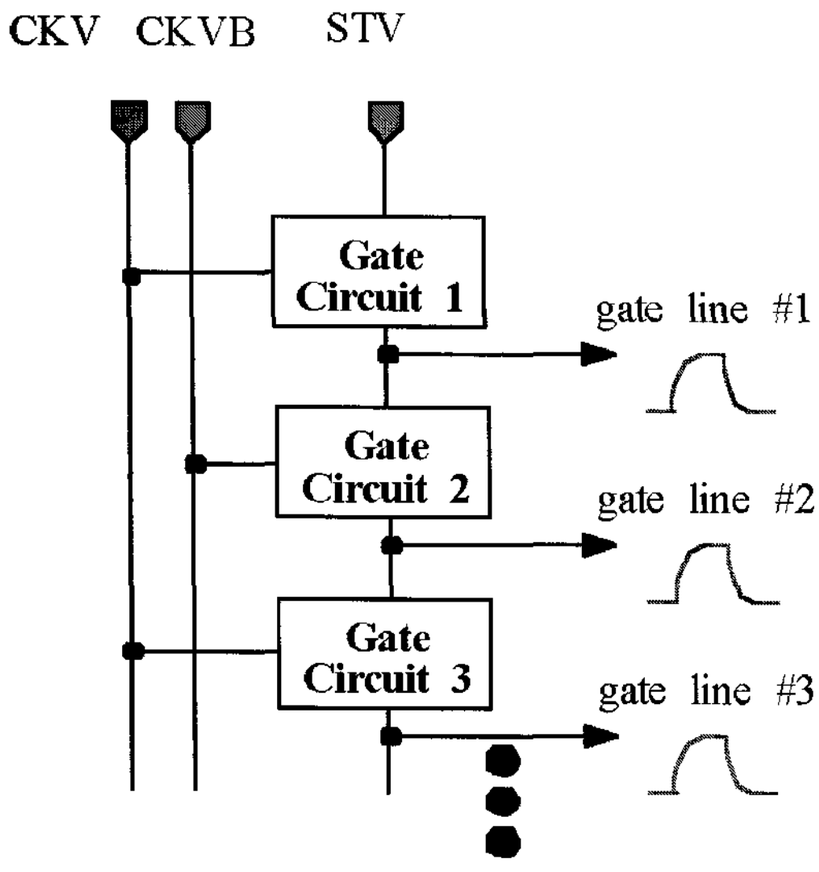

Fig. 5. Conventional a-Si TFT gate circuit structure

In improved a-Si gate circuit structure in Fig. 6, gate circuit output for gate line and carry signal is separated to reduce the delay of carry signal and delay accumulation can be eliminated. So with this new structure and improved vertical architecture in Fig. 4(b), reliability of low temperature operation can be guaranteed.

6. TFT-LCD Panel Structure with Built-in ASG (Amorphous Silicon TFT Gate driver circuit)

TFT-LCD panel with ASG technology was already announced by our previous work [4], but in this paper we developed double ASG structure as shown in Fig. 7. By locating ASG both side of active display area, we can

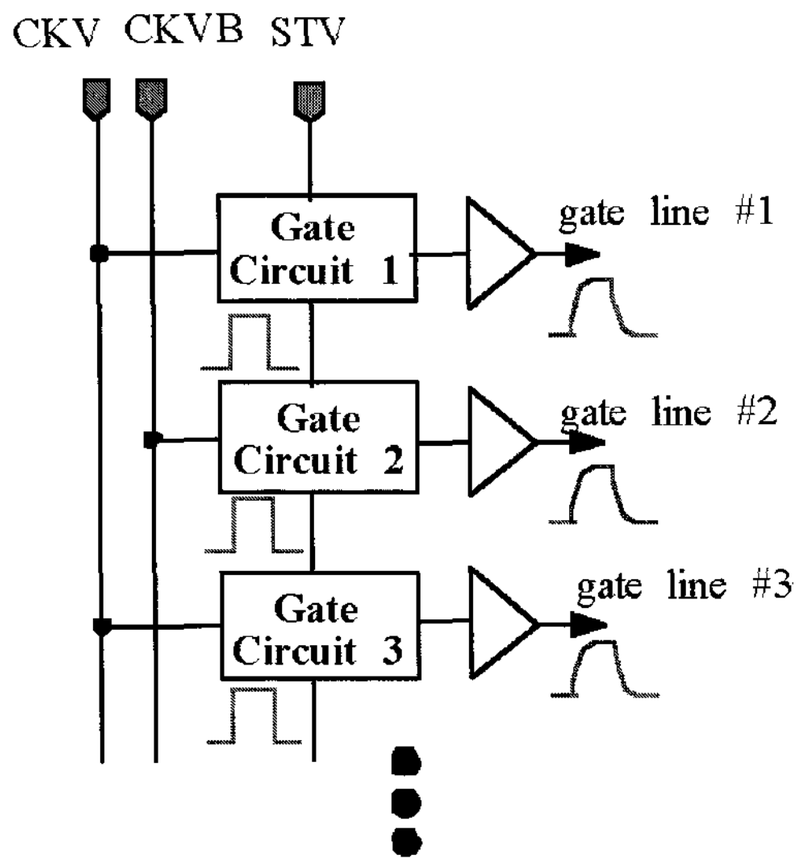

Fig. 6. Improved a-Si TFT gate circuit structure.

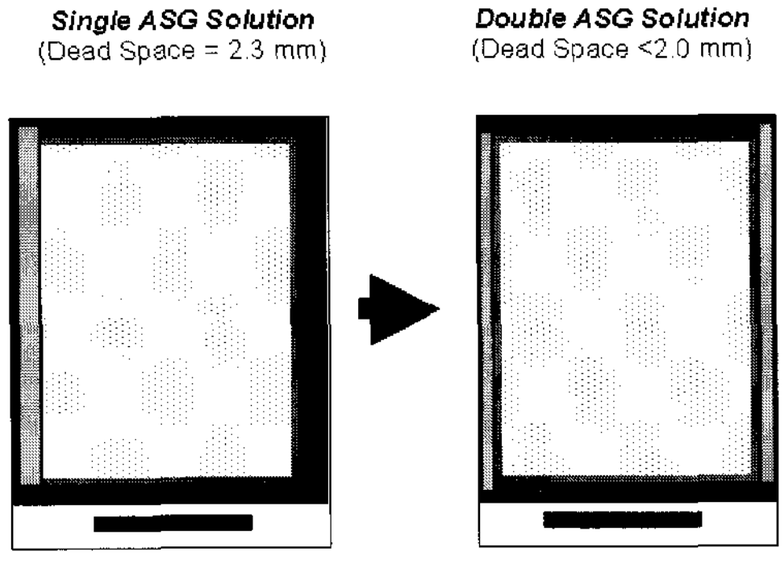

Fig. 7. ASG TFT-LCD panel structure; (a) Single ASG structure, (b) Double ASG structure.

reduce side dead space of the panel within 2 mm.

ASG(Amorphous Silicon Gate driver circuit) needed only 3 signals and 2 power lines which is the most simple interface than previous circuit structures [2,3]. So all signal generation components including power supplies for gate scanning circuit can be integrated inside single chip driver IC with easy as shown in Fig. 8.

This ASG panel architecture is almost same module architecture as the commercial LTPS products which use one or two driver IC. All the gate driver circuit can be integrated in side dead space area is minimized by double ASG technology. So with ASG panel structure we sure that a-Si TFT-LCD will be superior to LTPS TFT-LCD in panel cost, and the same in module cost in high-PPI mobile display. And we also sure that this panel structure can be extended to VGA resolution, 300 ppi panel by placing ASG units both side of panel.

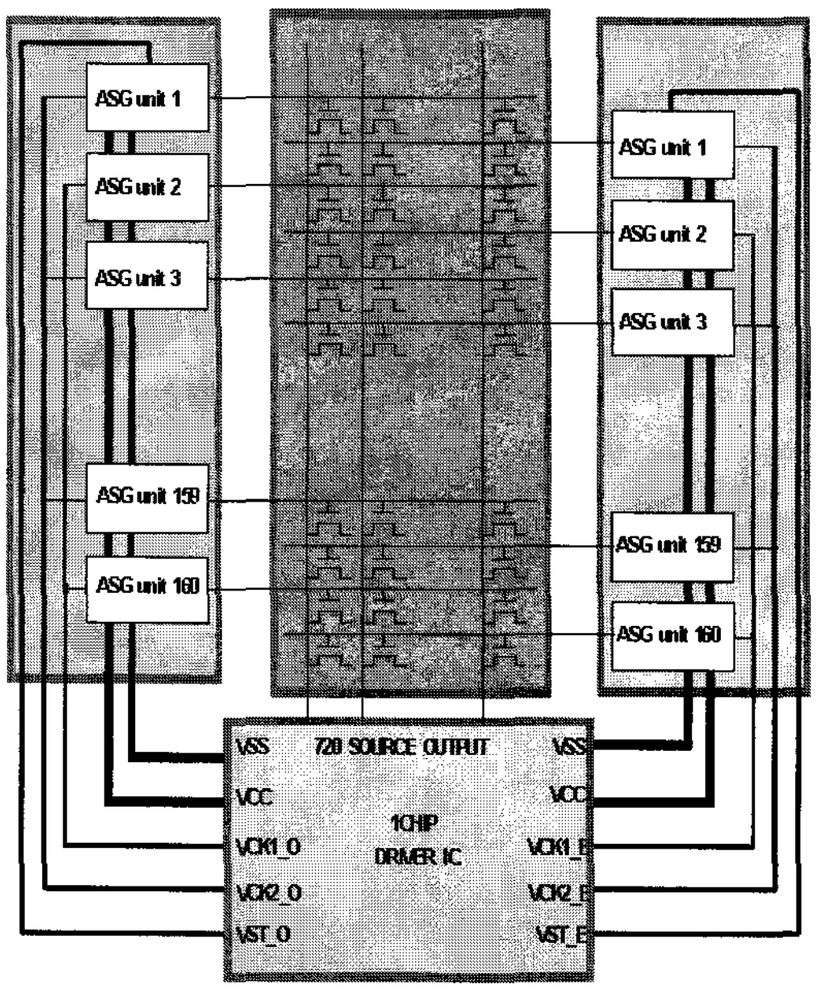

Fig. 8. Block diagram of QVGA panel with ASG.

PIN Name	Description
VGH	Power Supply (Gate On Voltage)
VGL	Power Supply (Gate Off Voltage)
VST_O, VST_E	Start Signal for ASG
VCK1_O, VCK1_E	Clock 1 for ASG
VCK2_O, VCK2_E	Clock 2 for ASG

Fig. 9. Power supplies and signals for ASG.

7. Specification of a New TFT-LCD PANEL with ASG

QVGA resolution a-Si TFT-LCD panel with ASG is manufactured with standard 5-MASK a-Si TFT-LCD process with no additional process. 320 gate circuit blocks are integrated at the both side of display area and all the other components to drive TFT-LCD panel such as power block, source driver circuit, timing controller, and signal level shifter for gate circuit are integrated in a single chip.

	Specification
Panel size	2.0" Diagonal
Resolution	QVGA (240 × RGB × 320)
PPI(Pixel Per Inch)	200ppi
AMLCD device	a-Si TFT
Optical Mode	TMR (Transmissive with Micro Reflective)
Brightness	150 cd/m²
Contrast Ratio	300:1
Driver IC	COG type 1 chip (Power block, Source driver circuit, Signal level shifter for gate circuit)

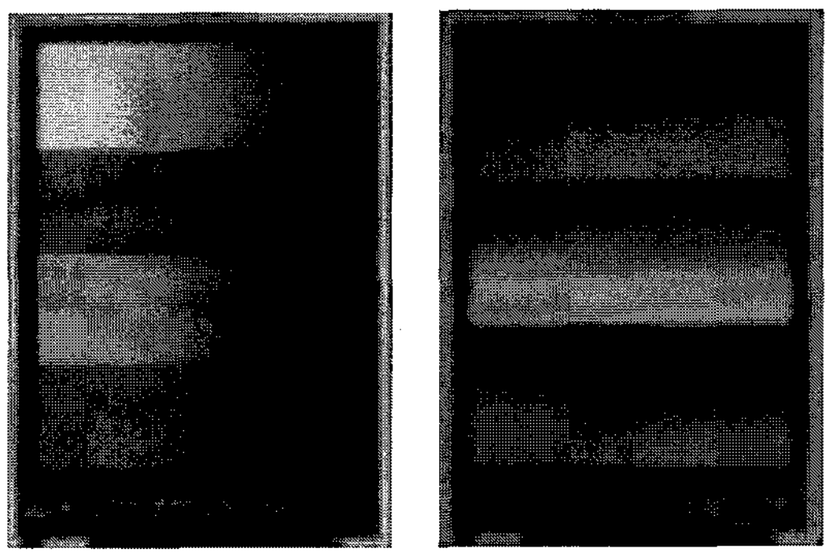

Fig. 10. Picture of QVGA a-Si TFT-LCD panel with ASG.

8. Conclusion

We developed a QVGA a-Si TFT-LCD panel with integrated gate circuit with standard 5-MASK process. To minimize the effect of the a-Si TFT current and LC capacitance variation with temperature, we improved circuit architecture and minimized coupling capacitance by changing vertical structure above the gate circuit. Integration of gate circuit on glass enables one chip and 3-side free panel architecture a-Si TFT-LCD. And using double ASG structure the dead space of TFT-LCD panel can be reduced to 2.0 mm.

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