Characteristics of poly-Si TFTs Required for System-on-Glass Analog Circuits

Dae-June Kim[**], **Kyun-Lyeol Lee, and Changsik Yoo**

Abstract

In this paper, we investigate on the characteristics of poly-Si TFTs reuired for the implementation of analog circuits to be integrated with System-on-Glass (SoG). Matching requirements in terms of resistor values, threshold voltage and mobility of poly-Si TFTs are derived as a function of the resolution of display system. Effective mobility of poly-Si TFTs required for the realization of source driver is analyzed for various panel sizes.

Keywords : poly-Si TFTs, analog circuits, System-on-Glass

1. Introduction

Since poly-silicon thin film transistors (poly-Si TFTs) outperforms amorphous-silicon thin film transistors (a-Si TFTs), there have been many efforts to realize driver circuits and pixel arrays on a single glass substrate with poly-Si TFTs [1-4]. The ultimate goal is to develop a System-on-Glass (SoG) as shown in Fig. 1, which is expected to reduce the cost of flat panel display system and increase the yield through the PCB (printed circuit board)-less assembly and simple module process.

For SoG, various kinds of analog and digital circuits need to be implemented with poly-Si TFTs whose performance is still inferior to that of single-crystal transistors. Moreover, due to irregular grain boundaries of poly-Si TFTs, threshold voltage and mobility are not uniform, and therefore the characteristics of analog circuits built with poly-Si TFTs may be different from location to location in a panel, making it difficult to achieve high resolution display. Moreover, the kink effect deteriorates the performance of analog circuits [5].

In this paper, allowable mismatch of poly-Si TFTs characteristics is derived as a function of the resolution of display system. Effective mobility required for the realization of source driver is analyzed for various panel sizes, and these results have been verified through HSPICE simulation.

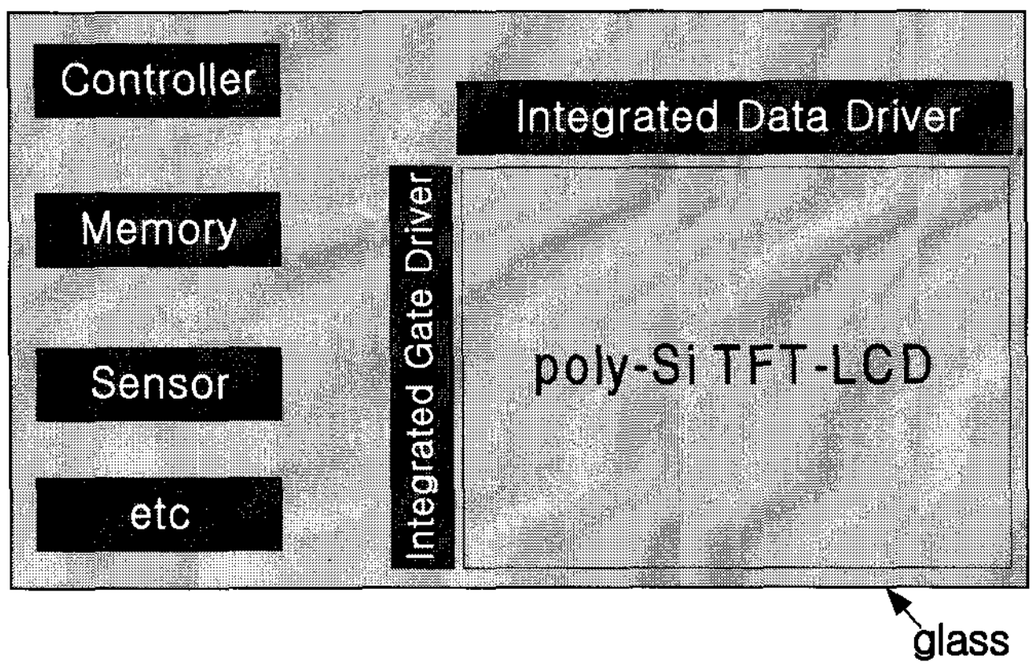

Fig. 1. System-on-Glass.

2. Resistance Matching of Resistor-string Type Digital-to-Analog Converter

Resistor-string type digital-to-analog converter (DAC) in Fig. 2 is most widely used to convert the digital video data into analog video signal with gamma correction capability. With this type of DAC, the achievable resolution of display system is determined by the mismatches in the resistor values. The full scale analog voltage is 5.8V and thus one least significant bit (LSB) value can be expressed as $\frac{\text{full scale analog voltage}}{2^n} = \frac{5.8\,\text{V}}{2^n}$, where n is the bit-depth of DAC. Therefore, 1/2LSB values of 4-, 6-, and 8-bit DAC are 181mV, 45.3mV, and 11.3mV, respectively. However, since Voltage-Transmittance (VT) of LCD device has S-shaped curve [6], gamma-corrected 1/2LSB values of 4-, 6-, and 8-bit DAC are 107.3 mV, 25.4 mV, 3.7 mV, respectively;

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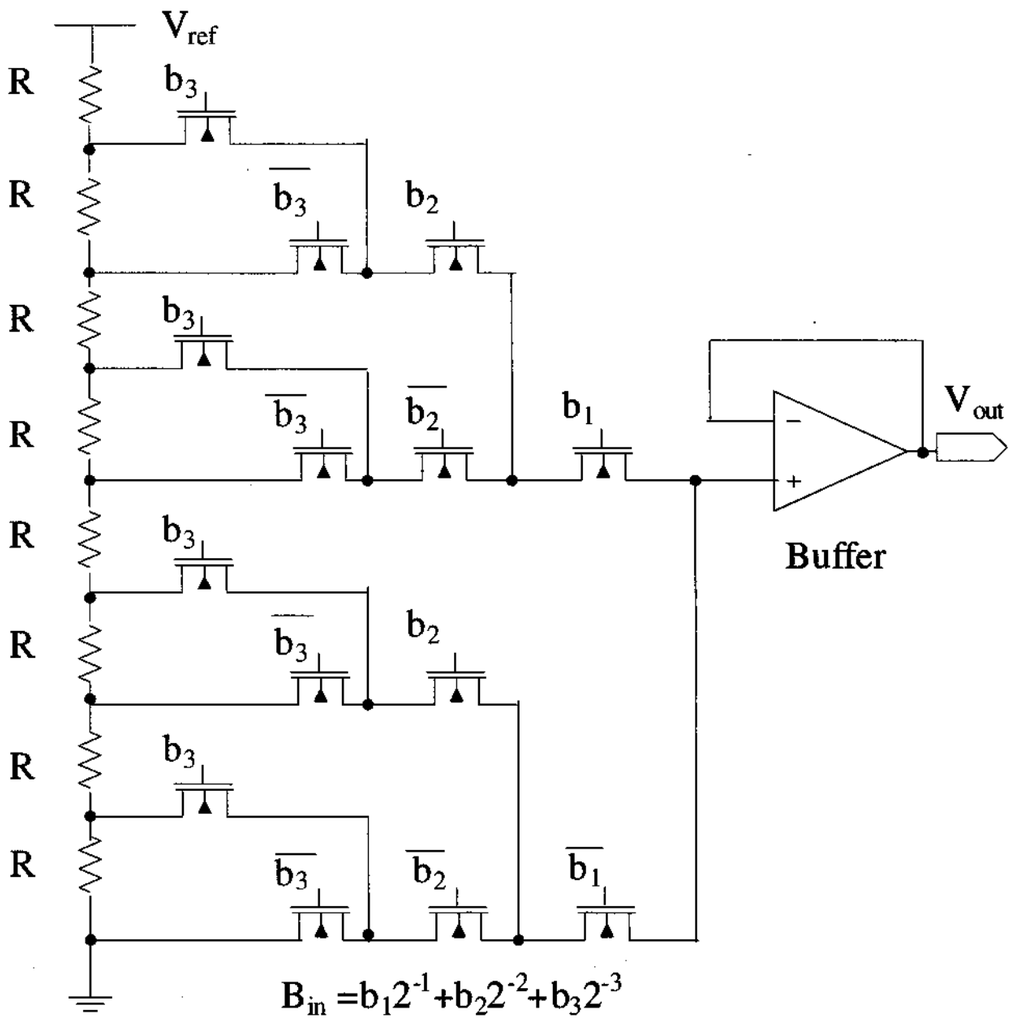
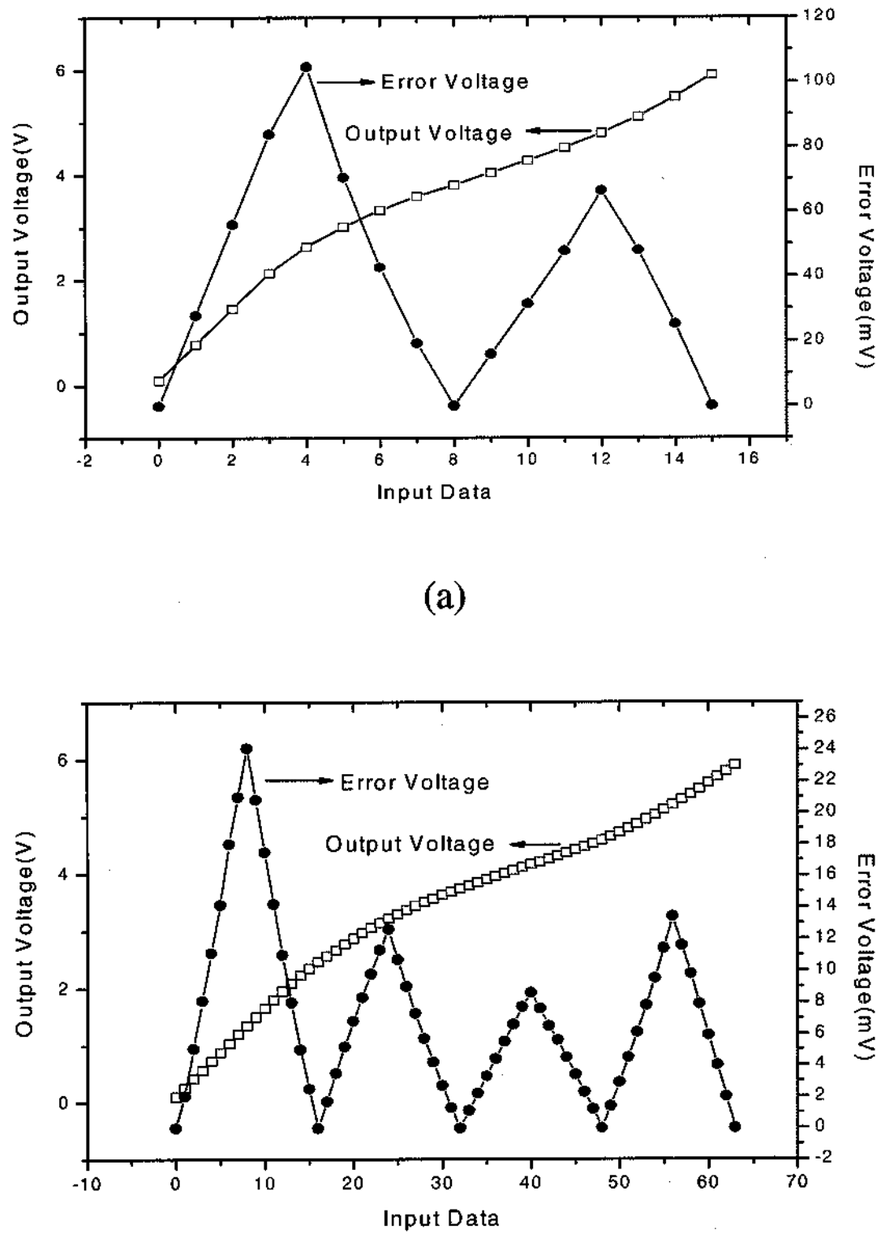


Fig. 2. Resistor-string type 3-bit DAC.

gamma-corrected 1/2 LSB values are obtained by simulation results, as shown in Fig. 3. These values are the allowable error, ΔV, in the output voltage of DAC. For the display resolution of 4-, 6-, and 8-bit, the required matching accuracy of resistor values according to ΔV are 12 %, 4 %, and 1 %, respectively. These results shown in Fig. 3 have been obtained by HSPICE simulation. The key parameters of poly-Si TFT used for the simulation are V_{th} = 1.68V, μ = 42.4 cm^2/Vs for n-type TFT and V_{th} = -0.96 V, μ = 12 cm^2/Vs for p-type TFT.

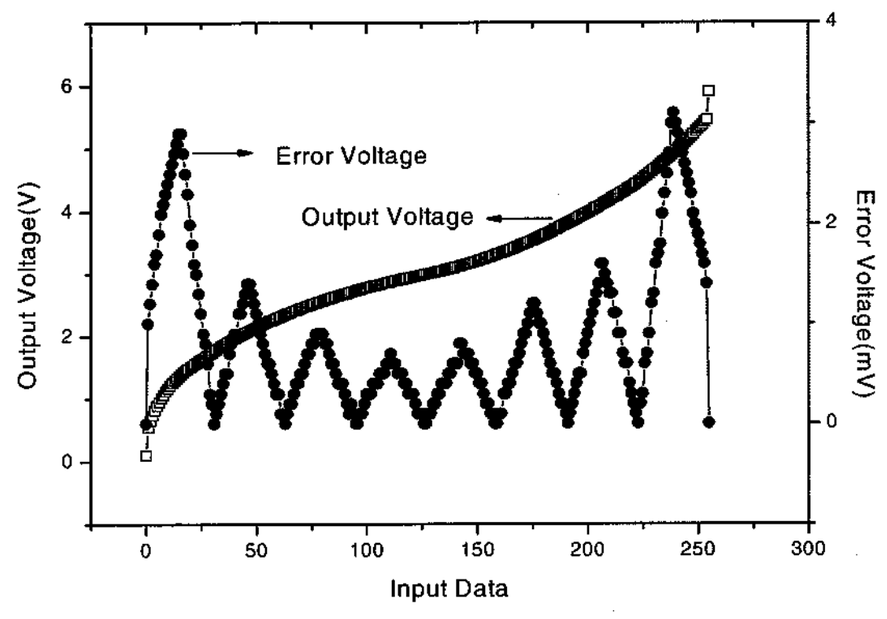
3. Allowable Mobility and Threshold Voltage Mismatch of poly-Si TFTs

For data line driving of liquid crystal displays (LCDs) panel, the operational amplifier (op-amp) implemented with a single crystal transistor is widely used by configuring it as a unity gain buffer [7-8]. Two-stage op-amp in Fig. 4 is the most popularly used circuit, and therefore, has been chosen as a reference circuit in driving the required performance of poly-Si TFTs in this study. Due to the irregular grain boundaries, op-amp built with poly-Si TFTs has a much larger offset voltage than the one on a single crystal substrate. To compensate for this offset, an offset compensated unity-gain buffer as shwon in Fig. 5 is normally used. During the offset detection period, the



(a)

(b)



(c)

Fig. 3. Simulation results of resistor-string DAC for (a) 4-bit with resistor-variation of 12 %, (b) 6-bit with resistor-variation of 4 %, and (c) 8-bit with resistor-variation of 1 %.

switches SW1 and SW3 are turned on, and then the offset voltage is stored in a capacitor C_{offset}. During the driving period, the switches SW2 and SW4 are turned on, and then the output becomes $V_{in} + V_{offset} - V_{offset} = V_{in}$, which is independent of the op-amp offset voltage.

Allowable mobility and threshold voltage mismatch with and without offset compensation were investigated as

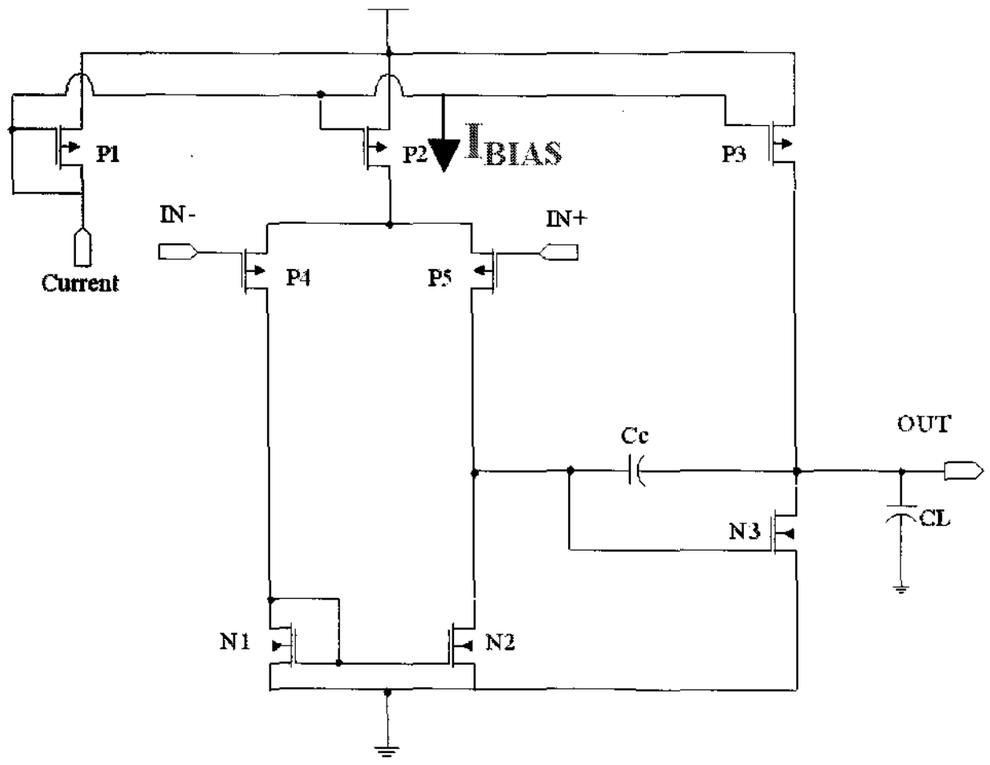


Fig. 4. Two-stage op-amp.

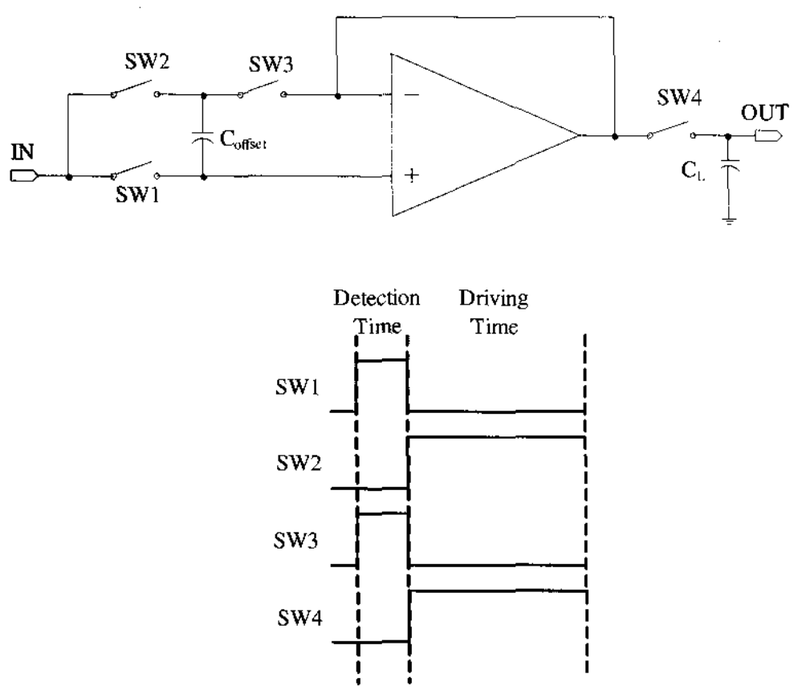


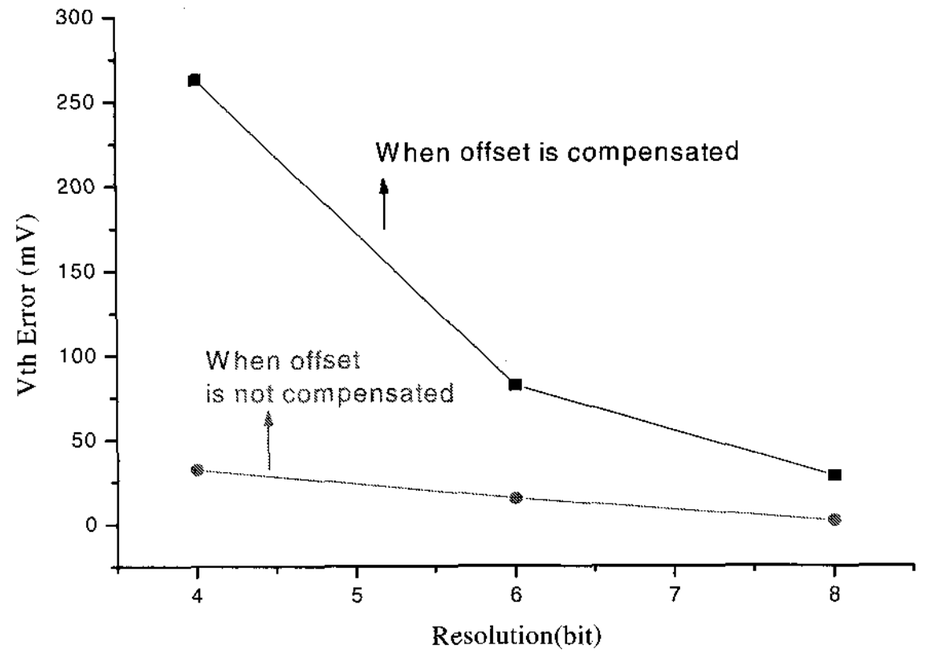
Fig. 5. Offset compensated unity-gain buffer and its timing diagram.

a function of display resolution, assuming that the total capacitance of data line was 30 pF and video voltage range is 5 V. Fig. 6 shows the allowable variations of threshold voltage and mobility as a function of the display resolution.

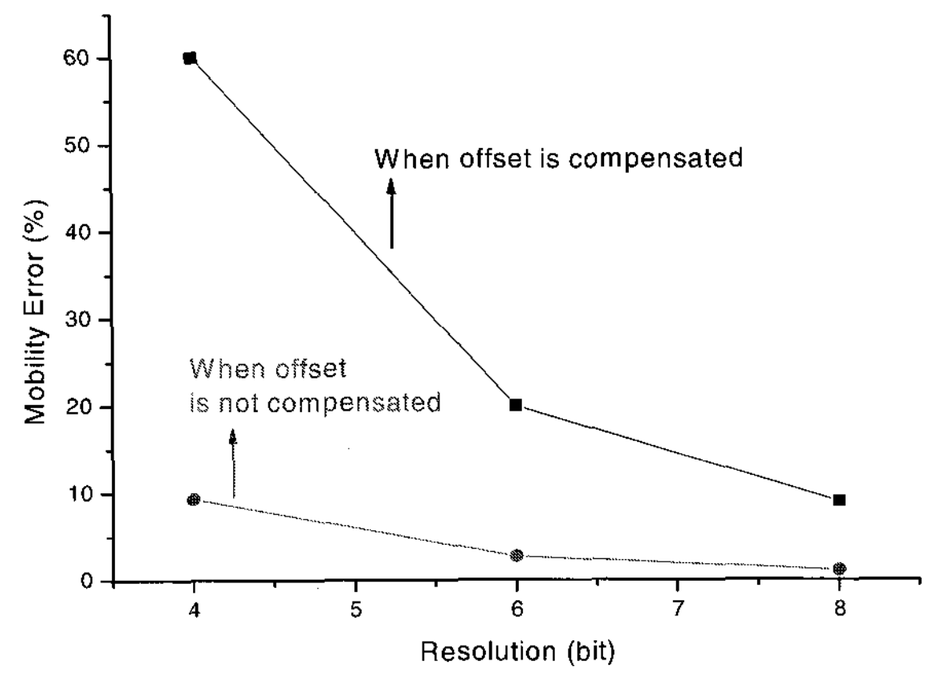
4. Required Effective Mobility

For larger panel size and better resolution format, the performance requirements on source driver become much more stringent. The most critical performance parameter is the data line charging time, because with larger panel size and better resolution format, the line time becomes shorter while the data line loading becomes heavier.

The required effective mobility of poly-Si TFTs was



(a)



(b)

Fig. 6. Allowable (a) threshold voltage and (b) mobility error with and without offset compensation.

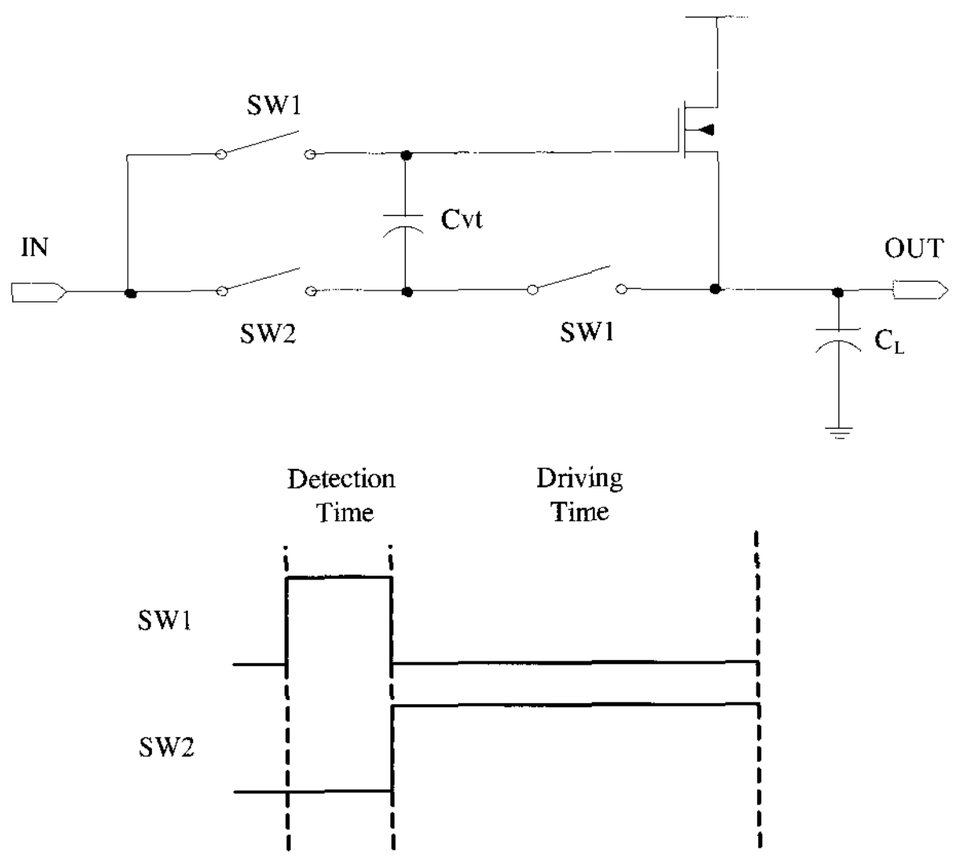


Fig. 7. V_{th}-mismatch compensated analog buffer and its timing diagram.

analysed for two types of source driver; (1) offset compensated unity-gain buffer in Fig. 5 and (2) V_{th}-mismatch compensated analog buffer in Fig. 7.

4.1 Unity gain buffer as source driver

The slew rate of op-amp as shown in Fig. 4 is the maximum achievable time derivative of the output voltage variation, and its value was determined by the maximum current available for charging or discharging the load capacitance. In order to drive the signal lines of LCDs panel, the slew rate of op-amp should be larger than the maximum video signal range divided by one row line time. It is evident that the bias current of op-amp used as a source driver should be increased for larger panel size and/or better resolution format. Therefore, the bias current of input differential stage of op-amp, which is the current in transistor P2 in Fig. 4, can be calculated by the equation (1), where C_c is the compensation capacitor whose value is chosen to be $0.22C_L$ to allow sufficient phase margin, γ is a constant determined by equation (2) and its value is approximately 7.64. The calculation results are listed in Table 1.

$$\left[\text{Slew Rate} = \frac{I_{BIAS}}{C_C}\right] \geq \left[\frac{\text{Gray Full Swing Range}}{\text{Line Time}}\right]$$

$$\text{Line Time} \geq \left[\frac{C_C}{I_{BIAS}}\right] \text{Gray Full Swing Range}$$

$$\text{Line Time} \approx \left[\frac{C_C}{I_{BIAS}}\right] \text{Gray Full Swing Range} \times \gamma$$

$$I_{BIAS} = \left[\frac{\text{Gray Full Swing Range}}{\text{Line Time}}\right] C_C \times \gamma \quad (1)$$

$$\gamma = \left[\frac{\text{Settling time of unity - gain buffer in Fig. 5}}{\text{Slewing time of unity - gain buffer in Fig. 5}}\right] \quad (2)$$

Larger bias current can be obtained by larger device size, but since the source driver must fit inside one pixel pitch, the maximum device size is limited. For the integration of op-amp in one pixel pitch, the transistor width of op-amp should be decreased if required. For

Table 1. Required bias current

Panel size (inch)	Resolution format	Line time (μs)	Compensation capacitor Cc (pF)	Load capacitor C_L (pF)	**Bias current I_{BIAS} (μA)**
3.8	QVGA (320×240)	69	6.6	30	**12.5**
5.5	QVGA (320×240)	69	8.8	40	**16.6**
8.4	VGA (640×480)	34	15.4	70	**62.8**
10.4	SVGA (800×600)	27	22	100	**117**
14.1	XGA (1024×768)	21	33	150	**237**
17	SXGA (1280×1024)	16	42.46	193	**433**
21	UXGA (1600×1200)	13	61.38	279	**834**

Table 2. Ratio of op-amp transistor width to be decreased

Panel size (inch)	Resolution format	Sub-pixel pitch (μm)	Source driver area for op-amp (μm^2)	Area of op-amp (μm^2)	**Ratio of op-amp transistor width to be decreased β**
3.8	QVGA (320×240)	80	28,000	172320	**1/6.2**
5.5	QVGA (320×240)	116	58,000	172320	**1/3**
8.4	VGA (640×480)	88	67,760	172320	**1/2.6**
10.4	SVGA (800×600)	88	84,216	172320	**1/2.1**
14.1	XGA (1024×768)	94	122,012	172320	**1/1.5**
17	SXGA (1280×1024)	87	135,720	172320	**1/1.27**
21	UXGA (1600×1200)	88	170,210	172320	**1/1.02**

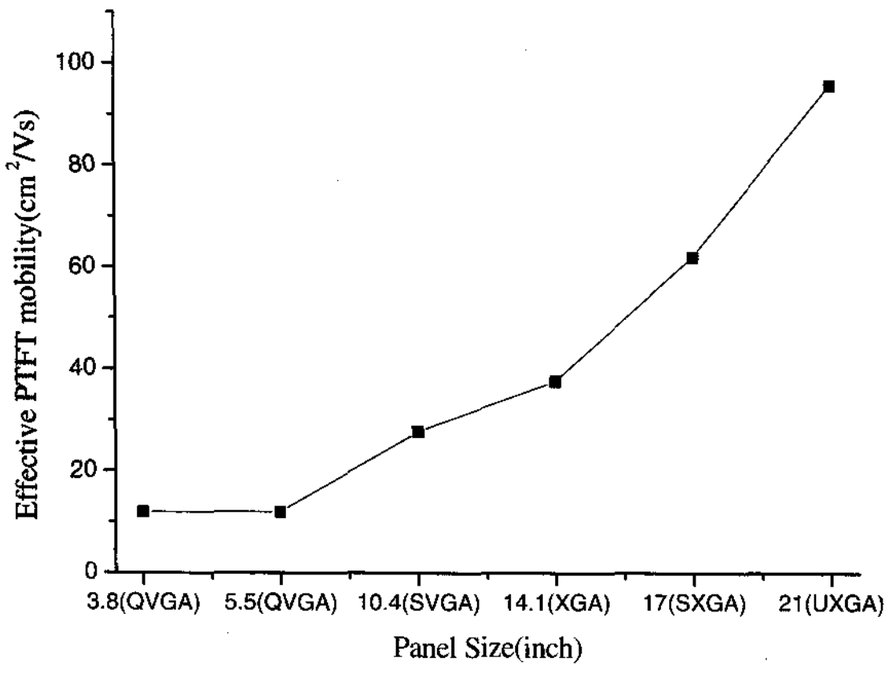


Fig. 8. Effective mobility vs. panel size when offset compensated unity-gain buffer in Fig. 5 was used as source driver.

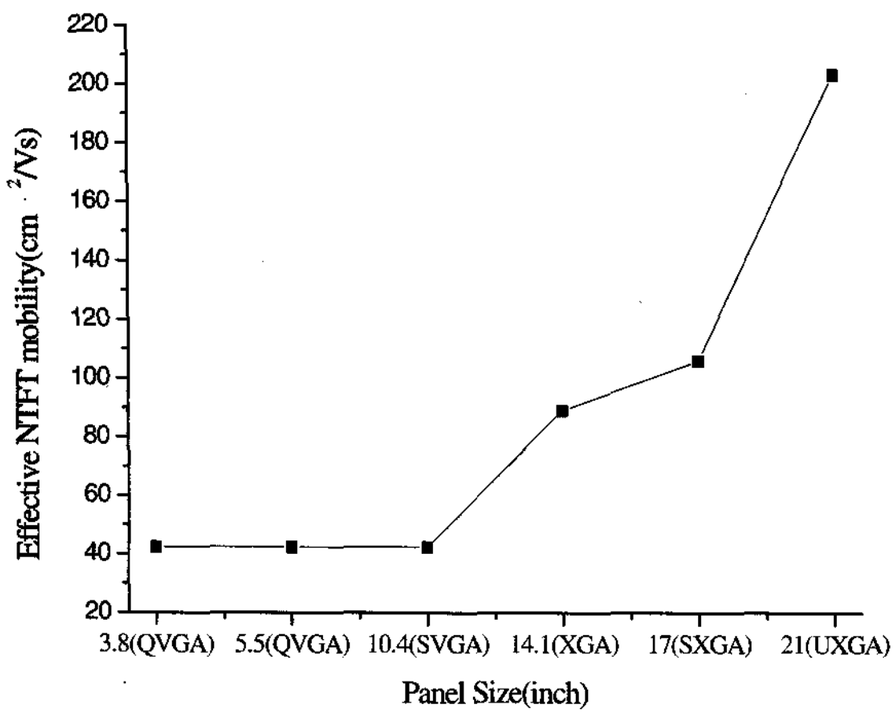


Fig. 9. Effective mobility vs. panel size when V_{th}-mismatch compensated analog buffer in Fig. 7 is used as source driver.

transistors with smaller width, the effective mobility of transistors should be improved for larger bias current. For a given panel size and resolution format, the device size is increased until either it is limited by the one pixel pitch or the required bias current is obtained. If the resultant bias current need to be further increased, the effective mobility is increased until the required bias current is obtained. The required effective mobility can be calculated by equation (3), where α is the ratio of effective mobility to be increased, β is the ratio of op-amp transistor width to be decreased (its values are listed in Table 2), and $\mu_p C_{ox}$ is a constant determined by the processing technology whose nominal value of the reference technology is 1.33 $\mu A/V^2$. The aspect ratio $\left(\frac{W}{L}\right)_2$ and the overdrive voltage $(V_{GS2} - V_{th})$ are (540/8) and 1.54 V, respectively.

$$I_{BIAS} = \frac{1}{2}(\alpha\mu_p C_{ox})\left(\frac{W}{L}\right)_2 \beta (V_{GS2} - V_{th})^2$$
$$\alpha = \frac{2I_{BIAS}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_2 \beta (V_{GS2} - V_{th})^2} \quad (3)$$

Then, α can be calculated by equation (3). Finally, the required effective mobility is determined by $\alpha\mu_p$, where μ_p of the reference technology is $12cm^2/Vs$. The result is shown in Fig. 8.

4.2 Analog buffer as source driver

As clearly demonstrated by the result in the pervious section, it is difficult to use unity-gain buffer as a source driver with poly-Si TFTs. An alternative to the unity-gain buffer is a simple analog buffer. Various kinds of V_{th}-mismatch com-pensated analog buffer [9-12] have been proposed among which the one in Fig. 7 [9] was chosen to derive the required effective mobility of poly-Si TFTs in our research. The analog buffer shown in Fig. 7 has two phase-clocks; SW1 and SW2. When SW1 is high, the voltage across the capacitor C_{vt} is the threshold voltage (V_{th}) because the transistor is turned off during that period. When SW2 goes high, the output becomes $V_{in} + V_{th} - V_{th} = V_{in}$, that is, the output is the same as the input regardless of the V_{th} variation.

For a given panel size and resolution format, the required effective mobility was obtained by HSPICE simulation. The supply voltage was 15 V and the load capacitor of data line according to panel size is listed in Table 1 and the results are shown in Fig. 9. Compared with the results in Fig. 8, the required effective mobility is about two times greater than analog buffer used as a source driver, because the driving source impedance of the analog buffer in Fig. 7 becomes very large as the output voltage approaches the final value. This is the inherent characteristic of source follower.

5. Conclusion

The characteristics of poly-Si TFTs required for the implementation of analog circuits for SoG were described. For SoG, the poly-Si TFTs technology should have a higher

effective mobility, lower threshold voltage and finer design rule and uniformity characteristics from location to location in a panel. Also, the performance of analog and digital circuit should be immune to the variation of poly-Si TFTs parameter.

More researches are being conducted on the SoG with poly-Si TFTs due to its feasibility of much cheaper flat panel display system. It is expected that this work will provide guidelines to developing poly-Si TFTs devices for SoG.

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