An Approach for Designing a UMTS and CDMA2000 Dual Standard Compatible Baseband ASIC

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Abstract

The Third Generation (3G) cellular mobile communication systems aim at providing higher data rates, improved quality of service, support for multimedia applications and global roaming. Cdma2000 and Universal Mobile Telecommunication System (UMTS) have emerged as two leading 3G standards in USA and European countries, respectively. Both the standards are capable of delivering high bandwidth data, voice and multimedia services to users of mobile equipment, but are not directly interoperableand are not available across different geographic areas, due to which global roaming is not possible in true sense of using single mobile equipment. However, both UMTS and cdma2000 are based on wideband code division multiple access (WCDMA) as the access method. Due to this, there exist some inherent commonalities between them. In this paper we will try to exploit the commonalities between the two standards in order to design an ASIC, which can provide dual standard capability. This paper discusses the physical layer aspects of the two standards and proposes an approach to design an ASIC which can be mapped to baseband processing part of the physical layer and is capable of delivering for either of the two aforementioned standards.

1. INTRODUCTION

As the number of wireless handheld devices designed to access the Internet increases, there is a serious need for a faster and better wireless communications technology. The third generation wireless technology will provide superior voice quality and data services, supporting video and multimedia content sent without wires

to laptops, handhelds, smart phones, and potentially many other electronic devices. The 3G wireless access and mobility will be merged with the internet to create new business opportunities and new services. Therefore, it has the potential to be the nucleus of new services for the end users.

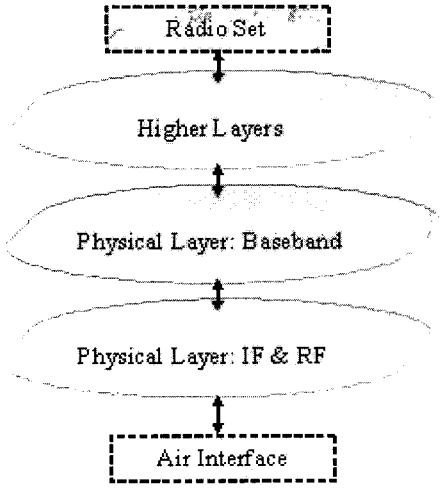
Cdma2000 and UMTS were developed separately and are two separate ITU approved 3G standards. Both these standards are based on (WCDMA) as the access method [1,2] in view of its several advantages such as ability to yield a good performance in the context of fading [3], ability for narrowband interference rejection and support for different data rates as well as multiple users. Cdma2000-1x and cdma2000-3x were developed to be backward compatible with IS-95B and it has already been implemented as an evolutionary step from cdmaOne. UMTS was developed by 3GPP (Third Generation Partnership Project). These systems have a complex physical layer, which is essential in view of the requirements such as support for different transmission speeds, backward compatibility and other involved complicated mathematical operations.

The computational complexity of a 3G baseband processor is huge and with the present state-of-artVLSI technology, it is very difficult to provide full speed processing in the form of a software solution on a digital signal processor and an ASIC solution is essential. The existing chip development efforts towards CDMA wireless solutions include systems developed by companies like Qualcomm, Phillips and LSI Logic. While some of these are ASIC's the others use a DSP core and a general-purpose system core. These solutions offer only low and mid-tier CDMA solutions. For instance the MSM6050 chipset of Qualcomm is designed for CDMA2000 1X and it is a mid-tier 3G solution (153 kbps), which works with a Zero IF direct conversion architecture [4]. Development of a full speed baseband processor is very useful and essential for a miniaturized 3G-air interface development.

Section 1 contains an introduction to the subject of the paper. Section 2 presents a brief overview of the physical layer and its interconnections with other layers. Section 3 presents the system architecture of the proposed dual standard baseband processor. Various units of the baseband processor have been described in section 4. Finally, the paper has been concluded in section 5.

2. A BRIEF OVERVIEW OF THE PHYSICAL LAYER

Physical layer functions can be divided into two parts: (i) Base Band processing (ii) IF & RF stage as shown in figure 1.

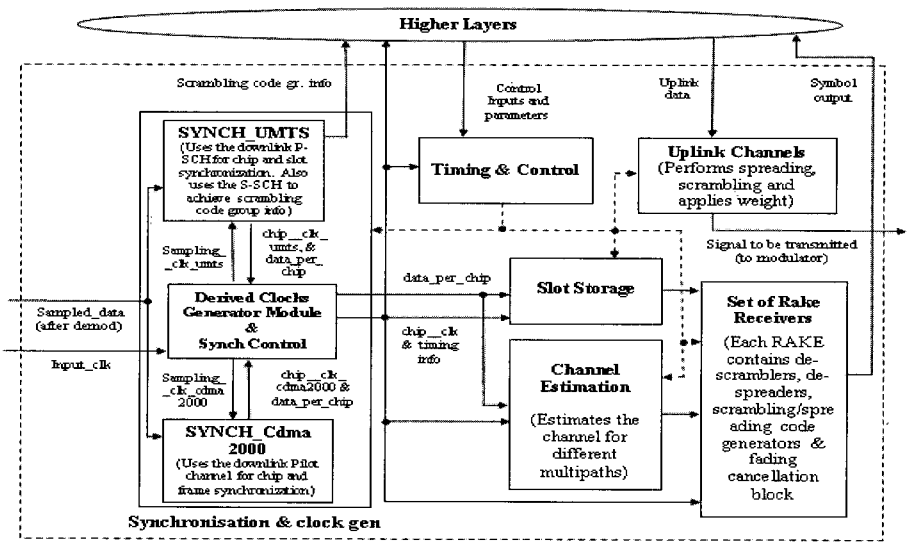


[Fig 1] Physical layer interconnections

In a typical implementation the higher layer functions can be performed by a micro-controller or a general purpose processor and the IF & RF physical layer functions are typically performed by separate ASIC(s). Here we will focus on baseband processing part of the physical layer. In both the standards the physical layer performs both uplink and downlink functions. For uplink it takes different physical channels (both dedicated and common channels) as input from higher layer(s) [5] and performs channelisation, relative channel gain weighting and scrambling. The process of channelisation preserves the orthogonality between the different physical channels scrambled using the same code and thus in turn enables the base station to separate out all the physical channels transmitted by the same user [6]. After channelisation, the real-valued spread signals are weighted by gain factors to provide relative channel gains among different physical channels. After the weighting, the stream of real-valued chips on the I and Q branches is then scrambled by complex-valued scrambling code [7]. Complex-valued chip sequence generated by the scrambling process is then QPSK modulated to generate the modulated output of baseband processor. For downlink the whole process in reversed i.e. demodulation, de-scrambling and de-spreading is performed in that order. In addition to that we need to do frame/slot synchronization, clock synchronization, multipath delay acquisition, channel response estimation and fading cancellation. A rake receiver is incorporated to exploit the multipath diversity.

3. SYSTEM ARCHITECTURE OF THE DUAL STANDARD BASEBAND PROCESSOR

Block diagram of the proposed dual standard baseband processor is shown in figure 2. Input data (demodulated data sampled at 16 times chip clock) is fed to the synchronization block. Synchronization block correlates this data with the reference sequence and locks itself with the base station (BS) whose received signal strength is maximum. In addition to that an early late bit correlator with an adaptive loop



[Fig 2] Block Schematic of the dual standard baseband processor

filter is used as a feedback to achieve clock synchronization. Synchronisation block also computes the beginning of the slot/frame and relative delays between strongest multipaths. Various outputs of the synchronization block i.e. data at chip rate, chip clock, slot/frame beginning and multipath delay are used in the subsequent blocks. Pilot symbols transmitted from the BS are used to estimate the channel response. Descrambling, despreading, fading cancellation operations are performed in each finger of the rake receiver. Finally rake receiver combines the output of each finger and truncates it to appropriate word size togive I and Q outputs. These outputs may be used either as received symbols or for further processing, such as de-interleaving or soft Viterbi decoding.

There is a separatetiming and control unit in the processor. This unit reads control inputs and parameters (e.g. initial state vectors for code generation etc.) from the higher layer(s) and stores them in a bank of flip-flops. Here we can not use a RAM in place of flip-flops, because many parameters may be read at the same instant (e.g. beginning of slot) by various other blocks of the system.

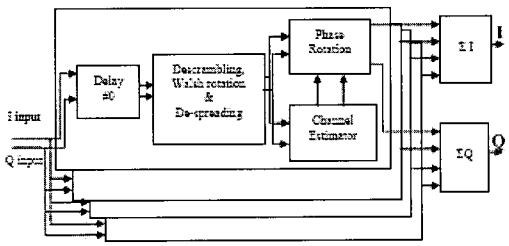
4. IMPLEMENTATION OF VARIOUS UNITS OF THE PROCESSOR

In this section we will describe each unit of the processor (shown in figure 2) in

separate sub-sections. In each sub-section, we will make out the commonalities and the differences between the two standards and briefly describe the hardware implementation of that unit.

4.1 Rake Receiver and Channel Estimation

We have gone for a four finger Rake diversity receiver, with each finger processing the replica of the received signal delayed by multipath delays (estimated by the synchronization block) with respect to the adjacent fingers. Figure 3 shows the block schematic of the rake receiver.



[Fig 3] Block schematic of the Rake receiver

Digitized input samples are received in I and Q branches in complex low-pass number format. The four fingers of the Rake receiver introduce delays of respectively t0, t1, t2, t3 in the input samples. The code generators in UMTS system consist of Gold code generators for complex valued descrambling code generation, and Orthogonal Variable Spreading Factor (OVSF)code generators for de-spreading code generators [7]. Whereas in cdma2000, I/Q PN sequences are used for de-scrambling and a combination of Walsh code & QOFsign bit is used for de-spreading operation [8]. In addition to the above mentioned differences an extra operation is performed in between de-scrambling and de-spreading operations in cdma2000. This operation is named as walsh-rotation.

$$SymbolRate = \frac{\text{Chip Rate}}{SpreadingFactor} \quad (1)$$

Where, the spreading factor may be 2^{s+2} (s=0 to 7 for UMTS, s=0 to 6 for cdma2000) [7,8]

It is to be noted that, chip rates are different in two standards. For downlink, chip rate is equal to 3.84 Mcps in UMTS and its value is 1.2288 Mcps in cdma2000. In each finger, the channel estimator uses the pilot symbols to estimate the channel characteristics. In UMTS, either dedicated pilots, which are time multiplexed with user data slot, or common pilots, which are transmitted separately on PCPICH are used for this purpose [5]. In cdma2000, Forward Pilot Channel is used for channel estimation [8]. To estimate the channel characteristics, apart from the received pilot values of the current slot, the pilots of previous slots may also be used. In a

slowly varying channel it is useful to use the channel estimates of a few previous slots with some forgetting factor. Let, for any slot k, the channel estimate calculated from its pilots is ch_k and the interpolated channel estimate for the slot is est_k. We perform the operation,

$$est_k = (1 - 2^{-W})\, ch_k + 2^{-W}\, est_{k-1} \quad (2)$$

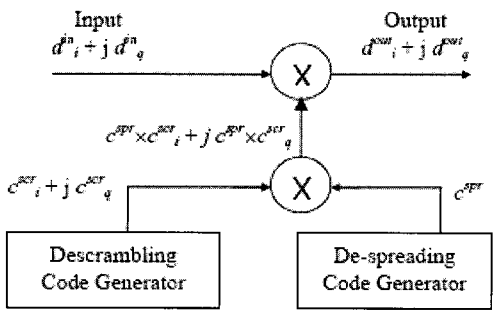
where W is an externally controlled forgetting-factor which is signaled by higher layers.

The de-spread data in each finger is multiplied by the complex conjugate of the channel estimate corresponding to that finger. This has two effects. Firstly, the phase introduced to the signal is neutralized so that the outputs of all the fingers can be summed together. Secondly, stronger a multipath more is its weight in the final output, as a stronger multipath will cause higher amplitude of the channel estimate in the corresponding finger. In fact this essentially takes care of maximal ratio combining [9]. Finally the outputs of all the four fingers are summed together to give I and Q outputs. These outputs may be used either as received symbols or for further processing, such as multi-user detection or soft Viterbi decoding [10].

4.1.1 Implementation of the Rake Receiver

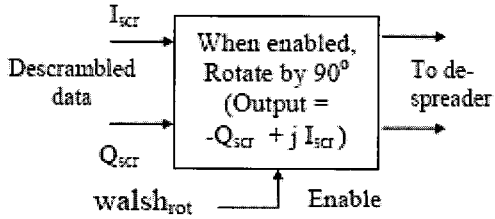
As all the four fingers of the Rake are identical, the description of only one of them suffices. The structure of a finger can be summarized as a sequence of a delay element, multiplication by descrambling and de-spreading codes, integration over a symbol duration, and finally, multiplication by the complex conjugate of the channel estimate. The delays are introduced using flip-flops operating on the clock whose frequency is 2 x $freq_{chip\_clock}$.

Descrambling and de-spreading code multiplication



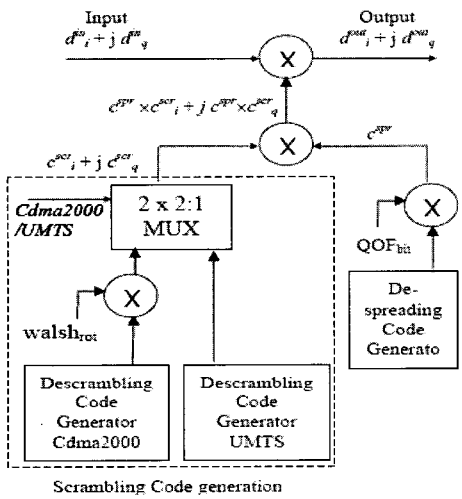
[Fig 4] Multiplication with UMTS descrambling and de-spreading codes

As mentioned before, in cdma2000 there is an extra operation which is called Walsh rotation. Figure 5 describes this operation

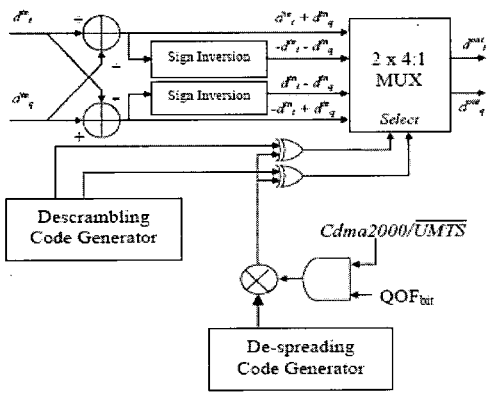


[Fig] 5] Walsh rotation of the descrambled data

Now, instead of applying the $Walsh_{rot}$ bit on the descrambled data we can club this bit with descrambling code. Hence, to make the system compatible with both the standards we can modify the scheme shown in figure 4 in the following way (figure 6). In figure 6 and 7 QOF_{bit} is always '0' for UMTS.



[Fig 6 Descrambling and de-spreading operations



[Fig 7] Hardware for multiplication with descrambling and de-spreading codes

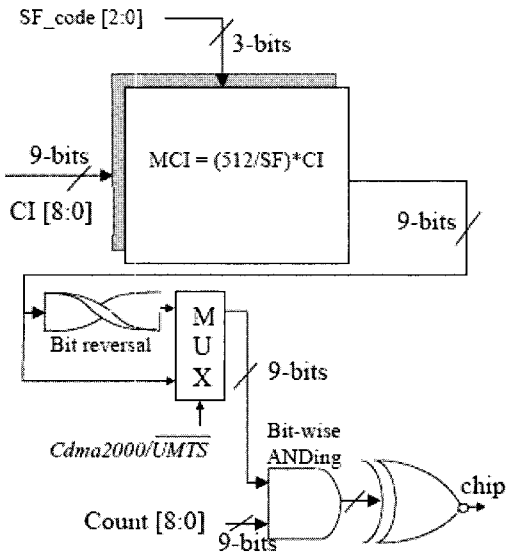
Descrambling codes are complex valued codes of the format $\pm 1 \pm j$, represented by two bits where bit '0' implies +1 and bit '1' implies -1. The de-spreading codes are real valued codes, having values $\pm$ 1. For better area and speed optimization, firstly these codes are multiplied together and the result, in turn, is multiplied to the input data. The first multiplication consists of two one-bit by one-bit multiplications, each of which can be performed by one XOR gate. For the second multiplication, we note that the output is of the form $(\pm d^{in}_i \pm d^{in}_q) + j (\pm d^{in}_i \pm d^{in}_q)$, where $d^{in}_i + j\ d^{in}_q$ is the input sample Figure 7 shows the hardware requirement for this scheme.

In UMTS the OVSF Codes are used for spreading. But cdma2000 uses Walsh code for this purpose. Both, the OVSF and Walsh codes can be uniquely defined by the Spreading Factor (SF) and the Code Index (CI). The OVSF code generator itself can be used to generate the Walsh code as well, by using the following simple property:

$$OVSF\_CODE_{(SF,CI)} = Walsh\_CODE_{(SF,\ CI\_bit\_rev)} \quad (3)$$

where, $CI\_bit\_rev = (CI)_{\text{bit reversed}}$

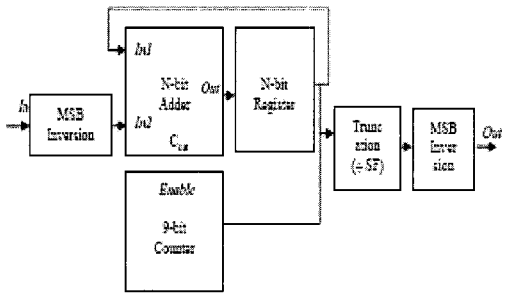
We have designed and implemented a novel scheme for OVSF/Walsh code generation (figure 8).



[Fig 8] Hardware for generating the de-spreading code

Integration over symbol period

The de-spread chips have to be integrated over the symbol period, which depends on the spreading factor. We have designed an accumulator architecture, which is optimized for the purpose. Let the input, in 2's complement format, be N-bit wide. Then the width of the accumulator has to be N+9, as the maximum spreading factor is 512. Firstly, we change the format of the input chips to an unsigned format by adding 2^{N-1} to each of them. This removes the need for sign extension. The change of the format can be done just by inverting the MSB's of the input chips. Similarly the output is converted back to 2's complement format just by inverting the MSB of the truncated result. Another optimization is achieved by replacing the N+9 bit adder by an N-bit adder and a 9-bit counter. This improves both the area and speed of the design as 9 full-adders are replaced by 9 half-adders. Figure 9 shows the structure of such an accumulator.



[Fig 9] Integrator over symbol period

Channel estimation

The pilot chips, for each finger of the Rake, have to be multiplied with the descrambling codes, de-spreading codes and the complex conjugate of the transmitted pilot symbols before being integrated over the pilot burst to get the channel characteristics for the multipaths corresponding to that Rake finger. Both descrambling codes and pilot symbols are complex numbers of the format $\pm 1 \pm j$. Hence, each of them has amplitude of $\sqrt{2}$ and phase of $\pm 3\pi/4$ or $\pm \pi/4$. The de-spreading codes can have values ± 1. Hence the product of all three of them will be a complex number having amplitude of 2 and phase of 0, π or $\pm \pi/2$. Multiplication with 2, or with any constant

for that matter, is redundant for the end result. Hence, we only need to multiply ± 1 or ± j to the input chips, depending on the descrambling code, de-spreading code and pilot signature. This multiplication, as can be easily seen, can be performed with just two sign-invertors and four 4:1 multiplexers. The result of the multiplication is accumulated over the pilot burst using an accumulator similar to the one shown in Figure 9. The previous channel estimate is combined, with a variable weight, with the estimate obtained from the pilot of the current slot to get a better estimate of the channel. Figure 10 shows the operations needed for this functionality. (See equation 2).

Note that all the multiplications in the diagram can be done by shifting the inputs. This technique is especially useful in a slow varying channel.

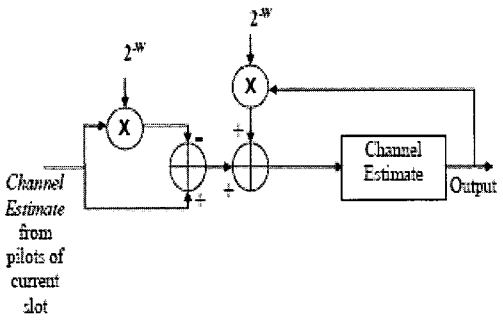


Figure 10: Weighted averaging of channel estimate of multiple slots

Phase rotation

The phases of the de-spread symbols of each of the fingers have to be neutralized, using the channel estimate of that finger, before the outputs of the fingers can be summed together.

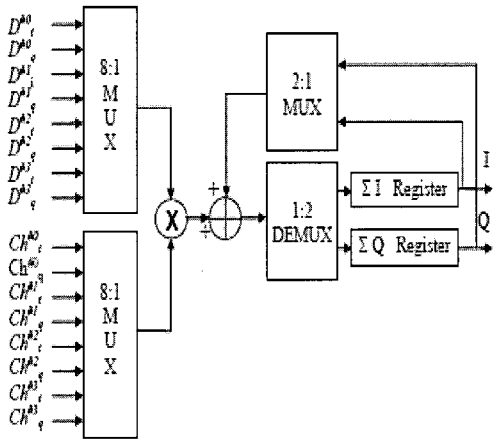


Figure 11: Shared hardware for phase neutralization and multipath summation

The whole operation for a four finger Rake requires four complex multiplications per symbol, each of which, in turn, requires four real multiplications. The input throughput at this stage is slow, being at de-spread symbol rate. This fact lets one share a single fast multiplier-accumulator for the phase rotation and summations of the de-spread symbols of all the fingers.

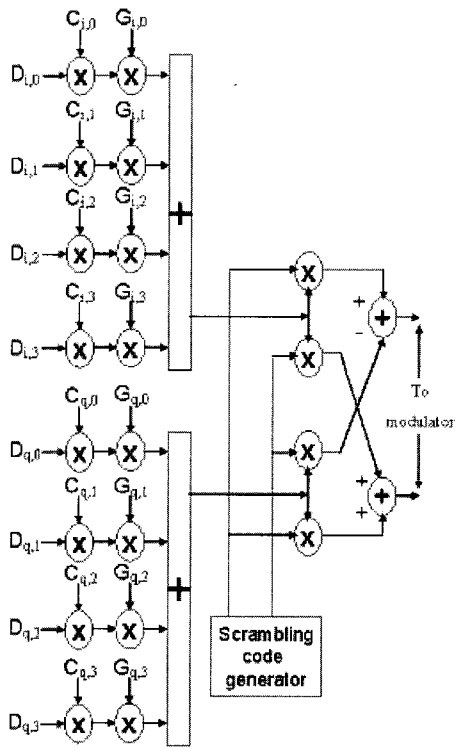
Word size

The word size at the different points in the design is a very crucial issue, which

has effects on area, power, hardware complexity, speed and accuracy of the design. Following is a description of the word sizes used in the different parts of the design. The widths of I and Q part of the data at each point of the design are equal. The input samples are assumed to be 8-bit wide. The output after multiplication with descrambling and de-spreading codes is 9-bit wide. The output after the integration of the chips over the symbol period is truncated to 11-bits. At this stage the truncation has to be performed on both MSB and LSB depending on the spreading factor. The channel estimate has been kept 10-bit wide. The final truncation is done after combining the outputs of different fingers to get 8-bit wide soft outputs.

4.2 Uplink Channels

The operations carried out in the baseband processor for the uplink channels have already been summarized in section 2. Here, these operations are shown in figure 12. This uplink unit is capable of processing 8 uplink logical channels simultaneously. $D_{i,k}$ (k= 0,1,2,3) is the input bit stream in the kth branch of the "in-phase" arm. Similarly, $C_{i,k}$ (k= 0,1,2,3) and $G_{i,k}$ (k= 0,1,2,3) are the values of the Channelization code and the relative channel gain factor in the k^{th} branch of the "in-phase" arm respectively. Similar nomenclature is used for the "quadrature" arm components as well. Typically, in both the standards some of these logical channels will be data channels and others will be control channels [5,7,8]. As mentioned before, cdma2000 uses walsh code and UMTS uses OVSF code for Channelization. The hardware scheme for generating OVSF/walsh code of given SF and CI is shown in figure 8. Relative channel gain block takes single bit spreaded data (± 1) and multiplies it with 4 bit unsigned number to produce weighted output (5 bit signed number) [7]. The hardware scheme for the same is shown in figure 13.



[Fig 12] Spreading, channel gain and scrambling mechanism for uplink channels

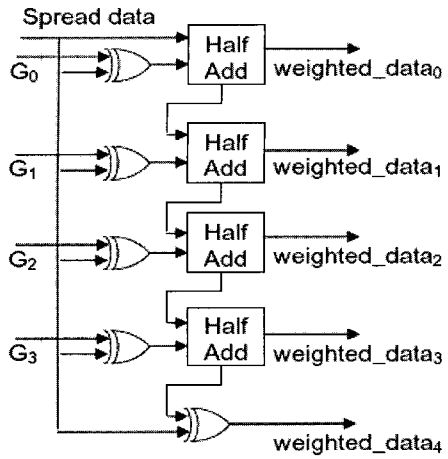
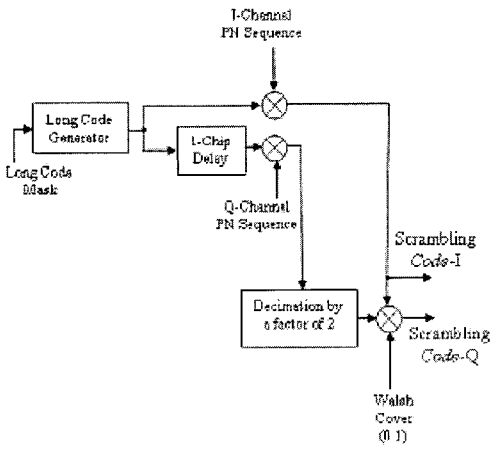


Figure 13: Weight Multiplier (Hardware implementation for Relative Channel gain)

For scrambling, the hardware implementation of the complex multiplier is already shown in figure 7. Scrambling code generation mechanism differs in the two standards. In cdma2000, scrambling code consists of a long code and I/Q channel PN sequences as shown in figure 14 [8].



[Fig 14] Generation of scrambling code for cdma2000 using long code and I/Q PN sequences

In UMTS, scrambling code can either be a long code or a short code depending upon the control inputfrom the higher layer. However at a given time, the mobile equipment will work in either UMTS system or cdma2000-1x system or cdma2000-3x system. Therefore we can reduce the hardware required for scrambling code generation for both standards by using the same set of shift registers for generating either (i) long scrambling code for UMTS or(ii) I and Q channel PN sequence for cdma2000-1x or(iii) I and Q PN sequence for cdma2000-3x. Similarly, this design approach can be replicated for de-scrambling code generation in the downlink.

5. CONCLUSIONS

In this paper, the physical layer aspects of both UMTS and cdma2000 are studied in detail and the commonalities and differences are brought out with the objective of proposing an ASIC implementation approach. Following are the major commonalities and differences between the two standards:

Commonalities:

- The same code generator (with a little extra hardware) can be used for OVSF and Walsh code generation, which are used for channelisation in UMTS and cdma2000 standards respectively.

  Exactly the same hardware is good

enough for relative channel gain weighting in both the standards.

- Given the appropriate scrambling/ de-scrambling code as an input, the same hardware can be used for (de)scrambling operation for both the standards.
- For both the standards, a common hardware block can be designed to estimate the channel response.

Differences:

- Scrambling code generators are different in the two standards.
- In UMTS, chip rate is always fixed at 3.84 Mcps for both uplink and downlink transmission and there is only one carrier that is modulated by the scrambled data. Whereas, in cdma2000 chip rate is different for cdma2000-1x and cdma2000-3x in uplink. In downlink, chip rate is same for both cdma2000-1x and cdma2000-3x, but cdam2000-3x operates in multicarrier mode (number of carriers=3).
- UMTS supports asynchronous base stations whereas cdma2000 relies on synchronized base stations [11]. Therefore, cdma2000 mobile station can use different phases of the same scrambling code to distinguish between adjacent base stations. However, in UMTS adjacent base stations can only be identified by distinct scrambling codes. Consequently, cell search, which involves the process of achieving code, time and frequency synchronization of the mobile station with the base station, takes longer for an asynchronous CDMA system in comparison to a synchronous CDMA system.

Also the hardware development of a Rake receiver based CDMA baseband processor in the form of an ASIC for 3G wireless communication systems is presented here. The hardware is optimized to the extent possible from the chip area and power consumption considerations while satisfying the requirements of a 3G wireless system. This design provides a path towards developing a full baseband chip for the 3G wireless communication systems.

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Biography

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