Design Improvement and Measurement of a Rapid Single Flux Quantum Confluence Buffer

Seung Hun Baek*[a], Jin Young Kim[a], Sehoon Kim[a], Joonhee Kang[a], Ku-Rak Jung[b], Jong-Hyeok Park[b] and Teak-Shang Hahn[b]

a Department of Physics, University of Incheon, Incheon 402-749
b Korea Photonics Technology Institute, Gwangju 500-210

zabahun@incheon.ac.kr

Abstract-- **Rapid Single flux quantum (RSFQ) confluence buffer is widely used in complex superconductive digital circuits. In this work, we have improved the currently used confluence buffer and obtained a more soundly designed confluence buffer. In simulations, improvements in the bias margins of 11% and the global margins of 10%, compared to the previously used confluence buffer, were achieved. Global margins are very important in estimating a process error range allowed in fabrications. We used two circuit simulation tools, WRspice and Julia, to design and optimize the confluence buffer. We used Xic to obtain a mask layout. We fabricated the improved circuits by using Nb technology. The test results at low frequency showed that the improved confluence buffer operated correctly and had a very wide main bias margin of +/-43% enhanced from +/-26% of the previously used confluence buffer.**

1. INTRODUCTION

Recent development in semiconductor technology has been following the Moore's law, but it is expected that the physical and power limitations may prohibit further progress of the technology.

In the mean time, a rapid single flux quantum (RSFQ) device [1] has been suggested to overcome the limitations of semiconductor devices. Large RSFQ circuits can operate up to a few tens of gigahertz with ultra-low power consumption [2]. Successful developments of various RSFQ logic circuits [3], including a digital-to-analog converter [4], an analog-to-digital converter [5], logic gates [6], a switching device [7], a router, and a voltage standard [8], have been reported. In RSFQ logic circuits, a magnetic-flux quantum stored in an inductor and controlled by a Josephson junction is used to build a fast digital logic circuit [9]. The development of new RSFQ logic circuits has been significant in recent years. A T flip-flop (TFF) circuit was built with this technology and was demonstrated at 770 GHz [10].

Even though most RSFQ circuit elements are relatively stable and have reasonably wide margins, insertion of these elements in the large-scale circuits can be difficult because RSFQ circuits are current biased. Distribution of the currents can be somewhat irregular, and the fabricated Josephson junction sizes can be somewhat non-uniform. Therefore, the actual circuit margins can be smaller than the designed values when fabricated. And designing the circuit elements with large margins is very important in building practical RSFQ digital circuits.

In this work, we have improved the RSFQ confluence buffer and optimized it to obtain a more sound circuit. Confluence buffer is one of the widely used circuits in RSFQ digital circuits. We carefully analyzed the currently used RSFQ confluence buffer by using WRspice[11], a computer simulation program. In simulations, the circuit schematics were drawn by using Xic[12], a circuit design program. Fig. 1(a) shows the circuit schematic diagram of the most widely used confluence buffer, and Fig. 1(b) shows the microphotograph of its fabrication.

We also performed margin analyses to evaluate the circuit performance. Based on the simulation results, we modified the circuit and optimized it by using a computer program called Julia. After confirming the enhanced performance of the new confluence buffer, we used Xic [12] to obtain the mask layout of the circuit. For the circuit layout we used Lmeter to extract the inductance values of the superconductor strip lines in the layout.

Accurate extraction of the inductance values is critical in obtaining the fabricated circuits performing as close as to the designed circuit. The circuit was fabricated by using Nb technology and tested at liquid helium temperature.
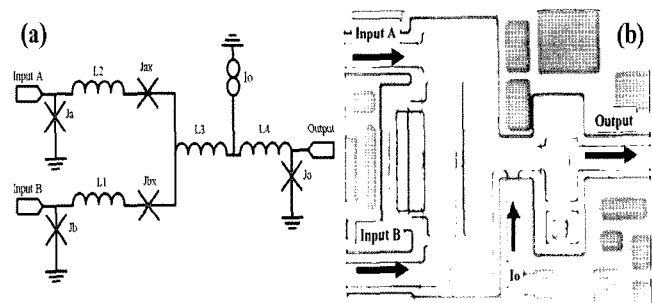

Fig. 1.(a) Schematic circuit diagram of the confluence buffer. This circuit has been used in various RSFQ circuits. (b) The microphotograph of the commonly used confluence buffer. The circuit size was $103\mu m \times 71\mu m$.

2. CIRCUIT DESIGN

The confluence buffer permits channeling of the SFQ pulses passing from two inputs to one output. The circuit schematic diagram that shows this circuit operation shown in Fig. 1(a). Two inputs are noted as "Input A" and "Input B." The output is noted as "Output." The main input junction Ja or Jb switches when there is an SFQ pulse input to the corresponding input node "Input A" or "Input B." The auxiliary junction Jax and Jbx protect the inputs from the reverse flow of the SFQ pulses and isolate the inputs from each other. When an SFQ pulse enters into the confluence buffer, it does not propagate to the other input port because of these auxiliary junctions. An SFQ pulse from "Input A" or "Input B" propagate through Ja (& Jbx) or Jb (& Jax), and switches Jo resulting to the output of an SFQ pulse.

To make sure that the drawn circuit operates correctly according to the circuit operation principle, we did computer simulations by using a Josephson circuit simulation program WRspice. The results of the computer simulation for the circuit shown in Fig. 1 were as shown in Fig. 2. Fig. 2 shows the results of the transient analyses done for the confluence buffer. In simulations, we arbitrarily chose 8ns for the data period. We used "10101" for the "Input A" data pattern and "00110" for the "Input B" data pattern. In simulations, we obtained the "Output" data pattern of "10111" for these input patterns. As can be seen in the Fig. 2, the confluence buffer was performing the asynchronous OR function. When either of the two inputs was "1" the output was "1." This shows that the confluence buffer operated correctly.

As can be seen in Fig. 2, WRspice is very powerful in confirming the circuit operation. However, WRspice does not have circuit optimization tool. To optimize the design of the confluence buffer, we used a computer simulation program Julia. Julia has the optimization function that searches the best values of the device parameters and bias values automatically.

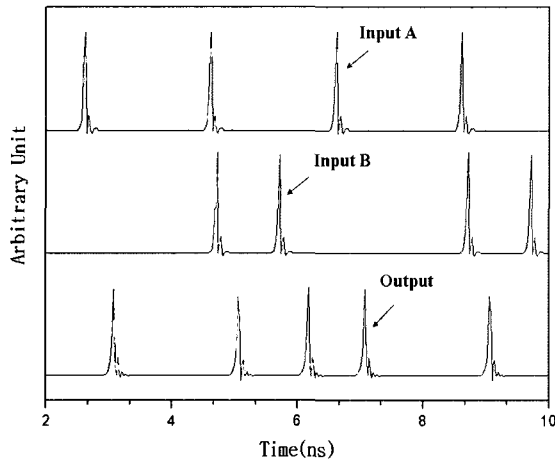Circuit margins were obtained by using Julia. Margin

analysis in Julia used "pass/fail" method. Julia checked the results of the simulation for the circuit parameters in test, and noted "pass" if the circuit operated correctly as shown in Fig. 2. If the results of the simulation were incorrect the Julia noted as "fail". In this way, we obtained the range of the circuit parameter values that enable as "pass" and found the circuit margins. Table I shows the circuit margins of the newly optimized confluence buffer. Most of the new circuit parameters had very wide margins, and the minimum circuit margin was from Io with ±33%. For the old confluence buffer as shown in Fig. 1(b), the margin calculations showed that the minimum circuit margin was also from Io with ±26%.

Julia also calculates the global margins. Fig. 3 shows the calculated global margins for the old confluence buffer and the new confluence buffer. Global margins are more important than the individual margins because fabrication errors and common bias values raise or lower the circuit parameters in groups. Global margins can be used in estimating a process error range allowed in fabrications. We calculated the global margins of the optimized confluence buffer. As can be seen in Fig. 3, it is apparent that the optimized confluence buffer had more evenly distributed bias and junction global margins, raising the lowest margins quite significantly. The graph showed that we improved bias global margin by 10% more than the existent confluence buffer.

With the optimized circuit parameters, we attempted to make the mask layout to test the new confluence buffer. We used Xic to layout the circuit and Lmeter to extract the inductance values of the superconductor strip lines. Calculations of the inductance values for the circuit components in the layout showed that the circuit layout was very close to the designed circuit.

The new confluence buffer was fabricated in Hypres fabrication facility by using a ten-level Nb process with a junction critical current density of 1 kA/cm^2 [13]. Fig. 4 shows the microphotograph of the fabricated new confluence buffer. The new confluence buffer was more compact. We noted two inputs, one output, and one bias line on the above picture. We also used a few ground holes around the circuit to minimize the flux trapping problems.

Fig. 2. Correct operation of the confluence buffer was confirmed in simulations. We used WRspice as the circuit simulation program.

TABLE I
THE OPTIMIZED CONFLUENCE BUFFER MARGINS.

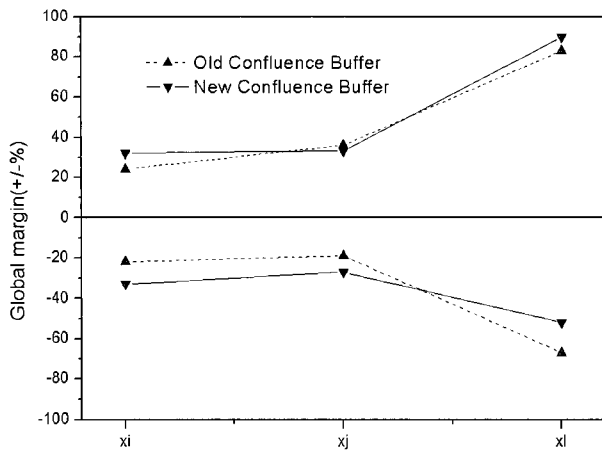| Device Name	Center Value	(-)margin (%)	(+)margin (%)
Ja	0.22mA	>90	>90
Jax	0.22mA	73	61
Jb	0.22mA	>90	>90
Jbx	0.22mA	73	61
Jo	0.24mA	>90	>90
L1	0.63pH	>90	>90
L2	0.63pH	>90	>90
L3	1pH	>90	>90
L4	3.17pH	>90	>90
Io	0.46mA	33	37

Fig. 3. Comparison of the global margins for the old confluence buffer and the new confluence buffer. Xi is the global parameter for bias, xj is for junction, and xl is for inductance.
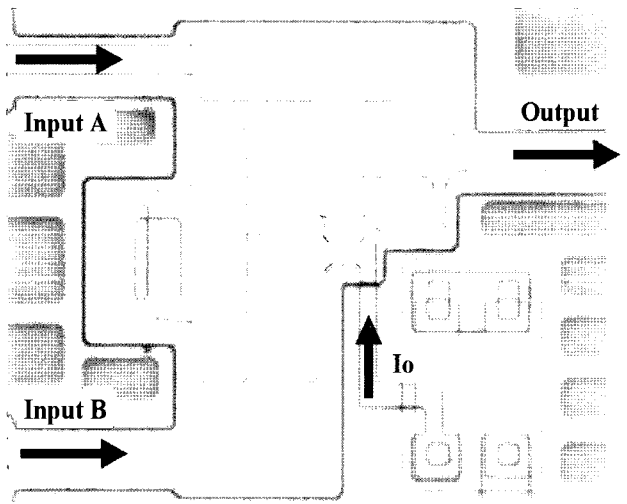

Fig. 4. Microphotograph of the fabricated confluence buffer. 5 Josephson junctions are shown in the picture. Two inputs, one output, and one bias line are noted on the picture. The confluence buffer size is $89\mu m \times 64\mu m$.

3.   CIRCUIT TESTS

To test the fabricated confluence buffer at 4.2 K, the fabricated chip was immersed into liquid He. A specially designed cryo-probe was used to transmit the data between the cooled chip and the room temperature instruments. This probe had 40 parallel contact pads, 26.7 GHz bandwidth, and auto alignment of 5 mm × 5 mm chip. Multi-channel stable current sources were used to bias the circuits.

We used a computerized test setup to test the RSFQ digital circuits more effectively. Finding optimum DC bias current values was essential to operate the RSFQ circuits.

By using the computerized test setup, we could find the optimum bias current values with a minimum effort. In this work, we constructed an automatic test setup with a PXI

measurement system. Fig. 5 shows the simplified block diagram of our measurement system. Our PXI system was consisted of a PXI main frame, a PXI control card, a SCXI signal conditioning card, analog-to-digital (A/D) modules, digital-to-analog (D/A) modules. National Instruments PXI-1006 PXI main frame had an 18 slot chassis and could be equipped with 17 modules. National Instruments PXI-PCI8335 PXI control card was essential to control the PXI system with a computer and had a communication speed of 84 Mbytes/s - 132 Mbytes/s. Due to the very small output voltages generated in SFQ circuits, we employed an SCXI instrument for low speed tests. An SCXI with 8 channels provided isolation between the test samples and the PXI modules, a 1000x gain, and a 10kHz low pass filtering.

To test the performance of the confluence buffer, we used an A/D module and a D/A module. We used National Instruments PXI-6052E 16-bit A/D module to measure the output signal from the confluence buffer. We could use this module to measure the small output voltage signal with the resolution of $25\mu V$. The sampling frequency of this module was 333 kS/s. Our PXI system had several National Instruments PXI-6713E D/A modules. All the signals were measured with an A/D module. The measured signals include an output signal from the confluence buffer, two input monitors that monitor the correct SFQ pulse generations from the input DC/SFQ pulse generators, and the two input signals. We used Labview software as a programming tool to control the PXI instruments and for data acquisitions.

A DC/SFQ circuit was used to generate a stream of SFQ pulses, and an SFQ/DC circuit to monitor them. Since we used a T flip-flop (TFF)-type SFQ/DC converter for the data monitoring, any SFQ pulse output toggled the output between two voltage levels. By using the other branch of SFQ/DC circuit (180° out of phase), we made a direct connection of an SFQ/DC circuit to the DC/SFQ circuit to monitor if the correct SFQ pulses were generated from the DC/SFQ circuit.
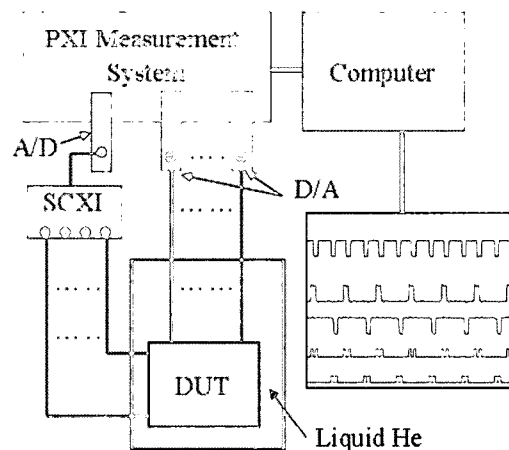

Fig. 5. Simplified block diagram of the PXI measurement system that was used to test the RSFQ confluence buffer.

Fig. 6 shows the test results of the correctly functioning confluence buffer. We only did a functionality test at low speed, and the test speed was 250Hz. Our RSFQ circuits can easily operate at tens of a GHz. However, the detection speed of RSFQ pulses is limited by the scope bandwidth because of the very small amplitude (about 0.1mV). Since our goal of this work is in the functionality test of the new confluence buffer we used a PXI measurement system that can read small signals at 330 kHz. In simulations, we confirmed the correct operation of the circuit at tens of a GHz. The bottom two traces noted as "Input A" and "Input B" were the input signals and the top trace noted as "Output" was the output signal from the TFF-type SFQ/DC converter on the confluence buffer output. The middle two traces noted as "Input A monitor" and "Input B monitor" were from the SFQ/DC converters directly connected to the other branches of the DC/SFQ input circuits. For each rising edge of "Input A" and each falling edge of "Input B", an SFQ pulse was generated and transferred to the confluence buffer. The top trace toggled for each of these input pulses, indicating that the circuit operated correctly as designed. Synchronization between the output and the input signal shows that the input pulses triggered the output pulses. In the middle traces, "Input A monitor" toggled for each falling edge of the "Input A" signal and "Input B monitor" toggled for each rising edge of the "Input B" signal, showing that the correct SFQ pulse generations were made.

By varying the output, input, and the confluence buffer biases, we obtained the circuit margins of the new confluence buffer. Table II shows the measurement results. The confluence buffer main bias (Io) had a very wide margin of +/-43.2%, showing that our improved confluence buffer can be comfortably applied to the practical RSFQ devices. In our measurements with the old confluence buffer we observed +/-22.6% for the main bias margins.
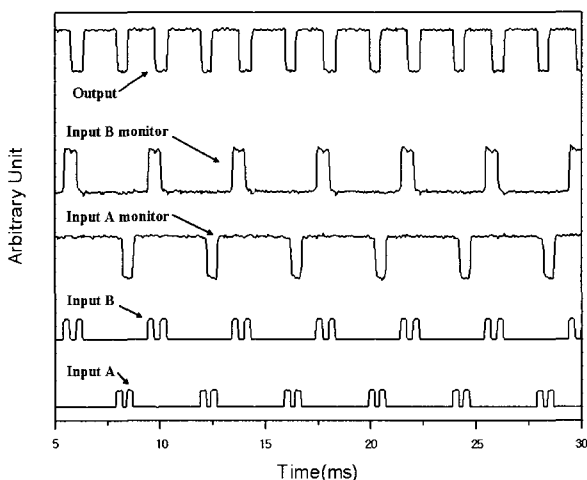

Fig. 6. Measurement results at 250Hz. For each input, the corresponding input monitor toggled between the two voltage levels. Output shows that the confluence buffer operated as an asynchronous OR because there was no clocking.

TABLE II
THE OPTIMIZED CONFLUENCE BUFFER MARGINS.

Bias Name	Minimum(mA)	Maximum(mA)	margin (%)
Input	2.79	5.9	35.8
Io	0.27	0.68	43.2

4. CONCLUSION

We have developed an improved RSFQ confluence buffer. We designed, simulated, and optimized the circuit. It was fabricated using Nb process with Josephson junction critical current density of 1 kA/cm^2 in HYPRES. Operation of the fabricated chip was made with a PXI automated system. The main bias margin of the optimized confluence buffer was more than +/-33 % in simulations, enhanced from +/-26 % of the old confluence buffer. The improved confluence buffer had more evenly distributed bias global margins and junction global margins, raising the critical margins significantly. Therefore, developing more complex RSFQ circuits with the improved confluence buffer became more realistic. The test of the fabricated chip at the liquid helium temperature showed that the improved confluence buffer operated correctly and showed main bias margin of +/-43 %. The size of the confluence buffer cell was about 90μm × 60μm. Not only bias margin but also layout size was improved by the optimization of the circuit parameter values. The new confluence buffer had wider bias margins and more compact layout size.

REFERENCES

[1] J. Y. Kim, S. H. Baek, and J. H. Kang, "Construction of a single magnetic flux quantum switch and its usage in an arithmetic logic unit," J. Korean Phys. Soc, vol. 43, pp. 1129-1134, 2003.

[2] K. Likharev and V. Semenov, "RSFQ logic / memory family: a new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," IEEE Trans. Appl. Supercond, vol. 1, pp. 3-28, 1991.

[3] Q. P. Herr, N. Vukovic, C. A. Mancini, K. Gaj, Q. Ke, V. Adler, E. G. Friedman, A. Krasniewski, M. F. Bocko, and M. J. Feldman, "Design and low speed testing of a four-bit RSFQ multiplier-accumulator," IEEE Trans. Appl. Supercond, vol. 7, pp. 3168-3171, 1997.

[4] R. D. Sandell, B. J. Dalrymple, and A. D. Smith, "An SFQ digital to analog converter," IEEE Trans. Appl. Supercond, vol. 7, pp. 2468-2471, 1997.

[5] V. K. Semenov, "Digital to analog conversion based on processing of the SFQ pulses," IEEE Trans. Appl. Supercond, vol. 3, pp. 2637-2640, 1993.

[6] K. R. Jung and J. H. Kang, "Application of fast-moving magnetic-flux-quanta in constructing an AND gate and an OR gate," J. Korean Phys. Soc, vol. 45, pp. 479-484, 2004.

[7]   N. B. Dubash, P. F. Yuh and V. V. Borzenets, "SFQ data communication switch," IEEE Trans. Appl. Supercond, vol. 7, pp. 2681-2684", 1997.

[8]   C. J. Burroughs, S. P. Benz, T. E. Harvey, and C. A. Hamilton, "1 volt DC programmable Josephson voltage standard," IEEE Trans. Appl. Supercond, vol . 9, pp. 4145-4149, 1999.

[9]   C. A. Hamilton and Frances L. Lloyd, "100 GHz binary conter based on DC SQUID," IEEE Electron Dev. Lett., Vol. EDL-3, pp. 335-338, 1982.

[10] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, "Rapid single flux quantum T-flip flop operating up to 770 GHz," IEEE Trans. Appl. Supercond, vol . 9, pp. 3212-3215 , 1999.

[11] http://www.wrcad.com/wrspice.html

[12] http://www.wrcad.com/xic.html

[13] HYPRES design rules can be found at Hypres web site at www.hypres.com.