The Methodology of Systematic Global Calibration for Process Simulator

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This paper proposes a novel methodology of systematic global calibration and validates its accuracy and efficiency with application to memory and logic devices. With 175 SIMS profiles which cover the range of conditions of implant and diffusion processes in the fabrication lines, the dominant diffusion phenomenon in each process temperature region has been determined. Using the dual-pearson implant model and fully-coupled diffusion model, the calibration was performed systematically. We applied the globally calibrated process simulator parameters to memory and logic devices to predict the optimum process conditions for target device characteristics.

Keywords : Process simulation, Calibration, Implantation, Diffusion, Silicidation

1. INTRODUCTION

Accurate and reliable TCAD (technology computer-aided-design) tools play a major role in development and manufacturing of semiconductor[1]. The progress of NSI (nano-scale integrated circuit) technologies to yield higher density DRAM and ultra-high performance and low power chips has brought with it the need to use in a wide variety of ways of TCAD tools[2,3]. As a result of the progress in areas such as process and device physics, the utilization of experimental techniques and the power of computing, the TCAD has reached a level that was considered virtual fab which used the simulation environment.

In silicon microelectronics, the understanding of impurity diffusion is one of the oldest research topics awaiting a satisfactory solution. Over the past few years, considerable progress was made towards the goal of being able to accurately predict doping profiles. In today's advanced and extremely scaled MOS technologies, the formation of shallow junctions is of particular interest. While extremely challenging from a modeling viewpoint, the approach of calibrating the process models to advanced experiments such as seconddary ion mass spectroscopy (SIMS) or nano-spreading resistance profiles seems to be quite successful.

As NSI technology advances, the accuracy and predictive capabilities of process simulation have become more and more important in device design and development[4,5]. But there are still many limitations in the process simulation which is not well modeled. Furthermore, it is necessary to use the process simulation parameters which are globally applicable to all kinds of devices in fabrication. This paper proposes a novel methodology of systematic global calibration and validates its accuracy and efficiency with application to memory and logic devices.

2. METHODOLOGY

The process simulator calibration environment based on the TCAD framework[6], as shown in Fig. 1, has been constructed to systematically extract ion implantation and diffusion model parameters. The TCAD framework worked as manager of the database, the optimizer and runner to control the simulation status on distributed systems. The analytical modeling of ion implantation have shown good promise in real applications. Compared to implantation, accurate and physics-based simulation of thermal annealing steps is considerably more challenging. Impurity diffusion in silicon occurs via a pair diffusion mechanism which means that the impurity atoms join one or more point defect as an interstitial. These point defects are generated during previous process steps such as an ion implantation. Modern technologies require very shallow junctions below 0.1 μm, which leads to rather short annealing times in the range of a few seconds. Therefore, the diffusion kinetics can be characterized as extremely nonlinear and non-stationary, putting stringent conditions on the numerical methods employed for equation

solution. While many aspects of the impurity-defect clustering and de-clustering processes are still unknown. This is the reason why the calibration methodology should be developed.

We analyze the implantation, gate oxidation and annealing process conditions of each process technology generation to make the critical point of experiment window. Based on this experiment window, we process the short-loop experiment such as in the right box of Fig. 1 The SIMS data are stored as data-base system for efficient handing[7]. From the target SIMS data, we optimize the parameters which are previously determined for each process condition by the sensitivity analysis. Such as the box diagram of center and left in Fig. 1, we sequentially extract the diffusion parameters starting from the intrinsic carrier concentration region with impurity diffusivity to TED (transient enhanced diffusion) parameters. Then the set of the extracted parameters is validated by the device simulation in term of electrical characteristics.

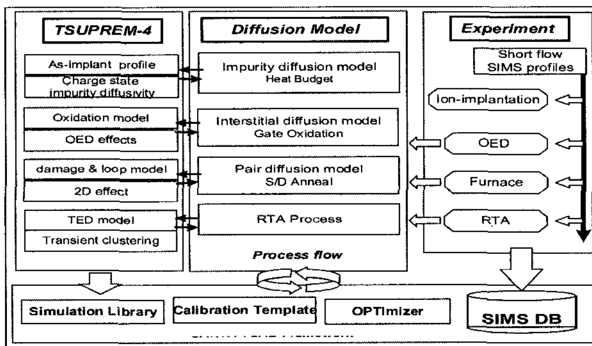


Fig. 1. A calibration environment for process simulator.

3. CALIBRATION

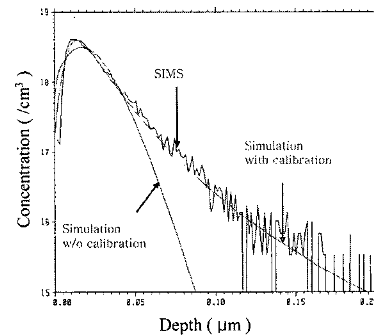
With 175 SIMS profiles which cover the range of conditions of implant and diffusion processes in the fabrication lines, the dominant diffusion phenomenon in each process temperature region as shown in Fig. 2 has been determined.

Fully coupled diffusion model	1000℃ ~ 950℃	900℃	850℃	830℃/ 800℃	RTA
Impurity diffusivity extraction					
Interstitial parameters extraction					
Pair reaction & diffusivity extraction					
Damage / loop clustering extraction					
Segregation extraction					

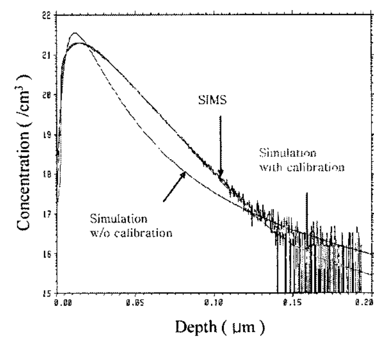
Fig. 2. The global calibration methodology for the fully-coupled diffusion model.

From the fully-coupled diffusion model[8], impurity diffusivities at the high temperature over 950 ℃ and interstitial-related parameters from the OED (oxidation enhanced diffusion) phenomenon at 900 ℃ have been sequentially extracted. Then, the parameters for the impurity-defect pair movement have been extracted because the impurity redistribution and dopant activation are dominant below 850 ℃[9]. In addition to implant and furnace diffusion calibration, the TED (transient enhanced diffusion) parameters in RTA models including the silicidation process have been extracted at the final calibration step. The adjustment of parameters for the dose loss and snow plowing effects has been considered for the whole temperature region.

Figure 3 shows that the simulation results for ion-implantation with calibrated parameters are well matched to the peak and tail regions of as-implanted SIMS profiles for arsenic and phosphorus impurities. Optimization is carried out using the 9-momentum of dual-pearson model. The implant table of commercial process simulator is good for medium dose and energy, but the low energy and high dose range have discrepancy in peak and tail profiles. The low energy implantation has complex scattering mechanism and the high dose implantation has surface amorphization and clustering effect. So, the analytical implantation modeling has limitation to predict these phenomena accurately. It need to simulate with more physically based approach such as the monte-carlo or molecular dynamics method.



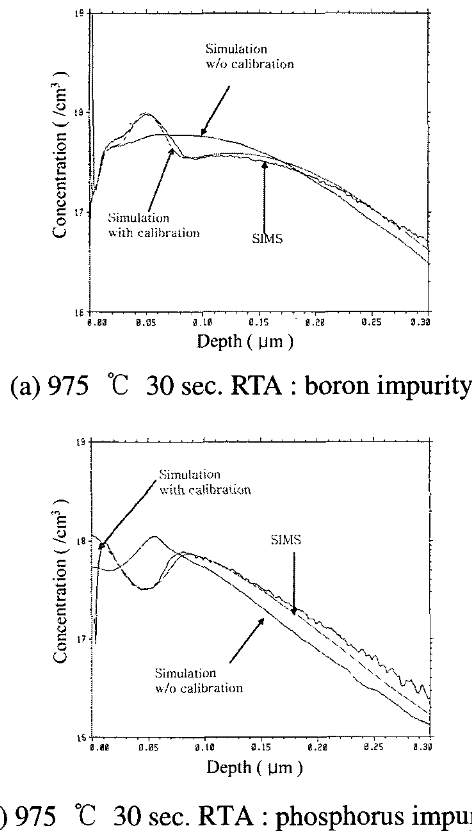
(a) Arsenic impurity



(b) Phosphorus impurity

Fig. 3. The calibration results of the ion-implantation process compared with SIMS data.

Figure 4 also shows the accurate simulation results for boron and phosphorus redistribution caused by the source and drain implantation damage at the RTA temperature and time of 975 ℃/30 sec. To monitor how the TED affects the channel impurity redistribution, the damage generation is made by high dose (5.0×15 cm^{-2}) arsenic implantation which is the condition for the source/drain process. The surface concentration pile-up is the result of the gradient in the interstitial concentration produced by recombination at the silicon/oxide interface. The gradient in the interstitial concentration produces the gradient of dopant/interstitial pairs resulting in the diffusion of these pairs towards the Si/SiO_2 interface[10,11].

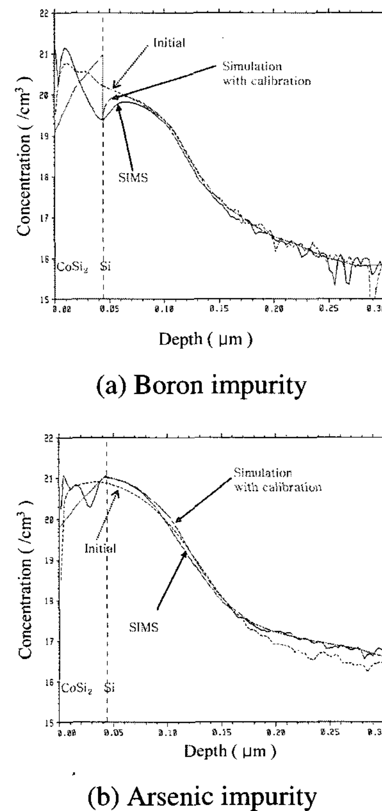


(a) 975 ℃ 30 sec. RTA : boron impurity

(b) 975 ℃ 30 sec. RTA : phosphorus impurity

Fig. 4. Calibration results of RTA process compared with SIMS data.

The simulation for the impurity redistribution at the $CoSi_2$/Si interface is shown in Fig. 5. The $CoSi_2$ appears during Co/Si reaction and this growth is induced by the diffusion of Co atoms through the silicide layer[12]. So, there are no generation of interstitials and no movement of dopant in silicon. But the dose variation at the interface is clearly seen. At the interface, the boron impurity shows strong dose loss and the amount is increased as the temperature and the time increase. But for arsenic, the snow plowing effect is observed at the interface and the amount is the same as the variation of the temperature and the time. In this calibration, we consider this effect as modification of segregation and trapping coefficients[13]. Because the $CoSi_2$ layer is treated as a conductor, the doping profile of the $CoSi_2$ layer has not calibrated.



(a) Boron impurity

(b) Arsenic impurity

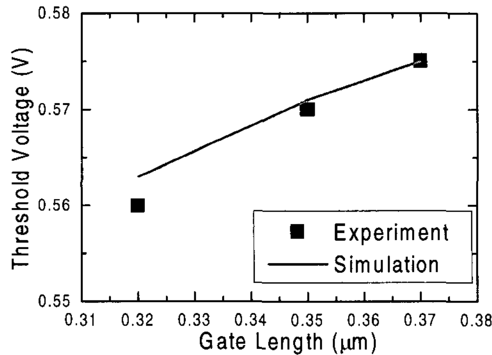
Fig. 5. Simulation and SIMS data of dopant redistribution due to the Co salicide process ($CoSi_2$ thickness = 430 Å)

4. APPLICATION

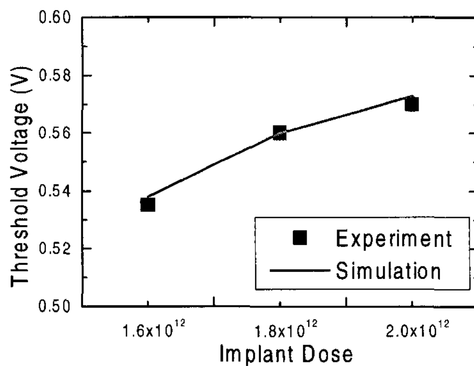
We applied the globally calibrated process simulator parameters to memory and logic devices to predict the optimum process conditions for target device characteristics. Figure 6 shows the DRAM NMOS threshold voltage simulation with the maximum 1 % error to the experimental data for the various gate lengths and channel doping conditions. The gate length was varied from 0.37 to 0.32 μm and the threshold voltage control implantation dose was varied from 1.16× 10^{12} to 2.0 × 10^{12}.

Based on the simulation, we can control the threshold voltage roll-off and the surface punch-through current in the n^- region. Figure 7 show the simulation results with errors less than 4 % for the reverse short channel

phenomena for 0.18 μm logic devices fabricated by the RTP and Co salicide process. The device was simulated following process sequence. First, N-well formation and threshold control implantation. Then the gate oxide and gate poly-silicon was constructed. Extension and source/drain were made by ion-implantation. Finally the activation was carried by rapid thermal annealing.

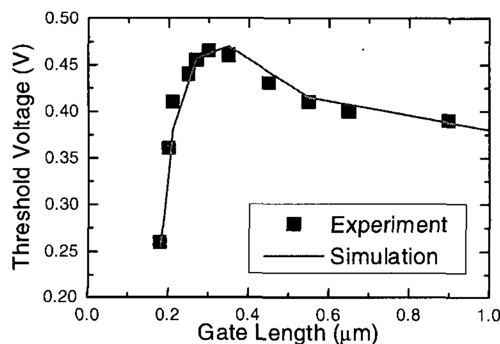


(a) Gate length vs. threshold voltage

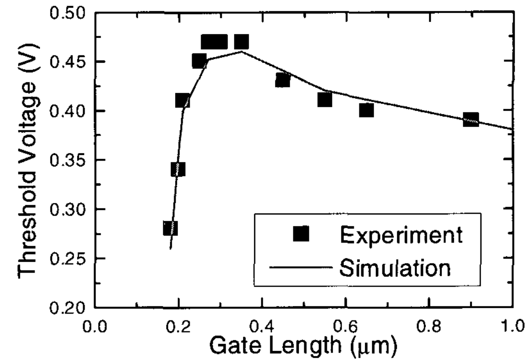


(b) Implant dose vs. threshold voltage

Fig. 6. The threshold voltages of a 256 M DRAM nMOS transistor depending on (a) various gate lengths and (b) channel implant dose variation.



(a) a 0.18 μm NMOS transistor



(b) a pocket-implanted 0.18 μm NMOS transistor

Fig. 7. RSCE simulation results compared with the experimental data for (a) a 0.18 μm NMOS transistor and (b) a pocket-implanted 0.18 μm NMOS transistor.

5. CONCLUSIONS

In conclusion, we have constructed a systematic calibration methodology for the ion-implantation and diffusion process simulation. With 175 SIMS profiles which cover the range of conditions of implant and diffusion processes in the fabrication lines, the dominant diffusion phenomenon in each process temperature region has been determined. The accuracy and efficiency of the globally extracted parameters have been successfully validated in the process design of DRAM and logic transistors. Useful agreement between measurement and simulation of device characteristics has been achieved.

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