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PRML Read Channel용 고효율, 저전력 FIR 필터 칩

(Highly Efficient and Low Power FIR Filter Chip for PRML Read Channel)

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요 약

본 논문은 고효율, 저전력을 갖는 PRML 디스크 드라이브 읽기 채널용 6비트, 8탭의 FIR 필터 칩을 제안한다. 제안된 필터는 병렬처리 구조를 채택하고 있으며 4단의 파이프라인으로 구성되어 있다. 곱셈 연산을 위하여 수정 부스 알고리즘을 사용하였으며 덧셈 연산을 위하여 압축회로 로직을 사용하였다. 전력 소모를 줄이기 위하여 CMOS 패스-트랜지스터 로직을 사용하였으며 싱글-레일 로직을 이용하여 칩의 면적을 감소시켰다. 제안된 필터는 실제 칩으로 구현되었으며 3.3V 전원을 공급하여 100MHz에서 120mW의 전력을 소비하고 1.88 × 1.38 ㎟의 면적을 차지한다. 구현된 필터는 유사 선폭의 공정을 사용한 기존 구조에 비해 약 11.7%의 전력이 감소하였다.

Abstract

This paper proposes a high efficient and low power FIR filter chip for partial-response maximum likelihood (PRML) disk drive read channels; it is a 6-bit, 8-tap digital FIR filter. The proposed filter employs a parallel processing architecture and consists of 4 pipeline stages. It uses the modified Booth algorithm for multiplication and compressor logic for addition. CMOS pass-transistor logic is used for low power consumption and single-rail logic is used to reduce the chip area. The proposed filter is actually implemented and the chip dissipates 120mW at 100MHz, uses a 3.3V power supply and occupies 1.88 × 1.38 ㎟. The implemented filter requires approximately 11.7% less power compared with the existing architectures that use the similar technology.

Keywords: FIR filter, CMOS pass-transistor, PRML, read channels, disk drives.

Ⅰ. Introduction

As the number of portable computers such as hand-held PCs and notebook computers dramatically increases, so does the demand for high density and high performance storage systems. Portable disk drives must have higher data rate processing, smaller size and lower power dissipation. Power consumption is a critical parameter in increasing battery life, and chip size is a critical parameter in reducing the device size in portable systems. In 1990, an advanced read/write technology called PRML was developed to meet these requirements[1]-[3]. The PRML technology is currently employed to increase both storage capacity and performance.

Prior to the development of PRML, low disk drive storage capacity was addressed via the (1,7) run length limited (RLL) coding scheme and the peak detection method[4],[5]. The peak detector reads bit streams by detecting the peaks of an analog signal. To correct the errors caused by inter-symbol inter

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-ference (ISI) and to effectively detect analog signal peaks, the data is encoded when it is written to the disk. However, since the encoder generates several bits to store an information bit in the disk, the data -encoding scheme for peak detection increases the amount of redundant information data written to the disk. Moreover, the method also reduces the data transfer rate[5], as the traditional read channels must read a bit stream consisting of several bits to detect one information bit. These methods are simple and inexpensive to implement. However, as the bit den -sity of a drive increases, so does ISI caused by the overlap of analog signal peaks streaming through the read/write head; the result is data bit errors[6]. Hence, it is difficult to distinguish between the signal and noise in the read channels using the peak detection method[1].

Therefore, the PRML read channels have been developed[1]-[3] to prevent bit errors caused by ISI by using digital filters that can shape the readback signal instead of separating signal peaks during the read operation[1],[4]. This detection method uses the Viterbi algorithm[5],[7]. PRML consists of two indepen -dent parts: partial response (PR) and maximum likelihood (ML). PR generates readback signals by accepting and controlling ISI, and ML detects the data sequence of bits most likely written to the disk[8]. The PRML read channels employ digital signal processing and maximum-likelihood detection to determine the most likely sequence of data bits written to the disk. Therefore, PRML channels have much less difficulty detecting signal peaks and can be adapted to high-density drives. Furthermore, as these channels use a more efficient RLL data enco -ding scheme rather than the (1,7) RLL coding scheme, the ratio of the information data to the stored data on the disk drives increases. The increase of the bit density leads to an increase in the data transfer rate. Therefore, the PRML read channels provide reduced cost, increased areal density, and improved performance at the same time[5].

The PRML read channels consist of analog front -end blocks, an analog-digital converter (ADC), and digital processing blocks[1],[5]. The analog front-end blocks use a read amplifier, a variable gain amplifier, and a low pass filter. The digital processing blocks employ an adaptive equalizer, a Viterbi detector, and a timing recovery block. The digital FIR filter descri -bed in this paper is a major part of the adaptive equalizer designed to increase transfer rates and recor -ding densities in the disk drive PRML read channel IC [9]-[12]. The FIR filters dissipate the most power and occupy a large area in the equalizer[9], [10]. The proposed filter chip can minimize power consumption and filter chip size while maintaining high processing performance.

The existing FIR filter that uses memories for the multiplication of data and coefficients[10] dissipates significant power. To reduce the power consumption, the filter chip employs a partial product generator (PPG) using the modified Booth algorithm for multip -lication and a compression scheme[11],[13]-[15] for addi -tion of partial products. Although the chip[11] can reduce the power consumption, the wiring complexity due to the dual-rail logic of its pass-transistor logic increases the area[16]. The proposed FIR filter chip [19]-[21] uses the single-rail logic, to reduce the chip area. The existing chip[11] uses the push-pull pass -transistor logic (PPL); however, the proposed chip uses CMOS pass-transistor logic to minimize the power consumption.

The proposed chip employs a parallel architecture using the modified Booth algorithm and a compressor logic that consists of four pipeline stages. The previ -ous chip[11] consists of three pipeline stages and its overall critical path contains nine MUXs. The propo -sed chip adds one more pipeline stage and changes the position of the pipeline registers to reduce the overall critical path. The overall critical path of the proposed chip contains six MUXs instead of nine. The architecture is optimized using the simplified PPG and the compact compressor circuit [13], [14]. The PPG and compressor circuit are designed using CMOS pass-transistor logic at the transistor level for high speed and low-power consumption. In the PPG, the scheme that removes the additional clear (CLR)

signal to make the PPG output '0'is used. The filter uses a 15-b final adder which consists of five 4-b conditional sum adder (CSA) blocks using the carry -select scheme. The existing final adder of an 8-tap FIR filter has the delay of six MUX stages[11]. How -ever, the critical path of the implemented final adder has only five MUXs. In addition, the design is tho -roughly optimized at both the circuit-level and transistor-level. The implemen -ted chip dissipates 120mW at 100MHz, uses a 3.3V power supply and occupies 1.88 1.38 mm2. The implemented filter requi -res approximately 11.7% less power compared with the existing architectures that use the similar techno -logy [10], [11], [17].

This paper is organized as follows. Section II descri -bes the proposed architecture, with its input delay stage, PPG, compressor, CSA, and its use of CMOS pass-transistor logics. Section III describes the imple -mentation, simulation results, and performan -ce comparisons with existing FIR filters. Finally, Section IV contains concluding remarks.

II. The Proposed FIR filter architecture

This section describes the overall architecture and details of the proposed filter shown in Figure 1. The filter chip consists of the input delay stage, PPG, compressors and CSA. The Pass-transistor logic used in the design is also described. The proposed filter architecture uses 6-bit, which is the number of resolution bits of typical adaptive equalizers for PRML read channels [9]. It consists of 8 taps and has 6-bit input, 6-bit coefficients and 15-b output. Coefficients of the filter are programmable for adap -tive equalization. The PPG is used for multiplication of data and coefficients. The PPG uses the modified Booth algorithm and generates three partial products as a result of one multiplication of 6-bit data and a 6-bit coefficient in one tap. Hence, twenty-four par -tial products are produced from eight taps.

The 24 : 2 compressor and CSA are used for the summation of partial products. The 24 : 2 compressor consists of one stage of the 3 : 2 compressor and three stages of the 4 : 2 compressor. After it adds twenty-four partial products to generate two rows, the CSA adds the two rows which are the results of the 24 : 2 compressor. The proposed architecture consists of four pipeline stages. In contrast, the previous chip [11] consists of three pipeline stages and its overall critical path contains nine MUXs. How -ever, the proposed chip adds one more pipeline stage and changes the position of the pipeline registers to minimize the critical path of each pipeline stage. Each critical delay of the pipeline stage is almost the same, except for the first pipeline stage. The critical delays of the first, the second, the third, and the fourth pipeline stages are three, six, six, and five MUX stages, respectively. Therefore, the overall critical path contains six MUXs.

1. Input Delay Stage and Partial Product Generator (PPG)

Figure 2 shows the input delay stage and PPG. The PPG generates three partial products as the result of multiplication of 6-bit data and a 6-bit coefficient. Since the filter has eight taps, it has eight PPGs and generates twenty-four partial products in

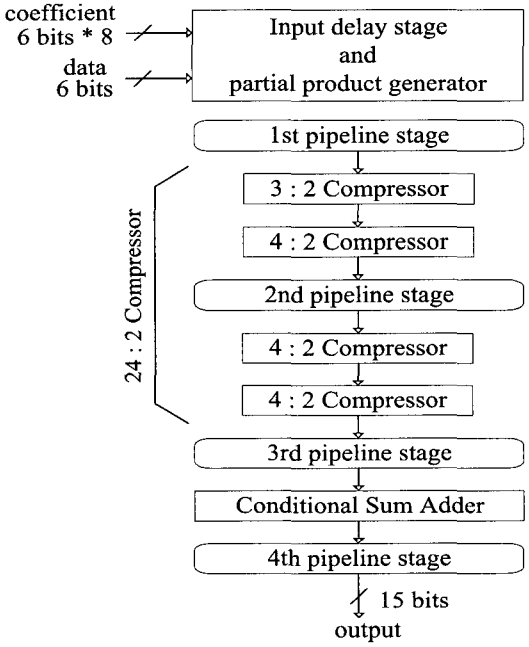

그림 1. FIR 필터 구조
Fig. 1. The FIR filter architecture.

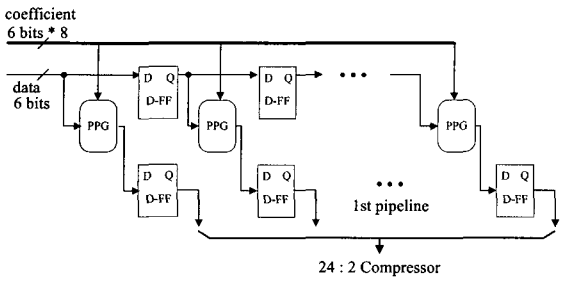

그림 2. 입력 지연단 및 부분곱 생성기
Fig. 2. The input delay stage and the partial product generator.

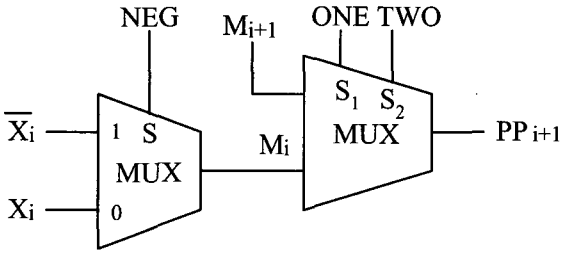

그림 3. 두 번째 및 세 번째 부분곱 생성기 블록도
Fig. 3. The diagram of the PPG for the second and third partial products.

표 1. 두 번째 및 세 번째 단의 부분곱 수정 부스 인코딩
Table 1. The modified Booth encoding of the second and third partial products.

Y2i+1	Y2i	Y2i-1	ONE	TWO	NEG	PP (Partial Product)
0	0	0	0	0	0	0X
0	0	1	1	0	0	+1X
0	1	0	1	0	0	+1X
0	1	1	0	1	0	+2X
1	0	0	0	1	1	-2X
1	0	1	1	0	1	-1X
1	1	0	1	0	1	-1X
1	1	1	0	0	1	0X

all eight taps per clock cycle.

Since the proposed filter has a 6-bit coefficient, $Y_5Y_4Y_3Y_2Y_1Y_0(Y_{-1})$, the booth encoder generates three partial products. The second and third partial products use the general modified Booth encoding shown in Table I [13]. There are five outputs, consisting of $-2X$, $-1X$, $0X$, $+1X$, $+2X$. According to the values of $Y_{2i+1}Y_{2i}Y_{2i-1}$, the values of ONE, TWO, and NEG are changed. If ONE is asserted, the

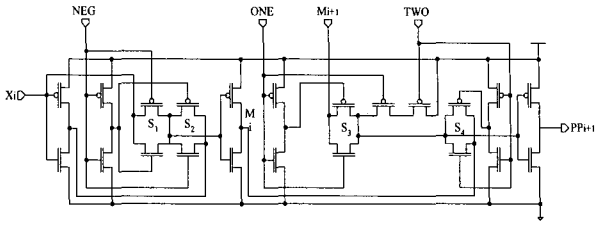

그림 4. 두 번째 및 세 번째 부분곱 생성기의 트랜지스터 회로
Fig. 4. The transistor logic of the PPG for the second and third partial products.

output PP is $1X$. If TWO is asserted, the output PP is $2X$. NEG means that the output PP has a negative value. Figure 3 shows the diagram of the second and third PPGs. PPG consists of two MUX logics. The first MUX is to select one value between a positive and a negative value and the other one is to select one value between Mi (X_I or $\overline{X_i}$) and Mi+1 (X_{i+1} or $\overline{X_{i+1}}$).

Figure 4 shows the logic implementation using the CMOS pass-transistor logic, which consists of twenty-two transistors. The first MUX consists of three inverters and two CMOS switches and the second MUX consists of three inverters, two CMOS switches, and two PMOS switches. If NEG is '0', S1is turned on and S2 is turned off, hence, Mi is $\overline{X_i}$. If NEG is '1', S1 is turned off and S2 is turned on, hence, Mi is X_i. Since the output inverter for buffering is added, PPi+1 has a negative value when NEG is '1'. If ONE is '1', S3 passes Mi+1 and if TWO is '1', S4 passes Mi. Note that two serial-connected PMOS transistors, which have the ONE and TWO input signals, are used instead of the CLR logic for a clear operation. When both ONE and TWO are '0', the circuit performs the clear operation and the output PPi+1 is '0'. This scheme removes the additional CLR signal. The inverter is added at the output of the PPG for buffering the output signal. The critical path of the PPG for the second and third partial products contains two MUXs.

Table II shows the proposed Booth encoding of the first partial product. The Booth encoding of the first partial product is proposed for simplification of the

표 2. 제안된 첫 번째 부분곱의 부스 인코딩
Table 2. The proposed Booth encoding of the first partial product.

0	0	CLR	0X
0	1	ONE	+1X
1	0	NT	-2X
1	1	NO	-1X

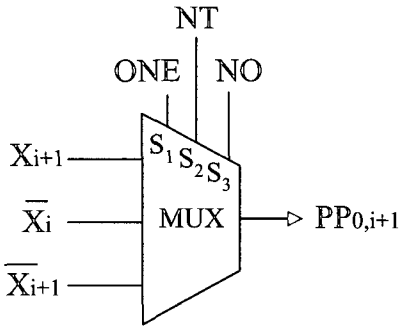

그림 5. 첫 번째 부분곱 생성기 블록도
Fig. 5. The diagram of PPG for the first partial product.

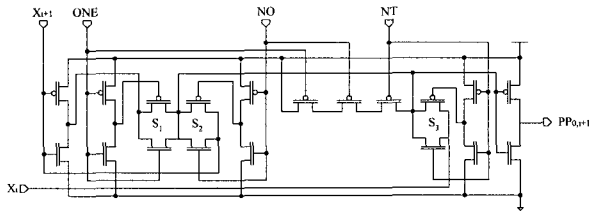

그림 6. 첫 번째 부분곱 생성기의 트랜지스터 회로
Fig. 6. The transistor logic of the PPG for the first partial product.

PPG logic. The LSB of the first Booth encoder input, denoted Y_{-1}, is always '0'. Hence, there are only four cases of Y_1Y_0, that is, "00", "01", "10", or "11", in the first Booth encoding. There is no $+2X$ as in the Booth encoding scheme of the first partial product. ONE, NT and NO mean $+1X$, $-2X$ and $-1X$, respectively. These signals are used in the PPG for the first partial product shown in Figure 5. Figure 5 shows the diagram of the first PPG. According to the values of Y_1Y_0, one of the signals, ONE, NT or NO, is asserted. If ONE, NT, or NO is asserted, PP0,i+1 is X_{i+1}, $\overline{X_i}$, or $\overline{X_{i+1}}$, respectively.

Figure 6 shows its logic implementation using the CMOS pass-transistor logic, which consists of nineteen transistors. The circuit has three CMOS switches, five inverters, and three PMOS switches. If ONE or NO is asserted, S1 or S2 is turned on and the output PP0,i+1 is X_{i+1} or $\overline{X_{i+1}}$, respectively. If NT is asserted, S3 is turned on and the output is $\overline{X_i}$. Note that three serial-connected PMOS transis -tors, which have the ONE, NT and NO input signals, are used instead of the CLR logic for a clear operation. The critical path of PPG for the first partial product contains one MUX.

2. 24 : 2 Compressor

The 24 : 2 compressor adds twenty-four partial products from eight PPGs. The 24 : 2 compressor consists of one stage of the 3 : 2 compressor and three stages of the 4 : 2 compressor. The compressor performs the carry-save addition to eliminate the carry-propagation delay [13]-[15].

Each 3 : 2 compressor adds three partial products from each PPG and generates two rows of results. When the partial products are loaded into the 3 : 2 compressor from the PPGs, the sign-bit extension is eliminated[15]. The PPG output is the one's comple -ment of the input data when the sign conversion of the input is required. Hence, two's complement sign conversion bits are used for the conversion from a one's complement number to a two's complement number. All twenty-four partial products are added by one stage of the 3 : 2 compressor to generate sixteen rows. The 4 : 2 compressors add four rows to generate two rows and three stages of the 4 : 2 compressor are used for adding sixteen rows to gene -rate two rows. Each of the 3 : 2 and 4 : 2 compre -ssors has three MUX stages as the critical path. The compact 4 : 2 compressor, which reduces the gate count and the critical path [13], [14] is used.

3. Pass-Transistor LogicFinal Adder

Figure 7 shows the block diagram of the proposed final adder. The final adder is a carry-select adder which consists of 4-b conditional sum adder blocks.

The second and third blocks use the typical carry-select scheme which selects the result based

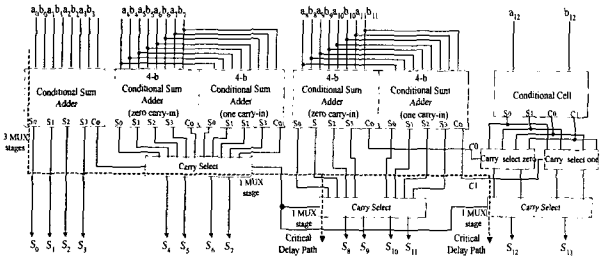

그림 7. 최종 단 덧셈기의 블록도
Fig. 7. The block diagram of the final adder.

on the value of the carry-in. The last block uses C0 (carry-out when carry-in is 0) output and C1 (carry -out when carry-in is 1) output of the third block and the carry-out of the second block. The 4-b conditional sum adder block has three MUX stages and the carry-select block has one MUX stage. Hence, the overall critical path of the final adder can be composed of only five MUX stages. However, the existing final adder of an 8-tap FIR filter has the delay of six MUX stages [11].

4. Pass-Transistor Logic

Recently, many high-speed and low-power transistor logic circuits have been investigated [16],[22]. Among them, complementary pass-transistor logic (CPL), suitable for a high-speed adder and low transistor count PPL, are frequently used [16]. However, since CPL and PPL have high wiring complexity due to the dual-rail logic, they increase the chip area. Hence, the single-rail logic is more appropriate to reduce the chip area and it is used in the proposed architecture.

All logics used in this paper consist of multiplexe -rs. It has been reported[16] that the multiplexer using the CMOS pass-transistor logic (i.e. the combination of NMOS and PMOS pass transistors) dissipates less power than multiplexers using other pass-transistor logics, such as CPL and PPL. Figure 8 shows the circuit diagram of the multiplexer using the CMOS pass-transistor logic. CMOS pass-transistor logics are often used for implementing multiplexers, XOR -gates, and flip-flops efficiently. Pass-transistor logi -cs, such as CPL and PPL, require the swing (or level) restoration circuitry to compensate the thresh

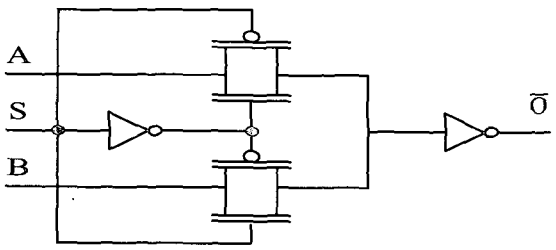

그림 8. CMOS 패스-트랜지스터 로직을 사용한 멀티플렉스의 회로도
Fig. 8. The circuit diagram of the multiplexer using the CMOS pass-transistor logic.

-old voltage drop (Vout = Vdd Vtn) through NMOS transistors while passing a logic '1'. However, no swing restoration circuitry is needed in the CMOS pass-transistor logic[16]. The swing restoration circuit -ry causes larger power consumption due to larger short circuit currents. To achieve low power consump -tion and high speed, the proposed architecture uses the CMOS pass-transistor logic with the single-rail logic.

III. Implementation and simulation results

The proposed filter has been implemented following the full-custom design methodology, using the Hyundai 0.65m CMOS technology (double-metal, Vtn = 0.75V, Vtp = -0.95V) and using the Cadence CAD tool. The design is optimized at the architecture-level, the circuit-level and the transistor-level. The simula -tion has been performed using HSPICE with level 49 NMOS and PMOS model parameters. The critical delays of each pipeline stage are shown in Figure 9. The proposed filter with the 3.3V supply voltage is simulated at 100MHz. We have thoroughly verified the function of the filter using random input data and coefficients. The delay times of the pipeline stages from the first stage to the fourth stage are 5.07 ns (Figure 9 (a)), 6.55 ns (Figure 9 (b)), 6.36 ns (Figure 9 (c)) and 5.87 ns (Figure 9 (d)). The overall critical delay time is measured to be 6.55 ns at the second pipeline stage, which consists of two 4:2 compressor logics and has 6 MUX stages. Therefore, the implemented FIR filter chip can operate at up to 150MHz.

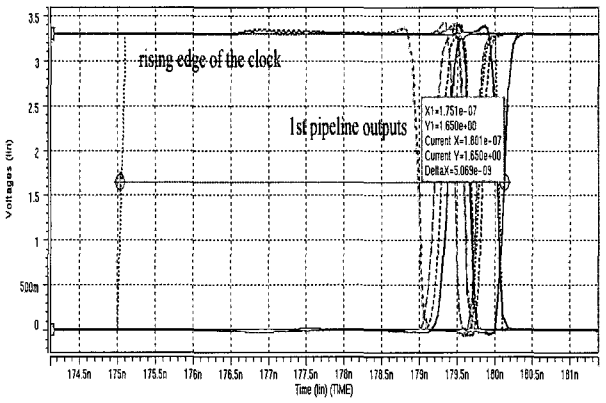

그림 9. (a) 첫 번째 파이프라인단의 최대 지연 시간
Fig. 9. (a) The critical delay time of the first pipeline stage.

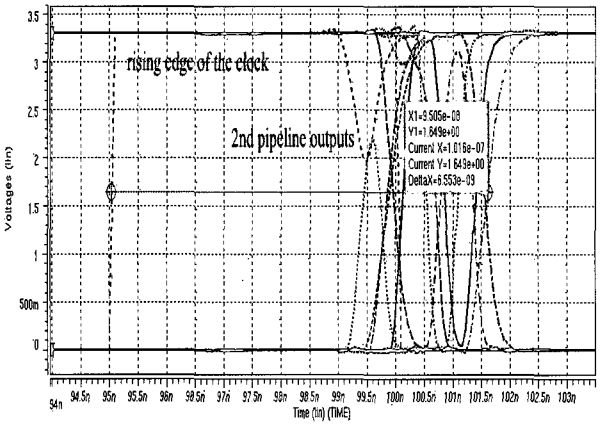

그림 9. (b) 두 번째 파이프라인단의 최대 지연 시간
Fig. 9. (b) The critical delay time of the second pipeline stage.

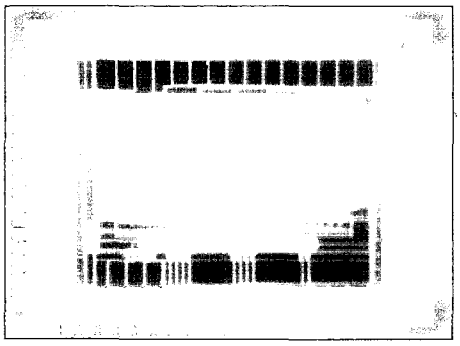

그림 10. (a) 구현된 칩의 마이크로그래프
Fig. 10. (a) The micrograph of the imple -mented filter chip.

Figure 10 shows the micrograph of the implemen -ted filter chip and the actual chip. The implemented filter chip has about 19,000 transistors, occupies 1.88 1.38 mm2 in area, uses a 3.3V power supply and dissipates 120mW at 100MHz.

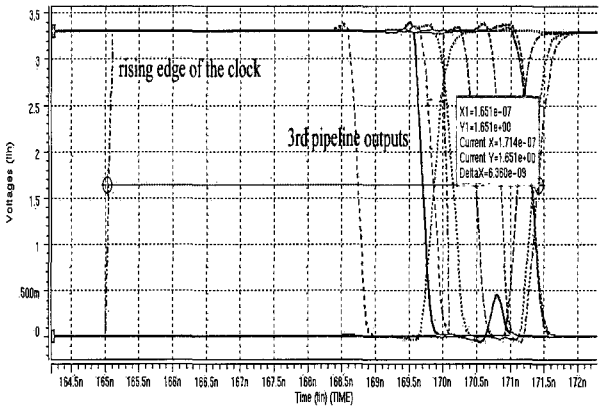

그림 9. (c) 세 번째 파이프라인단의 최대 지연 시간
Fig. 9. (c) The critical delay time of the third pipeline stage.

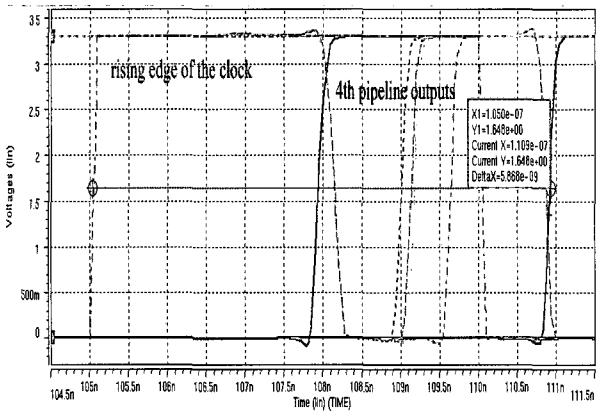

그림 9. (d) 네 번째 파이프라인단의 최대 지연 시간
Fig. 9. (d) The critical delay time of the fourth pipeline stage.

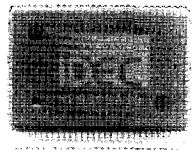

그림 10. (b) 구현된 칩 사진
Fig. 10. (b) The implemented chip.

Table III shows performance comparisons among the implemented filter chip and the existing architec -tures [10], [11], [17], [18]. It shows the technology used, maximum frequency, area, normalized area, power consumption, and power/MHz of each filter. To

표 3. 성능 비교
Table 3. The performance comparisons.

Paper	The proposed filter	[10]	[11]	[17]	[18]
Max. Freq. (MHz)	150	250	180	240	550
Area (㎟)	2.59	1.8	5.85	2.9	0.3
Norm. Area (㎟)	2.59	3.04	3.86	1.9	3.9
Power (mW)	120@ 100 MHz	340@ 250 MHz	140@ 100 MHz	426@ 240 MHz	36@ 550 MHz
Power/MHz (mW)	1.2	1.36	1.4	1.78	0.07

compare the areas, the normalized area is used, which is the area normalized by the 0.65m technology expressed by

$$\text{Normalized Area} = \frac{Area}{(Technology/0.65\mu m)^2} \quad (1)$$

If we assume that all the chips use the 0.65m process technology, the proposed chip can reduce the area by about 14.9% compared with [10], by about 32.9% compared with [11], and by about 33.6% compared with [18]. The Table III shows that the normalized area of the existing architecture [17] is very small. However, the power consumption of the architecture [17] is larger than the other architectures.

To compare the power consumption among the architectures, the power/MHz is used. The proposed filter dissipates 1.2mW/MHz and can reduce power consumption by about 11.7% compared with [10], by about 14.3% compared with [11], and by about 32.6% compared with [17]. Since the architecture in [18] was implemented using the 0.18㎛ technology, the power consumption of the architecture is quite low. However, the normalized area of the architecture is larger than the proposed architecture even though the architecture [18] used the 0.18㎛ technology. If the proposed architecture is implemented using the newest technology, it can dramatically reduce the power consumption and area and can increase the maximum operating frequency.

Ⅳ. Conclusion

A high efficient and low power FIR filter for PRML disk drive read channels has been proposed and implemented. The proposed architecture consists of four pipeline stages and employs a parallel processing architecture using the modified Booth algorithm and compressor logics. CMOS pass-transistor logic is used in order to reduce the power consumption, and single-rail logic is used in order to reduce the chip area. In general, the CMOS pass-transistor logic dissipates power at a lower rate than PPL and the single-rail logic has lower wiring complexity than the dual-rail logic. We have also proposed a final adder with the delay of five MUX stages instead of six, as [11]. The architecture is optimized using the simplified PPG and the compact compressor circuit. In addition, the design is also optimized at both the circuit-level and transistor-level. The chip was fabricated using the Hyundai 0.65m CMOS technology.

The implemented filter chip can operate at up to 150MHz, dissipates 120mW at 100MHz, uses a 3.3V power supply and occupies 1.88 × 1.38 ㎟. The filter chip requires approximately 11.7% less power compared with the existing architectures that use the similar technology.

참 고 문 헌

[1] A. Taratorin, PRML: A Practical Approach. Mountain View, CA: Guzik Technical Enterprises, 1995.

[2] E. Grochowski and R. F. Hoyt, "Future trends in hard disk drives," IEEE Trans. Magn., vol. 32, pp. 1850-1854, May 1995.

[3] J. D. Coker, R. L. Galbraith, G. J. Kerwin, and J. W. Rae, "Implementation of PRML in a rigid disk drive," IEEE Trans. Magn., vol. 27, pp. 4538-4543, Nov. 1991.

[4] R. D. Cideciyan, F. Dolivo, and R. Hermann, "A PRML system for digital magnetic recording," IEEE J. Select. Areas Commun., vol. 10, pp.

38-56, Jan. 1992.
[5] T. D. Howell, W. L. Abbott, and K. D. Fisher, "Advanced read channels for magnetic disk drives," IEEE. Trans. Magn., vol. 30, pp. 3807-3812, Nov. 1994.
[6] Seagate Technology. (2001). PRML: Seagate Uses Space Age Technology Today. [Online]. Available: http://www.seagate.com/support/kb/disc/tp/prml.html
[7] J. Hong, R. Wood, and D. Chan, "An experi-mental 180 Mb/sec PRML channel for magnetic recording," IEEE. Trans. Magn., vol. 27, pp. 4532-4537, Nov. 1991.
[8] H. Kobayashi and D. Tang, "Application of pro-babilistic decoding to magnetic recording systems," IBM J. Res. Dev., pp. 368-375, Jan. 1971.
[9] C. S. H. Wong, J. C. Rudell, G. T. Uehara, and P. R. Gray, "A 50 MHz eight-tap adaptive equalizer for partial-response channels," IEEE J. Solid-State Circuits, vol. 30, pp. 228-233, Mar. 1995.
[10] D. J. Pearson, S. K. Reynolds, A. C. Megdanis, S. Gowda, K. R. Wrenner, M. Immediato, R. L. Galbraith, and H. J. Shin, "Digital FIR filters for high speed PRML disk read channels," IEEE J. Solid-State Circuits, vol. 30, pp. 1517-1522, Dec. 1995.
[11] H. J. Ki, W. H. Paik, I. C. Hwang, K. Y. Chae, J. S. Yoo, and S. W. Kim, "A low power 8-Tap digital FIR filter for PRML read channels," Int. J. Electron., vol. 87, pp. 445-455, Apr. 2000.
[12] D. Moloney, J. O'Brien, E. O'Rourke, and F. Brianti, "Low power 200-Msps, area-efficient, five-tap programmable FIR filter," IEEE J. Solid-State Circuits, vol. 33, pp. 1134-1138, July 1998.
[13] G. Goto, A. Inoue, R. Ohe, S. Kashiwakura, S. Mitarai, T. Tsuru, and T. Izawa, "A 4.1-ns com-pact 54×54-b multiplier utilizing sign-select booth encoders," IEEE J. Solid-State Circuits, vol. 32, pp. 1676-1681, Nov. 1997.
[14] N. Ohkubo, M. Suzuki, T. Shinbo, T. Yamanaka, A. Shimizu, K. Sasaki, and Y. Nakagome, "A 4.4 ns CMOS 54 x 54-b multiplier using pass-transistor multiplexer," IEEE J. Solid-State Circuits, vol. 30, pp. 251-256, Mar. 1995.
[15] J. R. Choi, L. H. Jang, S. W. Jung, and J. H. Choi, "Structured design of a 288-Tap FIR filter by optimized partial product tree compression," IEEE J. Solid-State Circuits, vol. 32, pp. 468-475, Mar.1997.
[16] R.Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, pp. 1079-1090, July 1997.
[17] L. E. Thon, P. Sutardja, F. S. Lai, and G. Cole-man, "A 240 MHz 8-tap digital FIR filter for disk-drive read-channels," IEEE ISSCC Dig. Tech. Papers, pp. 82-83, Feb. 1995.
[18] K. Muhammad, R. B. Staszewski, and P. T. Balsara, "Speed, power, area, and latency trade-offs in adaptive FIR filtering for PRML read channels," IEEE Trans. on VLSI syst. vol. 9, pp. 42-51, Feb. 2001.
[19] B. G. Jo, J. Y. Kang, and Myung H. Sunwoo, "A low power and area efficient FIR filter chip for PRML read channels," in Proc. Int. Symp. Circuits Syst., May 2001, vol. 4, pp. 606-609.
[20] J, Y. Kang, B. G. Jo and Myung H. Sunwoo, "Implementation of an efficient FIR filter chip for PRML read channels," in Proc. IEEE Workshop on Signal Processing Systems Design and Implementation, Oct. 2001, pp. 201-208.
[21] M. H. Sunwoo, B. G. Jo, and J. Y. Kang, "Finite impulse response filter for partial response maxi-mum likelihood hard disk drive," Korea Patent Application # 10-2001-0007555, Feb. 15, 2001.
[22] M. Suzuki, N. Ohkubo, T. Shinbo, T. Yamanaka, A. Shimizu, K. Sasaki, and Y. Nakagome, "A 1.5-ns 32-b CMOS ALU in double pass-transistor logic," IEEE J. Solid-State Circuits, vol. 28, pp. 1145-1150, Nov. 1999.

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