An Investigation of Locally Trapped Charge Distribution using the Charge Pumping Method in the Two-bit SONOS Cell

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The direct lateral profile and retention characteristics of locally trapped-charges in the nitride layer of the two-bit polysilicon-oxide-nitride-oxide-silicon (SONOS) memory are investigated by using the charge pumping method. After charges injection at the drain junction region, the lateral diffusion of trapped charges as a function of retention time is directly shown by the results of the local threshold voltage and the trapped-charges quantities.

Keywords : SONOS, Flash memory, Charge pumping method, Locally trapped-charges, Two-bit storage.

1. INTRODUCTION

Recently, much study has been stimulated to achieve the ultrahigh-density nonvolatile memory (NVM) due to the tremendous portable electronic market. In order to overcome the scale-down problem of the conventional floating gate type devices, polysilicon-oxide-nitride-oxide-silicon (SONOS) memory has received much interest for next generation NVM due to simple process, low power operation, and high density[1-3]. Moreover, this SONOS technology has evolved into the two-bit storage devices, which are based on the localized trapped-charge in the nitride layer[4]. However, as the device size becomes smaller, data retention loss and lateral redistribution of trapped-charges in the two-bit SONOS memory have become a major reliability issue. It is known that the lateral redistribution of localized charge in the nitride layer may occur over long-time due to thermally activated charge hopping between traps. It changes the threshold voltage (V_{th}) of the memory cell and is hard to distinguish a difference between programmed and erased bits. In order to guarantee the reliable two-bit operation in localized charge-trapping, lateral redistribution in the nitride layer must be controlled as small as possible after program. Presently, while the physics of two-bit memory is well understood, there is no agreement about the physical processes for the data retention loss and lateral diffusion of trapped-charges in the two-bit SONOS cell. Therefore, to evaluate the spatial distribution of locally trapped charges is important for the two-bit operation. Previously reported characterization method is based on the comparison of the subthreshold slope with carefully calibrated 2-D simulations[5,6].

In this paper, however, we will directly show the spatial distribution and retention characteristics of locally trapped charges in a nitride layer using the single junction charge pumping method.

2. EXPERIMENTAL

Two-bit SONOS cells with channel width/length of 0.6 μm/0.5 μm are fabricated by using a conventional complementary metal-oxide-semiconductor (CMOS) process technology. The processing sequence is identical to CMOS technology, except for the formation of the oxide-nitride-oxide (ONO) dielectric stack. The process for an ONO gate dielectric is as follows: The bottom oxide is thermally grown at 900 ℃ in nitrogen diluted

with oxygen (5 % O_2 in N). A layer of nitride is deposited using low-pressure chemical-vapor deposition (LPCVD) at a low chamber pressure of 0.5 Torr and 770 ℃ by reacting of dichlorosilane (SiH_2Cl_2) : ammonia (NH_3) = 30 : 330 sccm. A blocking oxide is grown by using wet oxidation at 950 ℃ with a gas flow ratio of hydrogen (H_2) : oxygen (O_2) = 5 : 10 ℓ /min. A schematic cross-section and TEM image of the ONO layer of two-bit SONOS cell are shown in Fig. 1. The thickness of the ONO stack, as measured using transmission electron microscopy (TEM), is 34 Å for the bottom oxide, 73 Å for the nitride, and 34 Å for the top oxide.

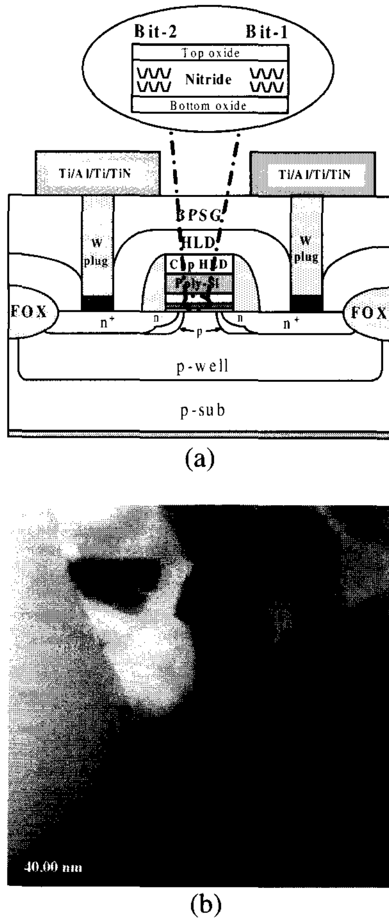

Fig. 1. Cross-sectional view (a) and TEM image of the ONO layer (b) of the two-bit SONOS cell.

The experimental setup for the single junction charge pumping measurement which allows the determination of the trapped-charges characteristics such as their local threshold voltage (local V_t) and their density (N_{ot}) within the nitride layer as a function of channel length is shown in Fig. 2. A square pulse is applied to the gate of the SONOS cell, the substrate is grounded, and semiconductor parameter analyzer (HP4155) is used to measure the charge pumping current (I_{cp}) from one junction while the other junction is left floating. The charge pumping pulses has a frequency of 1 MHz, 50 % duty cycle, rise/fall times of 5 ns and a fixed base voltage (V_b) of -1 V by a pulse generator (HP81101). Figure 2 show that applied gate pulse (V_h) and V_b are set to appropriate values to switch the SONOS memory between accumulation and inversion mode during applying the each cycle of the gate pulse.

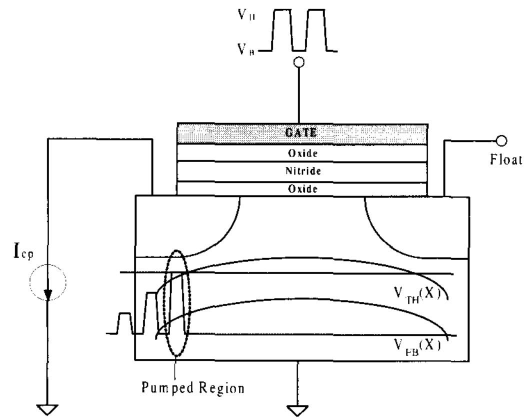

Fig. 2. Schematic diagram for measuring the single junction charge pumping current (I_{cp}).

3. RESULTS AND DISCUSSION

In order to determine the optimized condition of read drain voltage and programming time for a two-bit storage operation, the threshold voltage difference (ΔV_{th}) between the reverse and forward read with programming time as a parameter of read drain voltage is investigated after CHE injection, as shown in Fig. 3. Based on the experimental results of previous study, the gate and drain voltage for programming are fixed at 5 V [7]. Figure 3 implies that, when the read drain voltage larger than 2.5 V at programming time of 50 ~ 500 μs is applied, attainable V_{th} window (V_{th}>1 V) is achievable.

Figure 4 shows the I-V characteristics for the read drain voltage of 2.5 V compared to 0.1 V after CHE injection at the drain junction. Here, we present only the results from the drain injection in two-bit SONOS devices, although the same method can be readily applied to the source injection. Figure 4 shows that charges at both the source and the drain sides produce similar threshold voltage shift under a low read drain voltage (0.1 V). In this condition, the forward and reverse read operations have identical I_d-V_g curves because the surface potential (ϕ_s) is almost exclusively controlled by the gate. However, when a large read drain voltage (2.5 V) is applied, the difference between the forward and reverse read operation shows a significant

change in I-V characteristics. In this case, only reverse read in the source side can generate a threshold voltage shift and the forward read in the drain side has virtually no effect on the drain current because the surface potential ϕ_s close to the drain will be strongly influenced by the drain bias[8].

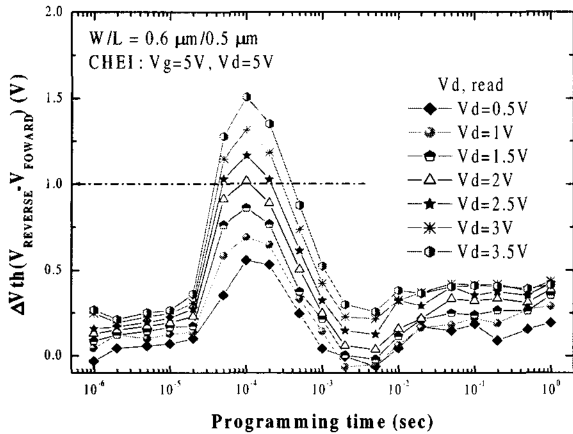

Fig. 3. The difference in threshold voltage between forward and reverse reads with programming time at various drain voltage.

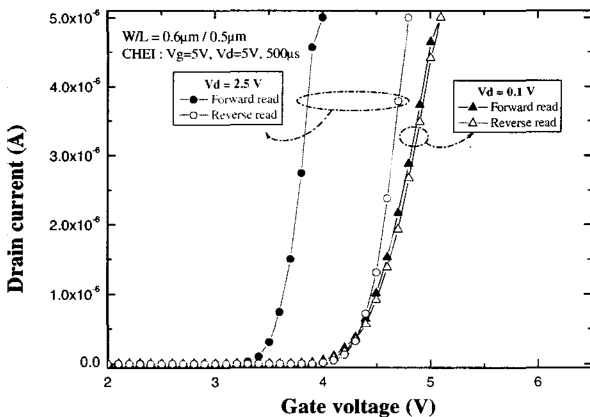

Fig. 4. I-V characteristics for different drain bias (V_d = 0.1 V, 2.5 V).

Based on the above experimental results, Fig. 5 shows the drain induced barrier lowering (DIBL) characteristics for the read drain voltage at 0.1 V and 2.5 V. The strength of DIBL is usually measured as the difference in V_{th} between a low and a high drain bias, and is defined as the V_{th} shift divided by the drain voltage variation ΔV_{ds} at the fixed drain current of 10^{-8} mA. The value of DIBL is calculated to be about 73 mV/V, it has no problem of read disturb. Thus, a read drain voltage of 2.5 V is determined for the two-bit storage operation.

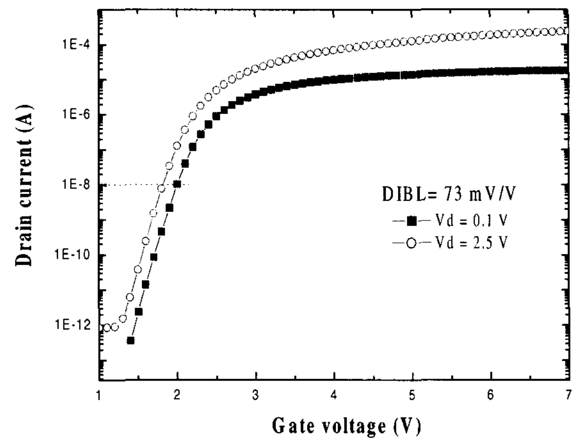

Fig. 5. DIBL characteristics.

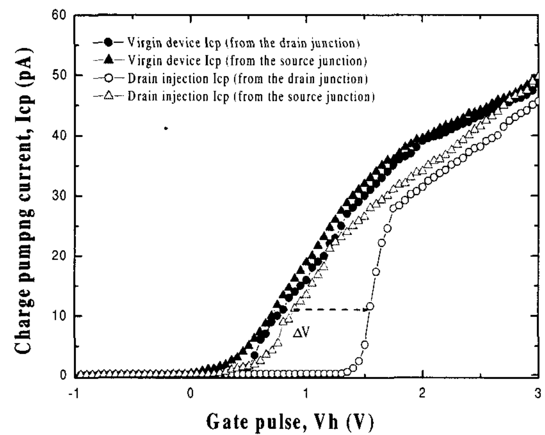

Fig. 6. Charge pumping current characteristics.

Figure 6 shows the charge pumping current(I_{cp}) measured separately from the source and drain junction at virgin and drain injection state. After drain programming, compared the I_{cp} of virgin device with the I_{cp} measured from the drain junction after drain injection, the I_{cp} curve of drain injection shows a rightward. This reason is that the local V_t at the drain region increases because charges are locally injected at drain region in the nitride layer. However, the I_{cp} curves from source junction appear the similar trend because charges are injected at the drain region.

After CHE injection at the drain junction region, the V_{th} for forward and reverse read as a function of retention time is shown in Fig. 7. It shows that the memory window is still maintained at more than 1 V after being extrapolated to 10 years. Thus, the requirement for data retention is guaranteed. Figure 7 shows that the vertical loss or lateral transport of trapped-charges as a function of retention time is expected to reduce the cell's threshold voltage. To

investigate these charges loss for the retention time, the charge pumping technique is used to investigate the spatial distribution of trapped-charges from the I_{cp} curves.

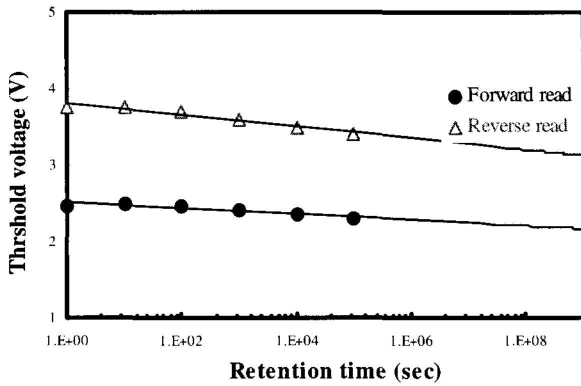

Fig. 7. Retention characteristics.

Figure 8 shows the I_{cp} curves for the retention time. Compared the I_{cp} of drain injection with I_{cp} after retention time of 10^4, 10^5 sec, the I_{cp} after 10^5 sec show a leftward shift (ΔV) because of the retention loss of injected charges. The magnitude of ΔV value is proportional to the local V_t and the trapped-charges quantities (N_{ot}).

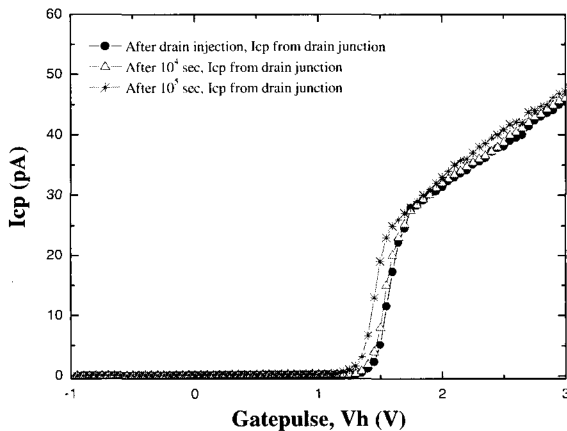

Fig. 8. I_{cp} curves for retention time.

Figure 9 shows the derived lateral profile of local V_t obtained at each position from the channel length after CHE injection at the drain junction. Simultaneously, the local Vt distribution as a parameter of retention time (10^4, 10^5 sec) is investigated. We define "local threshold voltage" as the gate voltage required to induce a certain density of minority carriers at the each position[9]. Compared to the local V_t distribution of virgin device, the local V_t at the drain/source region after drain injection increases asymmetrically. This implies that negative charges are trapped locally at drain region. After retention time of 10^4 sec, the change of local V_t doesn't nearly appear. But, after 10^5 , the local Vt show a little decrease near the drain side whereas a little increase near the 0.2 μm compared with Vt of 10^4 sec, as shown in fig.9. It implies that the lateral diffusion of trapped charges is slightly occurred.

Figure 10 shows the derived profiles of trapped charges for retention times as a function of the channel length. After charges are injected at the drain region, the observed quantities of trapped charges are approximately 1.8×10^{12} cm^{-2} near the drain junction. This result demonstrates that the electrons generated by CHE injection at the drain region are locally trapped at the drain region. After 10^5 sec, charge loss through both the bottom oxide and lateral diffusion of trapped charges has directly been found.

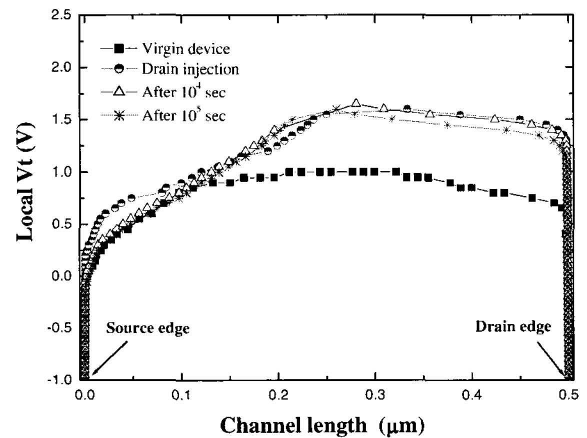

Fig. 9. Local V_t as a function of the channel length after drain injection.

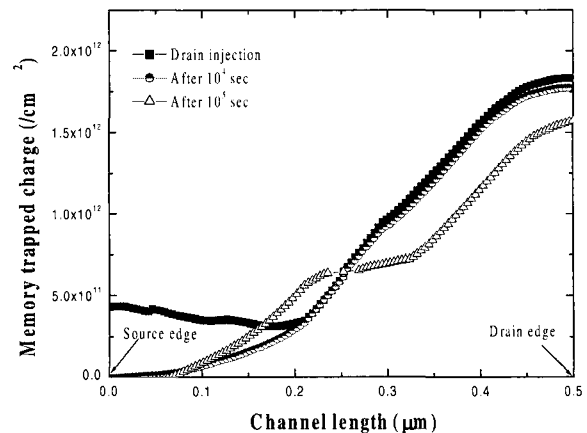

Fig. 10. Lateral profiles of memory trapped charge.

4. CONCLUSIONS

In this paper, the spatial profile and retention loss of locally trapped charges in CHE programmed SONOS cells are directly investigated by utilizing the single junction charge pumping technique. After the drain injection, we demonstrate that the trapped-charges are locally injected at the drain region. After 10^5 sec, the lateral redistribution of charges in the nitride layer has been found from the results of local V_t and the shifted quantities of trapped charges. Therefore, the single charge pumping method is the feasible technique to analyze adequately the lateral charge transport in a two-bit SONOS memory.

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