Wafer Burn-in Method of SRAM for Multi Chip Package

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This paper presents the improved burn-in method for the reliability of SRAM in Multi Chip Package (MCP). Semiconductor reliability is commonly improved through the burn-in process. Reliability problem is more significant in MCP that includes over two chips in a package, because the failure of one chip (SRAM) has a large influence on the yield and quality of the other chips - Flash Memory, DRAM, etc. Therefore, the quality of SRAM must be guaranteed. To improve the quality of SRAM, we applied the improved wafer level burn-in process using multi cells selection method in addition to the previously used methods. That method is effective in detecting special failure. Finally, with the composition of some kind of methods, we could achieve the high quality of SRAM in Multi Chip Package.

Keywords : Burn-in, Reliability, Multi Chip, Stress

1. INTRODUCTION

Recently electronic industries are growing rapidly as the semiconductor technology is developed. That enables us to use many portable products – cellular phones, digital cameras – through our living space. Many companies are developing higher-end, higher-capacity products. Corresponding to the trend, semiconductor industry is developing a higher-performance memory. This higher-performance memory is known as a fusion memory. A Fusion Memory is the compound of Flash Memory, DRAM, SRAM, etc in a package. Using a fusion memory, the manufacturer of electronic product can have the advantage in space, performance, size, and cost. In addition to those merits, the density of memory is also important requirement. Thus, we developed higher-density SRAM using SRAM-interface and DRAM cells, so called 1-transistor SRAM. This memory is usually used for Multi Chip Package (MCP).

In this paper, we consider seriously that the defect of each memory causes the failure of overall memory in MCP. That is the reliability problem of bare chip[1]. Semiconductor chip reliability is commonly improved through burn-in, including high temperature, high voltage, and long time[2]. To achieve the good reliability of 1-transistor SRAM in MCP, we apply new burn-in method in addition to the previous method for DRAM cells.

2. CONSIDERATION OF PREVIOUS METHOD

Most memory products are processed as follows [Fig.1].

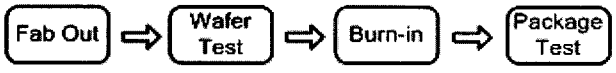


Fig. 1. Test sequence of memory product.

As shown in Fig.1, memory test is divided roughly into two steps – wafer level and package level. In general, burn-in is processed between two steps to ensure the

reliability and quality guarantee of packaged products. Burn-in has very severe condition - high temperature over 100 ℃, higher voltage than chip power voltage[3].

Recently, as memory products are compounded, quality in wafer level before assembly process has become very significant. Therefore, not only we but most of all semiconductor companies have burn-in process in a wafer level[4].

2.1 Conventional wafer burn-in method

In the conventional wafer burn-in method, stress is applied to memory cells. Most failure locations are pass gate, capacitor dielectric and storage node junction. To apply a stress effectively, each Word Line (W/L) and Bit Line (B/L) has a different electrical level and disturbs neighbor lines. Methods usually used are divided into 3 cases[5].

(i) True/Complement method
- W/L 0, 3 and W/L 1, 2 have different electrical level.

(ii) Even/Odd method [Fig.2]
- W/L 0, 2 and W/L 1, 3 have different electrical level.

(iii) Sensing method
- B/Ls have different electrical level when reading a cell data, but not connected to data output signal line.

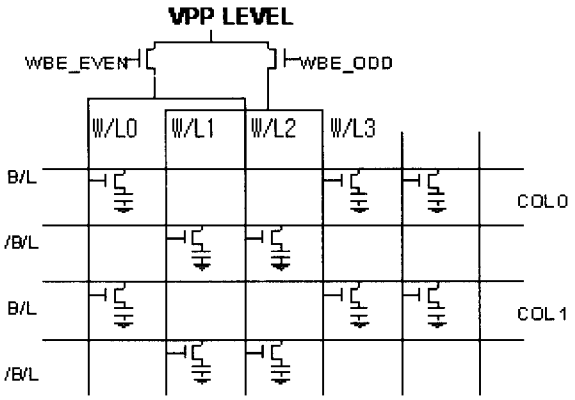


Fig. 2. Typical structure for a conventional burn-in. Each W/L is activated with other W/L having same electrical level at the same time.

For these methods, we can give an electrical stress to memory cell with an external signal for test mode in a burn-in step[6].

As a result of those burn-in methods, we can screen out gate oxide failure, excess junction leakage, and inter-layer dielectric breakdown[1,7]. In addition, after all word lines are activated, we can give a stress between a bit line and a bit line, a cell and a cell through bit line sensing.

2.2 Comparison of wafer and package burn-in

In Multi Chip Package, if any chip has a failure, other chips also go to fail. Thus, it is very important whether wafer level quality is reliable or not. First, we compared the failures of package burn-in with those of wafer burn-in.

Figure 3 shows the result of package burn-in failure. Main failures are classified into 3 types – failures of a bit line in a cell block, a single bit, and a bit line in a sensing circuit.

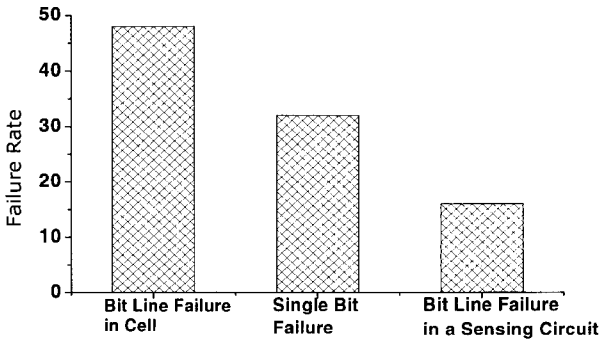
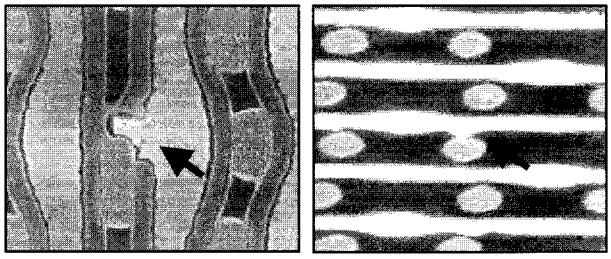


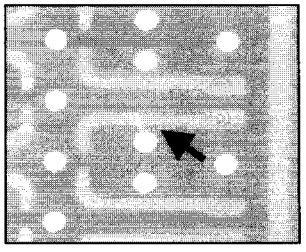
Fig. 3. Main failures after package burn-in. Most failures are occurred in a cell block.

The appearances of each failure are as follows.



(a) Bit line failure in a cell block

(b) Single bit failure



(c) Bit line failure in a sensing circuit

Fig. 4. Appearance of failures after package burn-in. All failures must be reproduced in wafer burn-in.

These figures are main failure of memory product-short failure. Now, we consider the correlation problem of both wafer level and package level. Thus, we experiment with going on the bath-tub evaluation[8] by conventional wafer burn-in method.

Table 1. Conventional wafer burn-in condition.

Method	Activation Cell	Cycle Time	Power
True/Comp	Half Word Line	1m sec	5.7 V
Eve/Odd	Half Word Line	1m sec	5.7 V
Sensing	Half Word Line	5m sec	5.7 V

By the condition described above, we progress bath-tub evaluation and as a result of that, we get the saturation level that failures was not occurred any more after 10 minutes [Fig. 5].

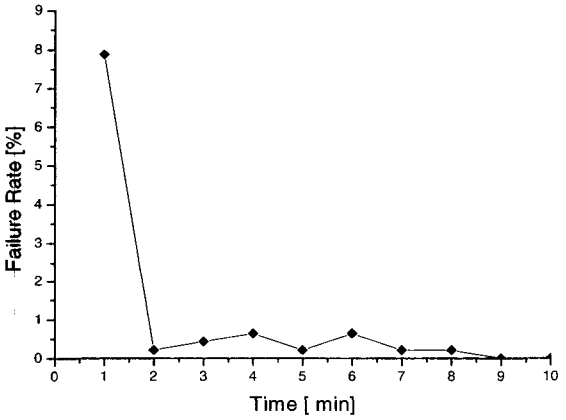


Fig. 5. The result of wafer burn-in bath-tub evaluation after 10 min, no failure was observed.

As mentioned before, failure rate has become zero after 10 minutes. However, failure case is different from that of package burn-in [Fig. 3]. The most different point is that the portion of bit line failure in sensing circuit is very small. [Table. 2]

Table 2. Failure case after conventional wafer burn-in.

Failure case	Rate
Single Bit	46 %
Bit Line failure in Cell	41 %
Word Line Failure	5 %
Bit Line failure in Sensing Line	2 %

Another different point is the increase of single bit failure. Wafer burn-in failures may include more hard-defective failures. Those could be caused by the particle occurred during fabrication. Most particles have an influence on cell blocks that have the largest section of chip area. Therefore, we think that single bit failure was increased in a wafer level than a package level.

3. IMPROVED WAFER BURN-IN METHOD

For the higher quality of SRAM bare chip in MCP, we introduced wafer burn-in. However, there remains problem that the tendency of wafer burn-in failure does not agree with that of package burn-in failure. The different failure mode between a wafer and a package is bit line failure in a sensing line. The point (shown in Fig. 4 (c)) is located in the sensing circuit between a data line and a cell block. Conventional wafer burn-in has been carried out only focused on memory cells so far. An undetected point in a conventional wafer burn-in is outside cell block, strictly core circuit area. We need to give an electrical stress to the core area.

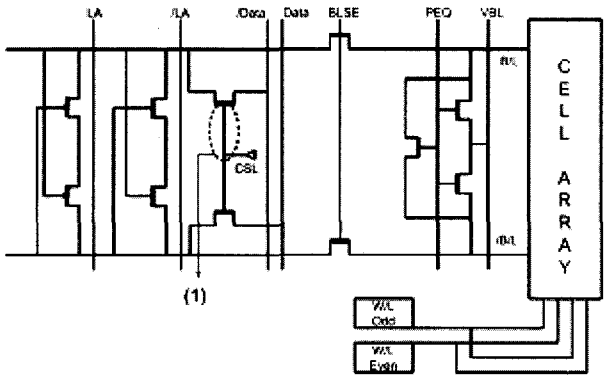


Fig. 6. Location of bit line failure in sensing circuit, this point is the location where data from cell block is transferred to peripheral signal line. Conventional burn-in cannot stress this point (1) and screen out this failure .

To give an electrical stress to sensing line, we used a peripheral data line for write and read operation during burn-in. Normally, conventional wafer burn-in uses an external signal line for activating half of all W/Ls. However, if we use a peripheral data line for burn-in, sequentially only one cell will be selected at each cycle and test time will be taken much longer than before. Therefore, we designed additional burn-in circuit that

can select multi cells (over 8 W/Ls, over 8 B/Ls) at the same time to overcome the test time problem. In other words, write and read operation behave normally, but multi cells are selected and data are transferred to a sensing line at a time.

In Fig. 6, (1) is the failure point of "the bit line failure in sensing circuit." This point is the location where a data from a cell block is transferred to a peripheral signal line. CSL (Column Select line) is a gate signal connecting a cell data line with a output signal line. Fig.4 (c) shows that a short failure has occurred between CSL gate and sensing line contact. Inter-layer dielectric was broken between two points and Tungsten contact met the gate poly slightly.

For improved burn-in method, some circuitry was inserted, but area overhead is negligible. Only a small number of address decoders are disabled for multi cells selection.

Table 3. Failure chips after improved wafer burn-in.

Method	Failure chips, After WBI	Single Bit	Bit Line	Sensing Circuit
True/Comp.	35	19	16	0
Even/Odd	27	13	14	0
Sensing	47	26	21	0
New Method	40	24	13	3

Table 3 shows the result of wafer burn-in after improved method is applied. The result indicates that only new method detects bit line failure in sensing circuit. Conventional methods also detect most failure, but because stress is transferred to only cell block through external signal line, those methods cannot detect the sensing line failure in a sensing circuit.

Through accurate failure analysis and modeling, we adopt improved wafer burn-in method and achieved the accordance of wafer and package burn-in failure.

Finally, we decided to set burn-in condition to the mixture of a conventional and a new method. The conventional method can be more efficient to detect the failure in a cell block and the new method is more detectable on the failure in the peripheral circuit. Total burn-in time is determined to be 10 minutes as evaluated in Fig. 5.

4. SUMMARY

This paper presents an improved method for wafer burn-in. External environment and internal schematic revisions are all included. By that method, we can detect the special failure that cannot be caught by conventional methods. In particular, two ideas are proposed for the detection of particular failure. Those are the use of peripheral data line for burn-in and selecting multi cells at a time. The former is for screening the peripheral failure and the latter is for reducing test time. We achieved confidential reliability in wafer level almost reaching package level. The reason why this work is needed is that this SRAM is for MCP. Thus, reliable quality in bare chips can minimize the bad influence to other chips and raise the yield and quality of MCP. Finally, after we adopted the two burn-in methods, failure rate was decreased under100 ppm and also obtaing "known good die" can become much more realistic.

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