The Design and Implementation of a Control System for TCSC in the KERI Analog Power Simulator

Jin-Hong Jeon†, Kwang-Su Kim*, Ji-Won Kim* and Tae-Kyoo Oh**

Abstract - This paper deals with the design and implementation of a TCSC (Thyristor Controlled Series Capacitor) simulator, which is a module for an analog type power system simulator. Principally, it presents configuration of controller hardware/software and its experimental results. An analog type power system simulator consists of numerous power system components, such as various types of generator models, scale-downed transmission line modules, transformer models, switches and FACTS (Flexible AC Transmission System) devices. It has been utilized for the verification of the control algorithm and the study of system characteristics analysis. This TCSC simulator is designed for 50% line compensation rate and considered for damping resister characteristic analysis. Its power rate is three phase 380V 20kVA. For hardware extendibility, its controller is designed with VMEBUS and its main CPU is TMS320C32 DSP (Digital Signal Processor). For real time control and communications, its controller is applied to the RTOS (Real Time Operation System) for multi-tasking. This RTOS is uC/OS-II. The experimental results of capacitive mode and inductive mode operations verify the fundamental operations of the TCSC.

Keywords: Control, FACTS, RTOS, Simulator, TCSC

1. Introduction

FACTS technology has developed into sophisticated system technology that combines conventional power system technologies with power electronics, micro-process control, and information technology. Its objectives are achieving the enhancement of power system flexibility and maximum utilization of power transfer capability through improvements in system reliability, controllability, and efficiency. The objectives of FACTS engineering technology are to obtain basic information regarding location application, types, capacity and control algorithm of the FACTS device by analyzing requirements of the power systems and proposing design and manufacturing requirements of the technological rates. Compared to conventional power system control devices, information technology based on FACTS devices is expected to enhance the competence of the power system industry and result in technological developments in the related areas. Moreover, introduction of the market system to the power system industry is expected to result in increased demand of the methods necessary for network congestion management and power system flexibility enhancement. Therefore, it is imperative to develop technologies for determining location of the FACTS device, controller type and capacity through device analysis, to analyze and evaluate FACTS application, to decide methods for structuring the FACTS system and basic specifications, etc.[1-4].

As its compensation type, the representative devices of FACTS System are TCSC, STATCOM (Static Synchronous Compensator) and UPFC (Unified Power Flow Controller). For simulating the operation status of power systems, an analog simulator or a digital simulator such as RTDS (Real Time Digital Simulator) has been commonly used. An analog simulator is a scaled-down type of hardware that represents the characteristics of a target power system. It is able to operate the test system as a real situation. A digital simulator is a software program model that is user defined and its simulation results are real time signals. It can be interfaced with any other real devices by using a various type amplifier. Its merits are flexibility and repeatability [1, 4].

In this paper, we present the design and implementation of the TCSC simulator, which is a module of an analog type power system simulator. Principally it presents configuration of controller hardware/software and its experimental results. An analog type power system simulator consists of many power system components, which include various types of generator models, scale-downed transmission line modules, transformer models, switches and FACTS devices. It has been utilized for the verification of control algorithms and the study of system characteristics analysis. This TCSC simulator is designed

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2. TCSC System

2.1 The characteristics of TCSC impedance

The basic TCSC scheme was proposed in 1986 by Vithayathil and others as a method of "rapid adjustment of network impedance". It consists of the series compensating capacitor shunted by TCR (Thyristor-Controlled Reactor, which is connected with a thyristor and a reactor by series). In a practical TCSC implementation, several such basic compensators may be connected in series to obtain the desired voltage rating and operating characteristics. This arrangement is similar in structure to the TSSC (Thyristor Switched Series Capacitor, which is connected with a thyristor and a capacitor by parallel) and, if the impedance of the reactor is sufficiently smaller than that of the capacitor, it can be operated in an on/off manner like the TSSC. However, the basic idea behind the TCSC scheme is to provide a continuously variable capacitor by means of partially canceling the effective compensating capacitance by the TCR. Since the TCR at the fundamental system frequency is a continuously variable reactive impedance, controllable by delay angle α, the steady-state impedance of the TCSC is that of a parallel LC circuit, consisting of a fixed capacitive impedance, X_C, and a variable inductive impedance, $X_L(\alpha)$, that is,

$$X_{TCSC}(\alpha) = \frac{X_c X_L(\alpha)}{X_L(\alpha) - X_c} \quad (1)$$

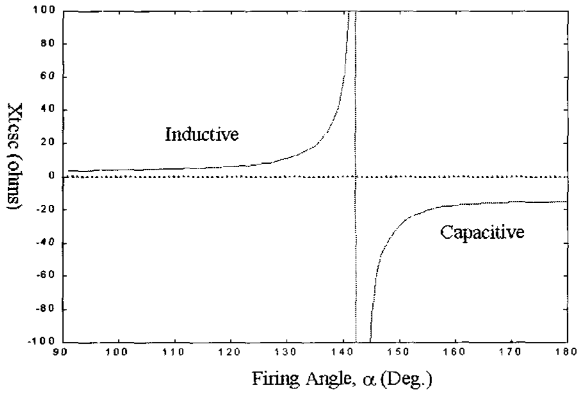

Fig. 1 Impedance Characteristics of TCSC

where,

$$X_L(\alpha) = X_L \frac{\pi}{\pi - 2\alpha - \sin 2\alpha}, \quad X_L \le X_L(\alpha) \le \infty$$

$X_L = \omega L$, and α is the delay angle measured from the crest of the capacitor voltage (or, equivalently, the zero crossing of the line current). The impedance of the TCSC by delay is shown in Fig. 1[1].

2.2 A design of TCSC impedance

An analog type power system simulator in KERI has transmission line modules that are modeled to be 345kV-100km. It is a π-equivalent circuit model and its impedance is 44mH (16.587 Ω). The impedance of the TCSC simulator is defined by that of the transmission line module. The compensation rate of the TCSC is determined to be less than 50% and its characteristics are verified by EMTDC simulation. The resonance frequencies of the TCSC simulator are listed in Table 1 by inductance and capacitance. As described above, we determine the 1.5mH and 3.5mH and the inductance value of the TCSC simulator for satisfied resonance frequency [5, 6].

Table 1 Resonance Frequency of TCSC Simulator as LC Parameter

Inductance(L) \ Capacitance(C)	500uF	1000uF
5.0mH	100 Hz	71 Hz
3.5mH	120 Hz	91 Hz
1.5mH	184 Hz	130 Hz
0.7mH	269 Hz	190 Hz

An impedance of the TCSC system can be variable by its delay angle because of its LC parameter and structure. An impedance characteristic of the delay angle is referred to as the impedance characteristic curve of the TCSC. As an impedance characteristic of the TCSC system in steady-state, the system can be in resonance state during a specific frequency range, so it is prevented from restricting the delay angle. In the case of 1000uF-1.5mH and 500uF-3.5mH, respectively, the operating rages of the TCSC delay angle are as follows.

- 1000uF-1.5mH
  - . Lead operation mode: $105^\circ \sim 125^\circ$
  - . Lag operation mode: $140^\circ \sim 160^\circ$
- 500uF-3.5mH
  - . Lead operation mode: $100^\circ \sim 120^\circ$
  - . Lag operation mode: $145^\circ \sim 165^\circ$

3. TCSC Controller

The major functions of the TCSC controller are the following: sensing input and output voltage and TCSC current; monitoring the status of switches; controlling voltage and current in the TCSC system; firing the thyristor by delay angle; and communication with the monitoring system. As such, the TCSC controller must be highly capable, and able to perform rapid calculations in a stable and flexible manner. In the case of a single board type controller, hardware is restricted with expendability and flexibility, and also, in the case of software, its main operating mechanisms are interrupt based system (time and event). In a interrupt based system, if a lot of interrupt is generated concurrently, in that case, it is very important that programmer estimate interrupt and controller interrupt service scheduling for system's reliabilities. If an event that programmer don't expect is occurred, the possibility of system's abnormal operation will be greatly increased. For that reason, the hardware structure of the TCSC controller was decided to be VMEBUS based hardware, by using the VMEBUS structure. As such, it has increased expendability and flexibility. In the case of software, it is programmed based on RTOS. RTOS is an operating system software that can process many functions in a specific time by concurrent priority [7, 8].

The control hardware is shown in Fig. 2 and its memory map is listed in Table 2. The control software structure is presented in Fig. 3.

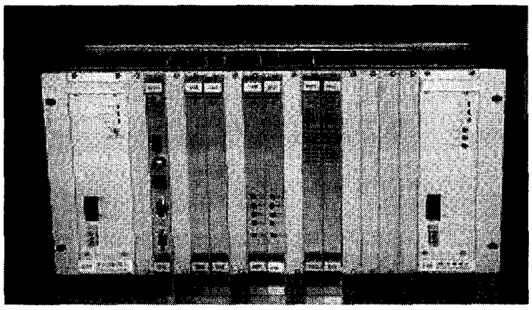

Fig. 2 TCSC Control Hardware

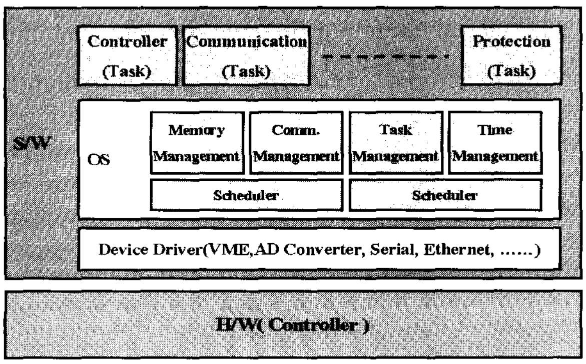

Fig. 3 Software Structure for TCSC Controller

Table 2 Controller Memory Map

Address	Contents	Size	Chip select	Strobe	Function
0x00000h 0x07FFFFh	boot program	512k bytes	ROM (EPROM)	STRB0	0x000000h 0x7FFFFFh reset-vector location external memory (8.192M words)
0x400000h 0x47FFFFh	program download	512k bytes	FROM	STRB0	
0x600000h 0x63FFFFh	main memory	256k words	RAM	STRB0	
0x800000h 0x807FFFh	reserved	32k words			
0x808000h 0x8097FFh	peripheral bus memory -mapped registers	6k words			0x808000h DMA0 0x808010h DMA1 0x808020h Timer0 0x808030h Timer1 0x808040h Serial Port
0x809800h 0x80FFFFh	reserved	26k words			
0x810000h 0x82FFFFh	external memory	128k words		IOSTRB	0x810000h UART 0x811000h RTC 0x812000h VIC068 0x813000h VME interrupt re-enable 0x814000h reset control 0x815000h interrupt acknowledge 0x816000h DIP switch 0x817300h RTL8019AS
0x830000h 0x87FDFFh	reserved	319k words			
0x87FE00h 0x87FEFFh	RAM block 0	256 words			
0x87FF00h 0x87FFFFh	RAM block 1	256 words			
0x880000h 0x8FFFFFh	external memory	512k words			
0xA00000h 0xA0FFFFh	VME BUS access	128k words	VME A16/D16	STRB1	0x900000h 0xFFFFFFh external memory (7.168M words)
0xC00000h 0xFFFFFFh	VME BUS access	1M words	VME A24/D16	STRB1	

4. TCSC Simulator and Its Operating Results

The basic structure of the TCSC simulator and its prototype is displayed in Fig. 4 and Fig. 5, respectively.

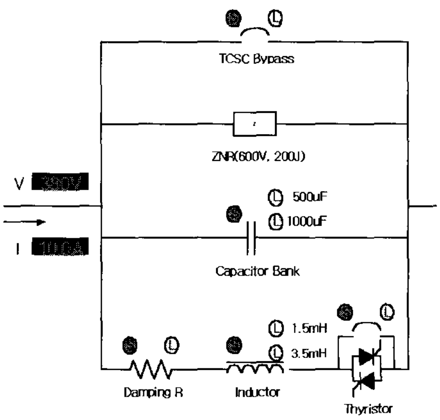

Fig. 4 Basic Structure of a TCSC Simulator

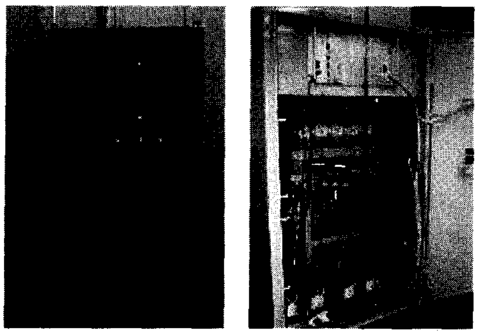

Fig. 5 Prototype of a TCSC Simulator

In Fig. 4, the TCSC simulator consists of capacitor bank module, damping resister module, reactor module and thyristor module. And its status is monitored at the front panel of the simulator. The prototype TCSC simulator was tested in a power system simulator and the results of the test operation for basic function are shown in Fig. 6, Fig. 7 and Fig. 8, respectively.

In Fig. 6, the thyristor is in off status in all ranges. The result of the test indicates that the voltage and current of the TCSC has a 90° phase status difference. In Fig. 7, the delay angle of thyristor firing is 112° . In that state, the TCSC system is operated in lag mode, and as a result, the voltage and current of the TCSC has a lag phase difference. In Fig. 8, the delay angle of thyristor firing is 155° . In that state, the TCSC system is operated in lead mode, and as a result, the voltage and current of the TCSC has a lead phase difference.

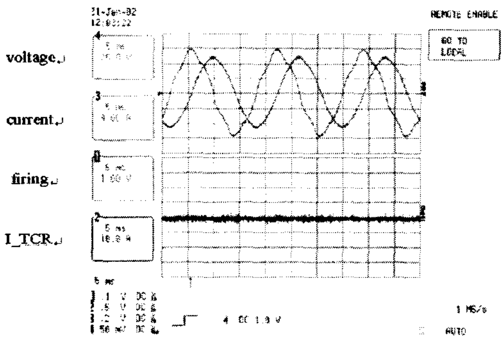

Fig. 6 Thyristor Off (delay angle: 180°)

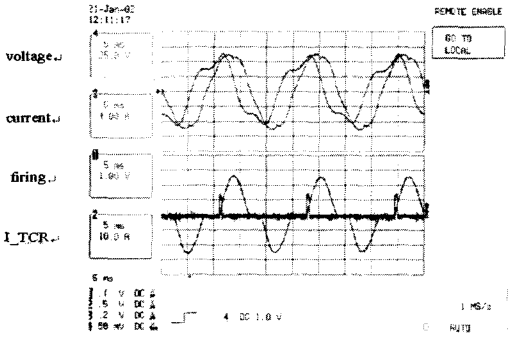

Fig. 7 Lag mode operation (delay angle: 112°)

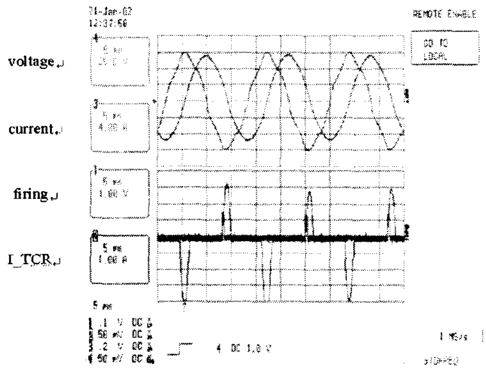

Fig. 8 Lead mode operation (delay angle: 155°)

5. Conclusion

In this paper, we present the results of design and implementation for a prototype TCSC simulator and its hardware and software structure. As test results with the power system simulator, we verify the basic operation of the prototype TCSC simulator. From these results, this paper arrives at the possibility of real-time simulation for FACTS devices on an analog power system simulator. Hereafter, a study will be performed concerning the multilayer control system with multi-processor platform and the combination control of FACTS devices (TCSC, HVDC, UPFC etc.) on power simulators.

Acknowledgements

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References

[1] Narain G. Hingorani and Laszlo Gyugyi, "Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems(Book)", *IEEE Press*, 2000

[2] "The research strategy for FACTS", *The final report, The MOST of Korea*, 1995

[3] "Development of 1MVA UPFC", *The final report, The MOST of Korea*, 1999

[4] "Development of Power Transfer Capability Enhancement Technology of Transmission and Distribution System by FACTS", *The first stage report, The MOST of Korea*, 1998

[5] "Development of the multi-mass turbine-generator simulator and TCSC controller", *The final report, KRCI*, 2002

[6] Jin-Hong JEON, etc. "Development of 20kVA TCSC

simulator", *KIPE. PEAC 2003*, pp158-151, 2003
[7] Jean J. Labrosse, "The Real-Time Kernal(Book)", *Miller Freeman*, 1999

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