Fabrication of Thin Film Transistor Using Ferroelectrics

Chang-Wu Hur, Jung-Tae Kim, *Member, KIMICS*

Abstract—The a-Si:H TFT using ferroelectric of $SrTiO_3$ as a gate insulator is fabricated on glass. Dielectric characteristics of ferroelectric are superior to SiO_2 and Si_3N_4. Ferroelctric increases on-current, decreases threshold voltage of TFT and also improves breakdown characteristics. The a-SiN:H has optical band gap of 2.61 eV, refractive index of 1.8~2.0 and resistivity of 10^{13}~10^{15} Ωcm, respectively. Insulating characteristics of ferroelectrics are excellent because dielectric constant of ferroelectric is about 60~100 and breakdown strength is over 1MV/cm. TFT using ferroelectric has channel length of 8~20 μm and channel width of 80~200 μm. And it shows that drain current is 3.4μA at 20 gate voltage, I_{on}/I_{off} is a ratio of 10^5 ~ 10^8 and V_{th} is 4~5 volts, respectively. In the case of TFT without ferroelectric, it indicates that the drain current is 1.5 μA at 20 gate voltage and V_{th} is 5~6 volts. With the improvement of the ferroelectric thin film properties, the performance of TFT using this ferroelectric has advanced as a gate insulator fabrication technology is realized.

Index Terms—TFT, Febrroelectrics

I. INTRODUCTION

Today, amorphous silicon is widely used in optical to electrical conversion device and wide area film device. Especially, it is used such as a switching device for active matrix LCD, contact image sensor for a-Si:H TFT and Fax, and a-Si:H solar cell. Usually, amorphous silicon TFT uses a-SiN:H as a gate insulator. Induced dielectric constant of a-SiN:H is 7.5. To increase a driving current of TFT, an insulator with a large of induced dielectric constant is needed. Recently, much works have advanced on TFT gate insulating layer. The commonly used materials are Ta_2O_5, MoTaO, Cr_2O_3 and Al_2O_3. These materials are used as base layer. Ferroelectric thin film is suitable as gate insulator because of a large breakdown electricity and induced dielectric constant. In this paper, we have fabricated a-Si:H TFT using gate insulator with ferrodielectric and compare their electrical characteristics with gate insulator a-SiN:H TFT used as commonly.

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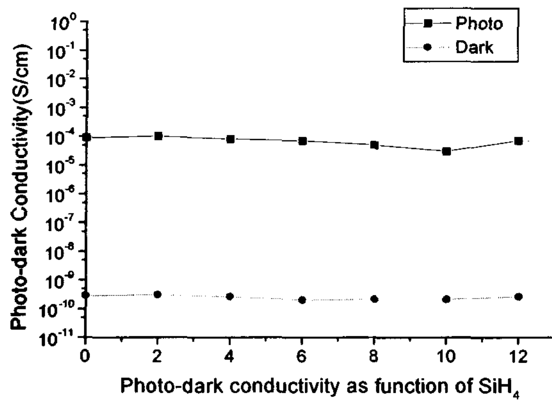
II. FABRICATION AND THEIR CHARACTERISTICS BETWEEN A-SI:H FILM AND FERROELECTRIC THIN FILM

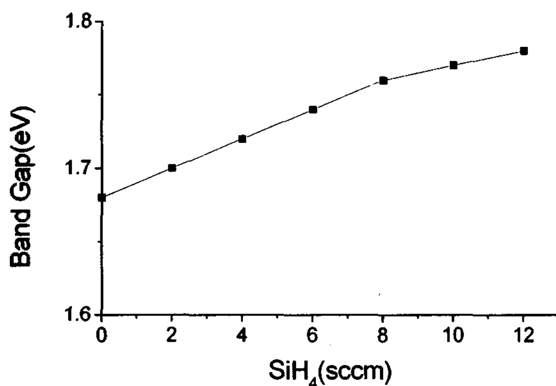
Amorphous silicon is deposited using plasma enhanced chemical vapor deposition (PECVD). At this time, electrical and optical characteristics of amorphous silicon such as conductivity, optical band gap and deposition rate are changed under deposition condition such as SiH_4, flux, chamber pressure, RF power and substrate temperature. Figure 1 shows the characteristics of experimental results according to amorphous deposition condition. From the results shown in figure 1, photo and dark conductivity are diminished according to SiH_4 flux, dark conductivity is changed 10^{-9}~10^{-11}(S/cm), in the case of photo conductivity is varied range from 10^{-4} to 10^{-6} (S/cm). Also, optical band gap shows 1.7~1.8eV, as a flux of SiH_4 is increased, it is deposited from 1.0 to 6.9 (Å/sec).

As shown in figure 1, we can estimate the trade-off relation between conductivity and optical band gap according to a flux of SiH_4 and control the optical band gap by adjusting a flux of SiH_4. But, the change of conductivity and optical band gap is little according to chamber pressure condition. The deposition rate is ranged from 1.0 to 3.0 (Å/sec). Also, the change of electrical and optical characteristics is a little according to RF power. Figure 2 shows the IR spectrum result. It represents a relation between Si of hydrogenated amorphous silicon film and bonding of H. Frequency of fundamental infrared absorption modes depends on a mass of oscillation dipole and amount of bond between elements including dipole. The a-Si:H film shows a type of vibration mode, it shows SiH_4 stretching mode at wave number 2000 cm^{-1}. Also, it represents a rocking mode at wave number 635 cm^{-1}. The bond represented at weaker bond range 800~900 cm^{-1} depends on the vibrational mode of SiH_2. Therefore, the fabricated a-SiH film in this experimental setup shows that Si-H bonding of stretching/rocking mode exists. The gate insulator layer and a-SiN:H film of passivation film are fabricated using PECVD by mixing SiH_4 gas and NH_3 gas. Figure 3 shows optical bandgap of a-SiN:H. Etching rate of a-SiN:H increases and refraction diminishes as NH_3/SiH_4 increases. Also, their characteristics are not related with RF power. The E_{opt} value is around 2.4 eV.

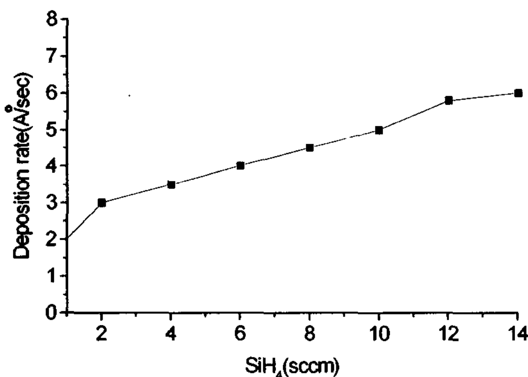
Ferroelectrics ($SrTiO_3$) film is fabricated by E-beam evaporator. The used ferroelectrics target forms ceramic type with high pressed PELLE. The ferroelectric thin films are evaporated by E-beam evaporator. Dielectric constant of ferroelectric thin film is 60 ~ 100 and has high value compared with another insulator. It has a high breakdown field about 1 MV and excellent characteristics as an insulator.



(a) Photo-dark current as function of thickness of AL_2O_3



(b) Band gap as function of SiH_4



(c) Deposition rate as function of SiH_4

Fig. 1 Electrical and optical characteristics of a-Si:H (a-Si:H properties as SiH_4 flow rate)

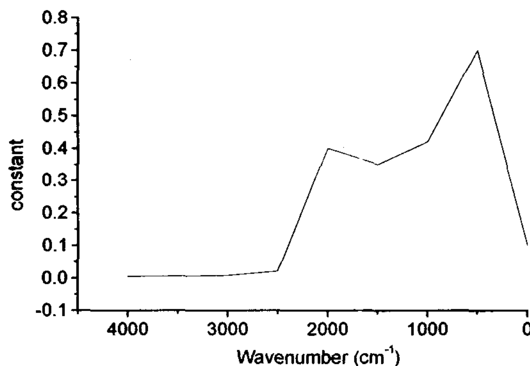


Fig. 2 FTIR characteristics of a-Si:H

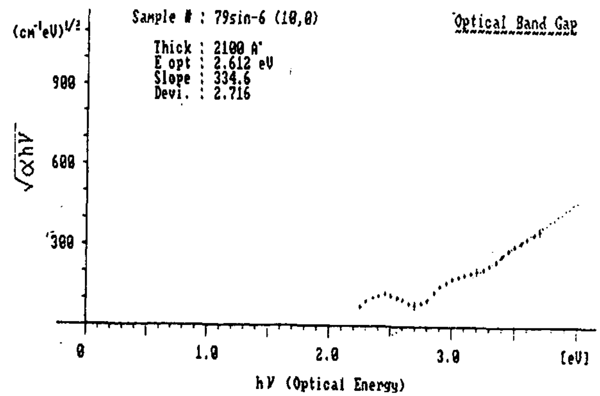


Fig. 3 Optical Band Gap of a-SiN:H

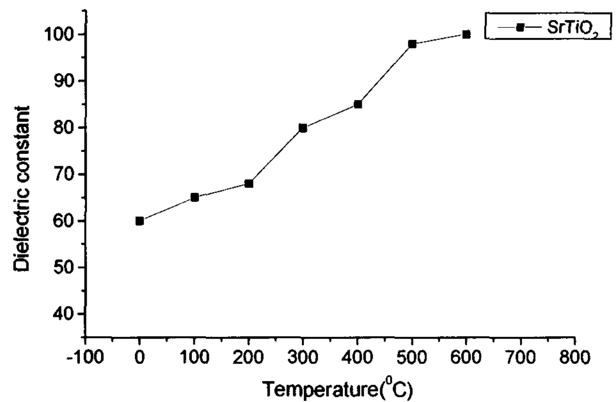


Fig 4. Dielectric properties of ferroelectrics

III. CHARACTERISTICS AND STRUCTURE OF THIN FILM TRANSISTOR

Figure 5 shows a cross-section of process for thin film transistor fabricated in this experimental setup. The gate electrode is formed by patterning with length of 8 μm~16 μm and width of 80~200 μm after depositing with gate electrode (Cr) 1000 Å under corning 7059 glass substrate. We have fabricated a-SiN:H, a-Si:H and n^+a-Si:H samples on gate electrode in sequence and ferroelectric ($SrTiO_3$), a-Si:H and n^+a-Si:H samples, respectively. The thickness of these thin films is formed with $SrTiO_3$ (2000 Å), a-SiN:H (3000 Å), a-Si:H (2000 Å) and n^+a-Si:H (500 Å). We have used a RIE (Reactive Ion Etching) method to etch after forming a-Si:H pattern of channel layer. RIE equipment is used RI mode of PECVD. After hole pattern is formed, a-Si:N:H is conducted RIE and the used gas is used by mixing CHF_3 and O_3. Ferroelectric ($SrTiO_3$) is mixed with HF:DI at a rate of 1:5 and etched by dipping with 17 seconds. To form a source drain electrode, the film is patterned after depositioning 4000 Å of Al by E-beam evaporator. Finally, n^+a-Si:H is conducted by RIE using CF + O_2 and gas for S/D metal pattern. To compensate a damage by RIE process, the n^+a-Si:H is annealed at temperature 200°C in vacuum state. To test a characteristics of fabricated sample, we have gained an I-V, V_{th} and I_{on}/I_{off} characteristics by using probe station and HP4145B parameter analyzer.

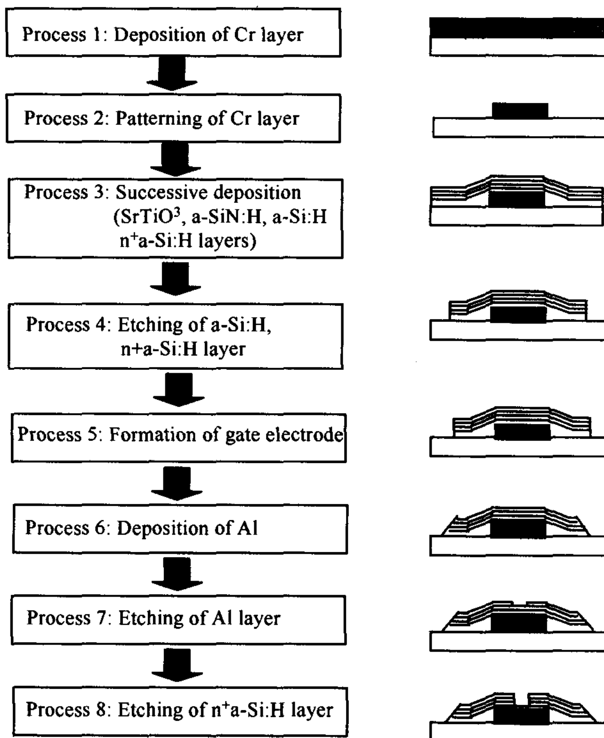
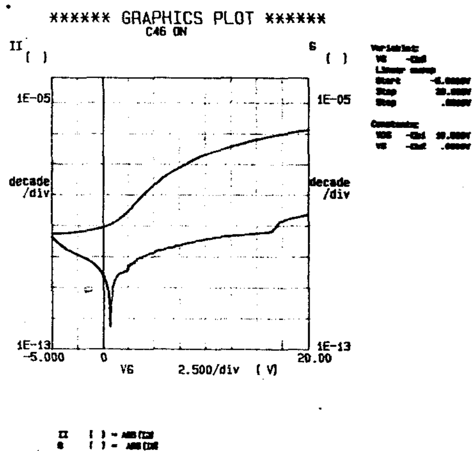
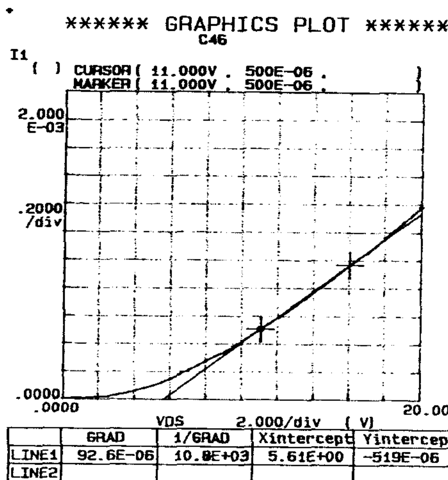


Fig. 5 Fabrication process of a-Si:H TFT



(a) I_{on}/I_{off} ratio



(b) Threshold voltage (V_{th})

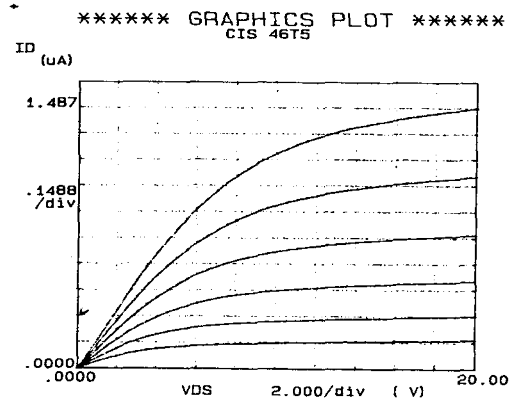
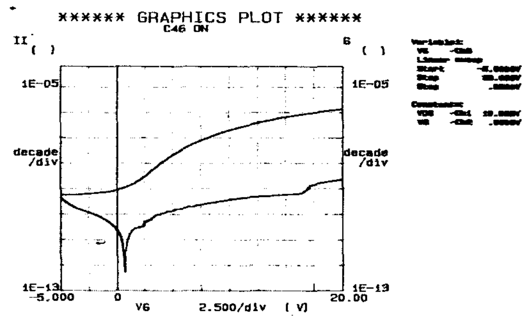
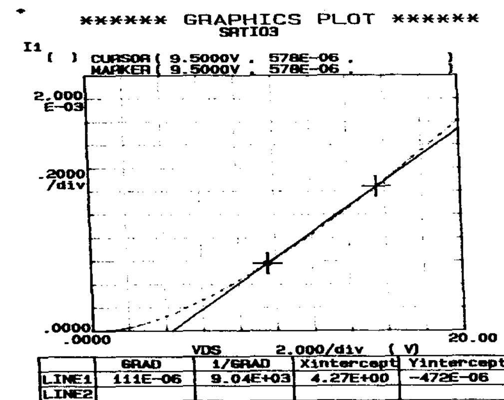


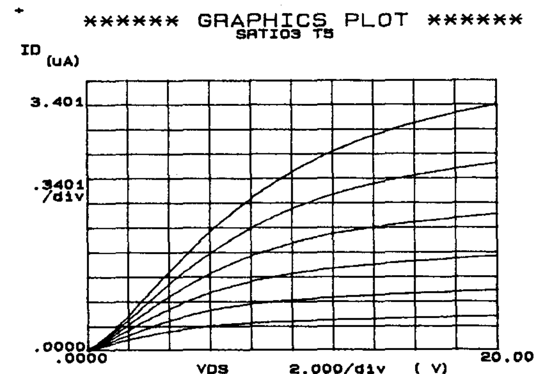
Fig. 6 Electrical Characteristics of a Si:H TFT Without Ferroelectric



(a) I_{on}/I_{off} ratio



(b) Threshold voltage (V_{th})



(c) I-V curve

Fig. 7 Electrical Characteristics of a Si:H TFT With Ferroelectric

As shown in the figure 6, we have been annealing for 1 hour at a temperature 200 °C to compensate damage by RIE process. To measure the electrical characteristics of the fabricated samples, we obtained characteristics of I-V, V_{th} and I_{on}/I_{off} by using probe station and 4145A parameter measurement equipment. As shown in figure 6, the saturation current at gate voltage 20 Volts without having ferroelectric TFT is 1.4 μA, I_{on}/I_{off} is 10^3 and V_{th} is 5.6 volts. In the case of TFT with ferroelectric gate insulator layer as shown in figure 7, saturation current at gate voltage 20 volts is 3.4μA, V_{th} is 4.5 volts and I_{on}/I_{off} gives a values range from 10^5 to 10^6. We have estimated that the leakage current of TFT with ferroelctric layer is smaller than that of without ferroelctric layer. That is to say, the V_{th} of the TFT with two layers using ferroelecric and a-SiN:H compared with TFT of gate insulator with a-SiN:H layer shows a small value and has 1 volts. I_{on}/I_{off} has 10^2~10^3 order value. Its I-V current has a 1.5μA times in the same gate and drain volts. From the results, we can estimate that the ferroelectric layers employing two layers gate insulator have a higher insulator characteristics. It enhanced good electrical characteristics. Also, the leakage current can be diminished by using two layers insulator.

IV. CONCLUSIONS

From the experimental results, the TFT with ferroelectric has a higher value of I_{on}/I_{off} compared with TFT having a gate insulator employing a-SiN:H. In the case of I_{off} current, leakage current between source and gate by using two layers gate insulator ($SrTiO_2$/a-SiN:H) reduces, pin hole employing gate insulator with one layer is more larger than two layer gate insulator. The probability of generation of pin-hole by using two layer is more smaller. Also, I_{on} current increases as dielectric constant of gate insulator increases. This effect gives the increase of I_{on}/I_{off}. As dielectric constant increases, V_{th} get smaller 1 volts value. The channel is formed in small gate voltage. From the I-V curve, we can estimate that drain current of TFT with $SrTiO_2$ at same gate voltage increases over 1.5 μA. And, leakage current between gate and source is much smaller. Under the voltage stress condition, TFT with ferroelectric compared to thin film has no influence on the voltage stress condition. From the results, we can estimate that TFT with ferroelectric has no interface trap. These phenomena give good results. Ferroelectric thin film can be applicable to TFT application such as HDTV display device.

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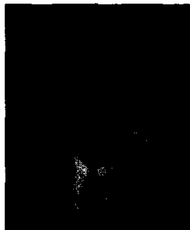

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