Fabrication and Characterization of Silicon Probe Tip for Vertical Probe Card Using MEMS Technology

Young-Min Kim*, In-Sik Yu and Jong-Hyun Lee***

Abstract - This paper presents a silicon probe tip for vertical probe card application. The silicon probe tip was fabricated using MEMS technology such as porous silicon micromachining and deep-RIE (reactive ion etching). The thickness of the silicon epitaxial layers was 5 μm and 7 μm, respectively. The width and length were 40 μm and 600 μm, respectively. The probe structure was a multilayered structure and was composed of Au/Ni-Cr/Si_3N_4/n-epi layers. The height of the curled probe tip was measured as a function of the annealing temperature and time. Resistance characteristics of the probe tip were measured using a touchdown test.

Keywords: annealing process, deep-RIE, porous silicon micromachining, probe tip, thermal expansion coefficient

1. Introduction

As very large scale integration (VLSI) technology progresses toward higher levels of integration and higher operating speeds, semiconductor device dimensions shrink and complexity increases because of decreasing pad size and increasing numbers of pads [1,2]. The probe card is used to test the performance of integrated-circuit (IC) chips in wafer-level before they are packaged. The traditional probe card, which is commonly used in testing IC chips, is composed of needles [3]. However, although high density and high pin count probing are required in wafer level testing, traditional probe cards with needles/wire have limitations due to the difficulty of manufacturing probe cards and the parasitic capacitance and inductance that is induced between needles in high operating speed tests [4,5]. Microelectromechanical system (MEMS) technology using silicon wafers has recently been developed for the purpose of high density, fine pitch, and high pin count as the substitute of traditional probing.

In this paper we present an array of silicon probe tips for probe card applications. One type of probe tip was fabricated using a silicon wafer and MEMS technologies in order to solve fine pitch limitations and silicon process related problems [6,7]. A probe tip consisting of array cantilever beams of various thicknesses and lengths, was also fabricated on a silicon substrate of $n/n^+/n$ structure [8,9]. The three dimensional structure of the probe tips were fabricated using a porous silicon micromachining process. For the purpose of IC pad probing, the cantilever type probe tip required optimal radius curvature. The height of the curled probe tip was measured as a function of annealing temperature and time. The electrical and mechanical properties of the fabricated probe tips are investigated.

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2. Design and Fabrication

2.1 Design of silicon probe tip

Fig. 1 shows a schematic diagram of a three dimensional silicon probe tip. The cantilever type probe tip was designed with a length of 600 μm and a width of 40 μm. The probe structure is a multilayered structure and consists of Au/Ni-Cr/Si_3N_4/n-epi layers. The oxidized surface of the IC chip pad was broken down electrically using the mechanical scrubbing motion of the probe tip.

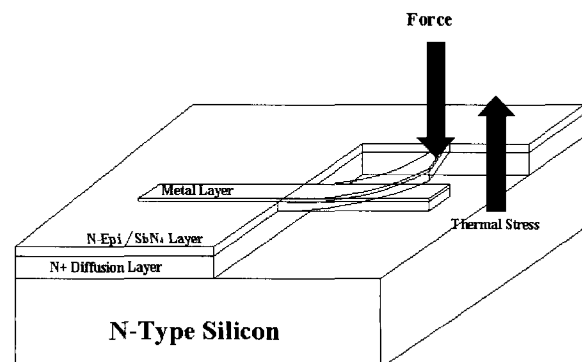


Fig. 1 Schematic of the silicon probe tip.

Probe tips curl up as a result of surface tension and the difference in the thermal expansion coefficients between films on the cantilever beam. The probe tip of optimal radius curvature can obtain as a function of the annealing temperature, time, and thickness of the free standing cantilever beam.

2.2 Porous silicon micromachining

Porous silicon which forms on the surface of crystalline silicon substrate in hydrofluoric acid (HF) under an appropriate anodic bias was first observed by Uhlir in 1956. Porous silicon can be formed by electrochemical etching in diluted HF. The anodization generates an array of holes or pores perpendicular to the surface of the substrate. Porosity, etch depth, and pore size vary depending on current density, hydrofluoric acid (HF) concentration, silicon type, and silicon resistivity.

In this paper, a micromachining process was presented for the fabrication of three-dimensional microstructures [10,11]. This is a simple process to form porous silicon using an anodic reaction. Fig. 2 presents the anodic reaction system to form a PSL (porous silicon layer).

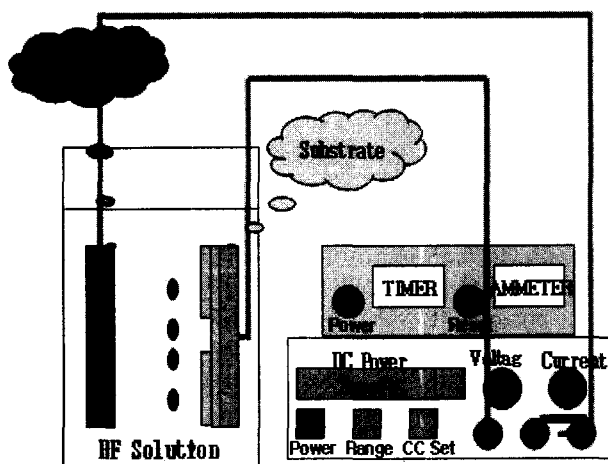


Fig. 2. System of anodic reaction

The PSL was obtained by the anodization process. It began with the diffusion to make a highly doped n^+ layer over an n-type substrate and the sequential growth of a lightly doped n-epitaxial layer. A PSL was formed on an n^+ diffused layer by the anodization process. The anodic reaction was performed in aqueous HF solution and constant current density. In order to obtain uniform PSL, the stirring rate was kept constant at 400 rpm. The porosity of the PSL increases with the decrease of HF concentration and increase of current density.

Fig. 3 shows a surface scanning electron microscopy (SEM) image of a PSL following anodic reaction. The anodic reaction was performed in aqueous HF (HF: H_2O=3:1) solution for 20 min at room temperature by applying a constant current density of 10mA/cm^2. The depth of the PSL was 20 μm.

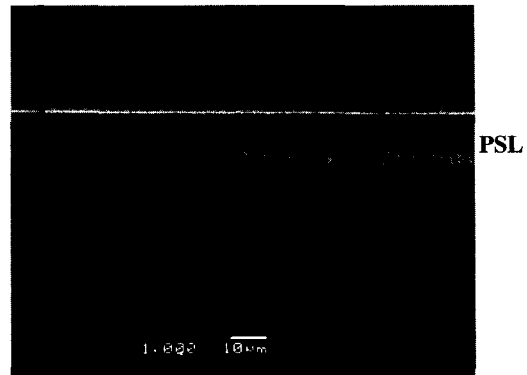


Fig. 3 SEM image of porous silicon layer

Fig. 4 shows a SEM image of three-dimensional microstructure. The structure of silicon wafer was n/n^+/n-sub structure. The thickness of the n^+ diffusion layer and n-epitaxial layer was 20 μm and 5 μm, respectively. The PSL was performed by the anodic reaction and etched by NaOH solution. The cavity depth between the probe tip and substrate was controlled by the anodic reaction time and the thickness of the n^+ diffused layer.

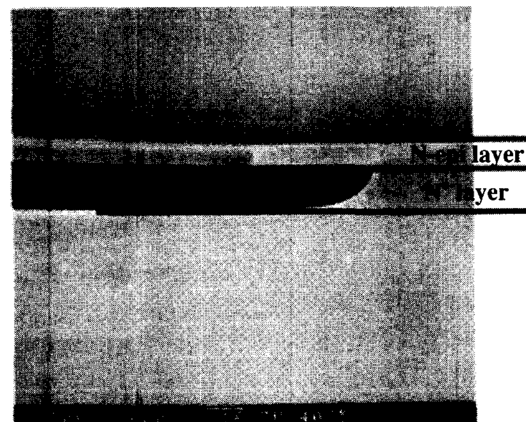


Fig. 4 SEM image of microstructure after anodic reaction

Since the highly doped n^+ diffused layer is much higher than that in the n-type substrate, the anodic reaction only occurs in the n^+ diffusion layer. Since the n+ region is selectively diffused on the n-type silicon substrate, porous silicon is only formed there while the lightly doped epitaxial silicon layer and substrate provide etch stops.

2.3 Fabrication of silicon probe tip

The probe tips were fabricated using a porous silicon micromachining, RIE, and silicon deep-RIE technique. The fabrication process of the probe tips is shown in Fig. 5.

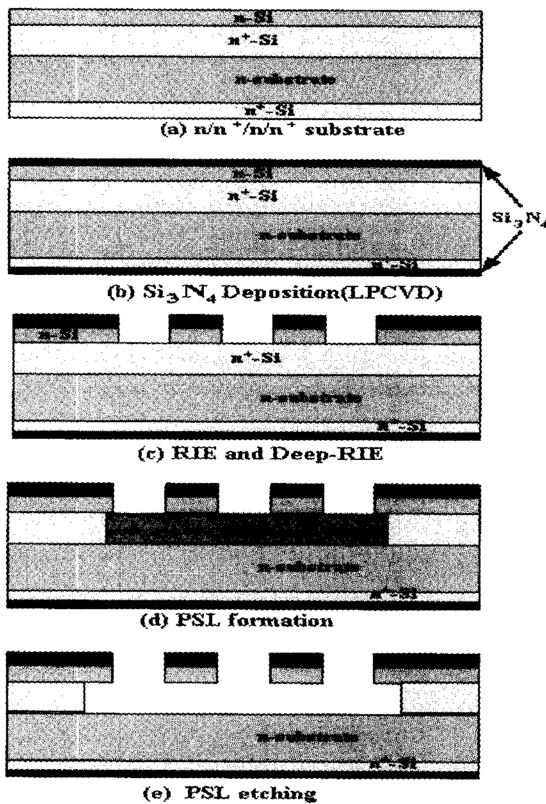


Fig. 5 Probe tip fabrication process.

The starting material was a double-sided polished (100) n-type silicon wafer. First, fabrication began with diffusion to create a highly doped n^+ layer over an n-type substrate and subsequently lightly doped n-epitaxial layer. The highly doped n^+ layer was used as a sacrificial layer in order to form the three-dimensional probe tips of cantilever type using an isotropic anodic reaction. The doping concentration of the n^+ diffusion layer was higher than 1×10^{19} /cm^3, high enough to form porous silicon. The doping concentration of the n-type epitaxial layer was 1×10^{15} /cm^3. The n^+ layer thickness has 20 μm and the n-epitaxial layer has a thickness of 5 μm and 7 μm, respectively (Fig. 5a). Then a silicon nitride (Si_3N_4) of 1,500 Å thick was deposited by low pressure chemical vapor deposition (LPCVD) on both sides of the wafer (Fig. 5b).

First, the Au (2,000Å)/Ni-Cr (2,000Å) were deposited on the Si_3N_4. Further Ni-Cr was used as a thin film to create thermal stress for deflection of the probe tip. Then aluminum was deposited by evaporation. The metal lines were patterned by photolithography. Next, probe tips were patterned and deep-RIE was then performed (Fig. 5c). A PSL was formed on an n^+ diffused layer by anodization. The anodic reaction was carried out in aqueous HF ($HF:H_2O$ = 3:1) solution for 25 min at room temperature by applying a constant voltage of 0.7 V to the wafer. A current density of 10 mA/cm^2 was used (Fig. 5d). The PSL was removed in a 5 wt.% NaOH solution (Fig. 5e). Since the doping concentration in the n^+ diffused layer is much higher than that in the n-epitaxial layer and substrate, the anodic reaction only occurs in the n^+ diffused layer. The formation of three-dimensional microstructure was controlled by the n^+ diffusion region and thickness of n-epitaxial layer. Finally, to obtain even more significantly curled probe tips, we performed an annealing process.

3. Results and Discussion

The multiarray silicon probe tip, to be applied in a probe card, was successfully fabricated using MEMS technology. Fig. 6 shows the cross-sectional SEM image of a silicon probe tip that was performed by the fabrication process (Fig. 5). The SEM image displays the silicon probe tips prior to the annealing process.

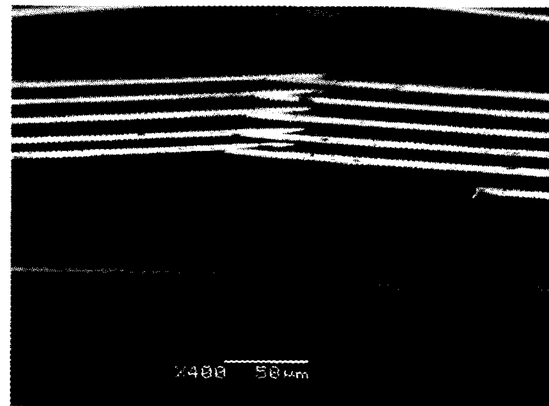


Fig. 6 SEM image of probe tip prior to annealing process.

3.1 Characterization of silicon probe tip

The height of the curled probe tips was measured as a function of the annealing temperature and time. The thickness of the silicon epitaxial layers was 5 μm and 7 μm, respectively. The width and length of the probe tips were 40 μm and 600 μm, respectively. Fig. 7 shows the height of the probe tip at various annealing times. The annealing temperature was fixed at 500℃.

Curled probe tips are obtained at high temperatures using the surface tension difference between the films on the cantilevers and the thermal expansion coefficient. In the case of a high annealing time over 20 min, the height of the curled probe tips was reduced as the stress between the films was relaxed.

Fig. 8 shows the height of the probe tips at various annealing temperatures. The annealing time was fixed at 20 min. The height of a curled probe tip is an important factor that relates to the force required to make contact with the pad on IC chips.

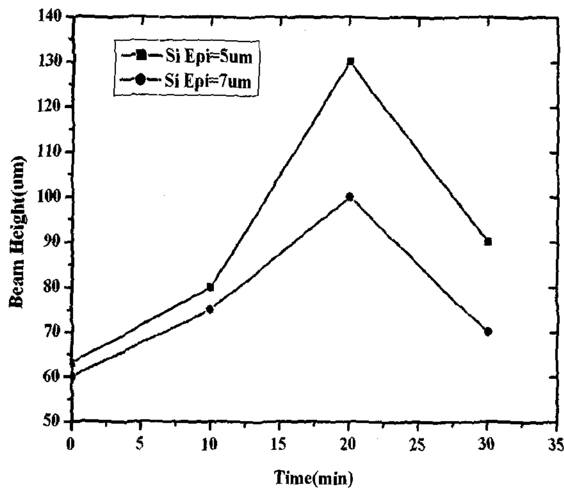


Fig. 7 Height of probe tip versus annealing time

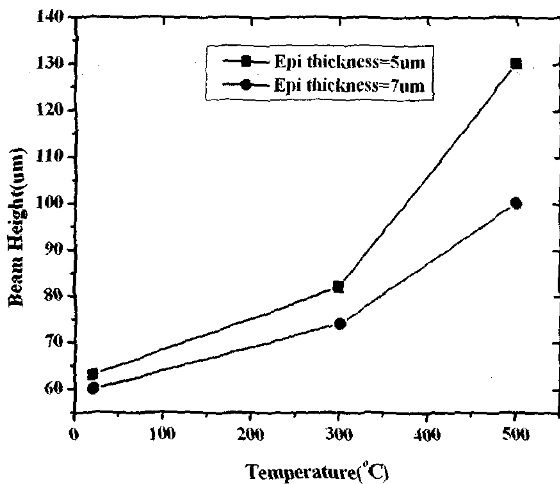


Fig. 8 Height of probe tip versus annealing temperature

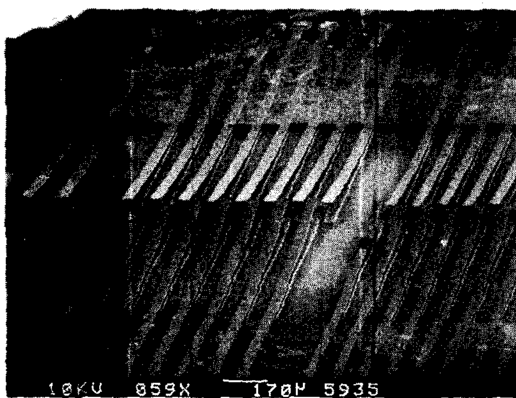


Fig. 9 SEM image of probe tip after annealing

To obtain even more significantly curled probe tips, the wafer was annealed in nitrogen ambient for 20 min at 500℃.

Fig. 9 shows the SEM image of a curled probe tip following the annealing process. The annealing process was performed for 20 min at 500°C. The result shows that a deflection height over 130 μm can be achieved for silicon epitaxial layer thickness of 5 μm.

Fig. 10 illustrates the contact resistance between the Au pad and probe tip versus the number of touchdowns. The thickness of the silicon epitaxial layers was 5 μm. The width and length of probe tips were 40 μm and 600 μm, respectively. The maximum height of probe tips was 130 μm.

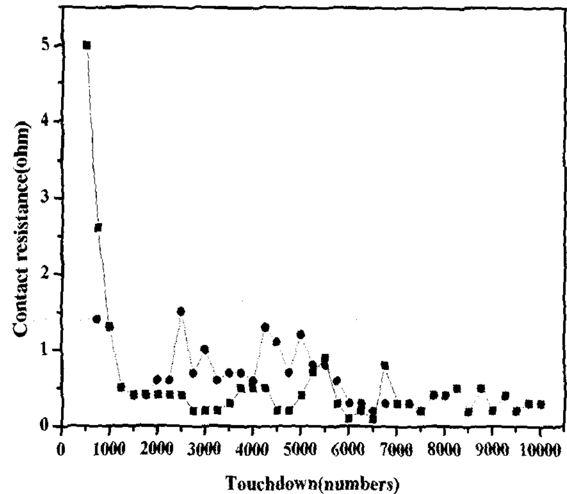


Fig. 10 Contact resistance versus touchdown number

As a result, the contact resistance of the probe tips was measured to be below 1 Ω and there was no change of contact resistance after 20,000 contacts. Also there was no peel-off of the metal on the top of the probe tips. The silicon epitaxial layer of 7 μm obtained identical results.

Individual probe tips were measured for resistance as a function of overdrive. The overdrive is the moved distance from the point of initial contact with an Au pad. All of the experiments were carried out on a clean bench at room temperature. Fig. 11 shows the resistance between the Au

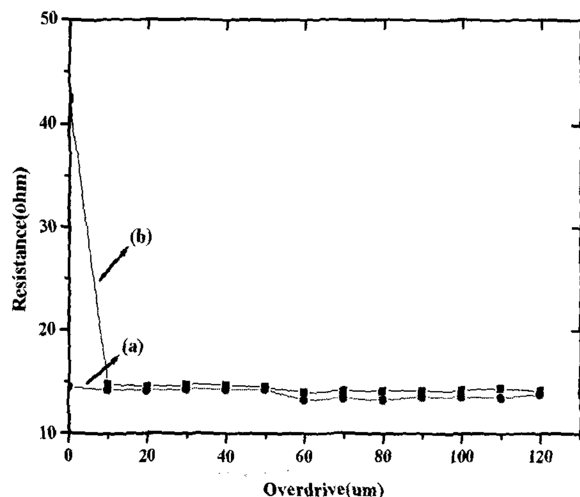


Fig. 11 Resistance characteristics versus overdrive

pad and probe tip versus overdrive force. Fig. 11(a) indicates the result that only measured resistance after Au evaporation. Fig. 11(b) displays the result of measurement using Au pad after the passage of a given time. We observed that the resistance falls to below 15 ohm after about 60 μm of overdrive and maintains constant with further overdrive. Overdrive is required to reduce resistance to an acceptable level during testing.

4. Conclusions

We proposed multiarray silicon probe tips for vertical probe card application. They were fabricated using MEMS technology and deep-RIE process. The thickness of the silicon epitaxial layers was 5 μm and 7 μm, respectively. The width and length of the probe tips were 40 μm and 600 μm, respectively. The maximum height of the probe' tip was measured at the condition of annealing for 20min at 500°C. We can sufficiently control the height and curvature of curled probe tips. Probe tips are curled up as a result of surface tension and difference in the thermal expansion coefficients between the thin films on the probe tips. The contact resistance of the probe tips was below 1Ω and there was no change of resistance over 20,000 contacts. We performed a simulation concerning the deflection of a beam as a function of input force and considered mechanical strength and curvature of the probe tips to endure scratching by the surface of the metal contact pad. The fabrication process used in this paper was very simple and highly reproducible. It is expected that this fabrication process can be applied to probe cards of fine pitch and multi-array probe tips.

References

[1] Shin'ichiro Asai, Kazuo Kato, Noriaki Nakazaki, and Yukihiko Nakajima, "Probe card with probe pins grown by the vapor-liquid-solid (VLS) method", *IEEE Trans. Comp., Package. Manufat. Technol.*, part A. vol. 19, pp. 258-267,1996.

[2] C. Barsotti, S.Tremaine. and M. Bonham, "Very high density probing", *in Proceedings of the IEEE International Testing Conference*, pp. 608-614, 1988.

[3] S. Maekawa, M. Takemoto, Y. Kashiba, Y. Deguchi, K. Miki, and T. Nagata, "Highly Reliable Probe Card for Wafer Testing", *Electronic Components and Technology Conference*, pp. 1152-1156, 2000.

[4] Y. Zhang, Y. Whzng, R. B. Marcus, "Thermally actuated microprobes for a new wafer probe card," *IEEE Journal of Microelectromechanical Systems*, vol. 8, pp. 43-49, 1999.

[5] S. Hong, K. Lee, J. C. Bravman, "Design and fabrication of a monolithic high-density probe card for high-frequency on-wafer testing," *in Technical Digest., Electron Devices Meeting*, pp. 289-292, 1989

[6] B. H. Kim, S. J. Park, B. L. Lee, J. H. Lee, B. G. Min, S. D. Choi, D. I. Cho, K. J. Chun, "A novel MEMS silicon probe card," *in the 14th IEEE International Conference on MEMS*, pp. 368-371, 2002

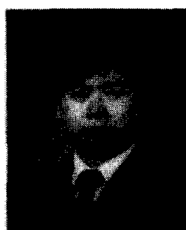
[7] K. Kataoka, S. Kawamura, T. Itoh, T. Suga, "Low contact-force and compliant MEMS probe card utilizing fritting contact," *in the Fifteenth IEEE International Conference on MEMS*, pp. 364-367, 2002.

[8] Y. M. Kim, D. S. Eun, S. G. Park, C. S. Jo, J. H. Lee, "Characteristics of Cantilever Beam Fabricated by Porous Silicon Micromachining for Flow Sensor Application", *IEEE SENSORS 2003*, p.641-642, 2003.

[9] Y. M. Kim, C. T. Seo, D. S. Eun, S. G.. Park, C. S. Jo, J. H. Lee, "Characteristics of Cantilever Beam Fabricated by Porous Silicon Micromachining for Flow Sensor Application", *Proceedings of IEEE International Conference on SENSORS 2003*, p.642-646, 2003.

[10] Y. M. Kim, K. Y. Noh, J. Y. Park, Y. D. Kim, I. S. Yu, C. S. Cho, J. H. Lee, "Fabrication of Oxidized Porous Silicon(OPS) Air-Brdige for RF Application Using Micromachining Technology", *Journal of the Korean Physical Socity*, p.S268-S270, 2001.

[11] Y. D. Kim, J. H. Sim, J. W. Nam, and J. H. Lee, "Fabrication of a Silicon Micro-Probe for Vertical Probe Card Application", *Japanese Journal of Applied Physics*, pp. 7070-7073, 1998.



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