A CMOS Bandgap Reference Voltage Generator for a CMOS Active Pixel Sensor Imager

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This paper proposes a new bandgap reference (BGR) circuit which takes advantage of a cascode current mirror biasing to reduce the V_{ref} variation, and sizing technique, which utilizes two related ratio numbers k and N, to reduce the PNP BJT area. The proposed BGR is designed and fabricated on a test chip with a goal to provide a reference voltage to the 10 bit A/D (4-4-4 pipeline architecture) converter of the CMOS Active Pixel Sensor (APS) imager to be used in X-ray imaging. The basic temperature variation effect on V_{ref} of the BGR has a maximum delta of 6 mV over the temperature range of 25 °C to 70 °C. To verify that the proposed BGR has radiation hardness for the X-ray imaging application, total ionization dose (TID) effect under Co-60 exposure conditions has been evaluated. The measured V_{ref} variation under the radiation condition has a maximum delta of 33 mV over the range of 0 krad to 100 krad. For the given voltage, temperature, and radiation, the BGR has been satisfied well within the requirement of the target 10 bit A/D converter.

Keywords : Bandgap reference(BGR), CMOS APS imager, Cascode current mirror, Total ionization dose(TID)

1. INTRODUCTION

The bandgap reference (BGR) circuit is one of the most popular reference voltage generators used in high precision comparators, A/D or D/A converters, and many other analog circuits to support a stable reference voltage and/or current. So the BGR is required to have good immunity against any supply voltage fluctuations or temperature variations. In addition, to be incorporated into a specific CMOS Active Pixel Sensor (APS) imager targeting an application field of X-ray imaging, the immunity of the BGR under radiation environment is also important.

Related to the BGR, several unique solutions have been suggested[1-3] and their experiment results under severe radiation condition have also been reported[4].

In this paper, another circuit solution is proposed and the test results of voltage characteristic, temperature characteristic, and radiation response of the proposed BGR, targeting a digital X-ray imaging application, are reported. The main focus of this paper is to evaluate the performance of the newly proposed BGR under voltage, temperature variation, and radiation condition, but not to analyze the evaluation results theoretically.

For the evaluation, the proposed BGR is actually designed and fabricated on a test chip. To set the design target, the following assumptions were made; The BGR will supply voltage of 2.5 V ±10 % for the A/D converter of a 10 bit A/D (4-4-4 pipeline architecture) which will be embedded in a CMOS APS imager for X-ray imaging.

2. PROPOSED BGR CIRCUIT

The proposed BGR shown in Fig. 1 consists of a differential op-amp, a bias circuit, a cascode current mirror, a level shifter, PMOS transistors with optimally controlled sizes, two PNP bipolar transistors, and resistors.

The cascode current mirror, which has wide swing characteristic and immunity against threshold variation, is used to reduce the variation of V_{ref} and temperature (PVT). The level shifter allows the proposed BGR to be fabricated under the processes providing only normal threshold voltage for MOS transistor. If low-V_{TH} MOS were to be available, this level shifter may be removed. The optimally controlled size of the PMOS transistors and its merits are discussed in detail below.

The ratio relationship between various components in the circuit is as follows; R3 = kR1, MP1a = MP1b = MP3a = MP3b = kWp and MP2a = MP2b = Wp. And the voltages V_a and V_b are controlled to be the same level by the operation of the level shifter and the differential op-amp. The current I is $I_1 + I_2$, where I_1 and I_2 satisfy the following equations,

$$I_1 = \frac{\Delta V_{BE}}{R_2}, \quad I_2 = \frac{V_{BE1}}{R_3} \tag{1}$$

where ΔV_{BE} is the voltage difference between the two BJTs Q_1 and Q_2, and is expressed as,

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln(kN) \tag{2}$$

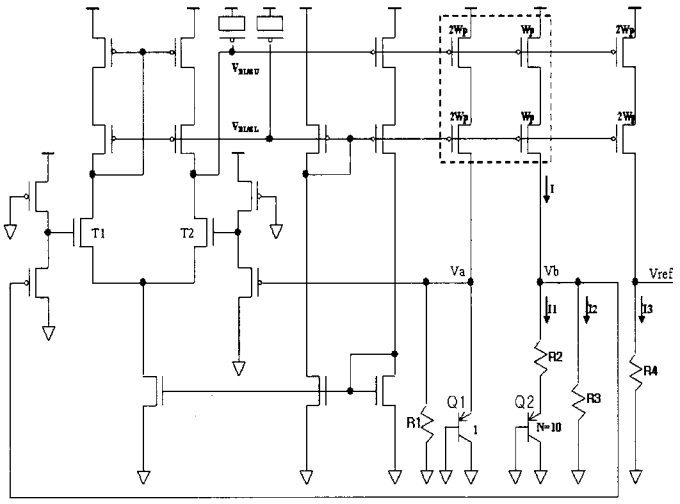


Fig. 1. Diagram of the proposed BGR circuit.

In equation (2), V_T, k and N are the thermal voltage, the number of PMOS transistors, and the area of BJT emitter.

Here, the current I is mirrored to I_3 and therefore, the output voltage of the proposed BGR, V_{ref}, becomes

$$V_{ref} = kIR_4 = \left(\frac{V_{BE1}}{R_1} + \frac{V_T k \ln(kN)}{R_2}\right)R_4 \tag{3}$$

If k is chosen to be 2 and appropriate resistance values are used, N is calculated to be 5. Compared to other BGRs[1,2] of which the value of N is 100, the proposed BGR needs only 1/20 of the area for the PNP BJT. Depending on the selection of the k value, N can be varied to satisfy the needs.

Generally a BGR generates a voltage which is independent of temperature by summing two voltages where one is proportional to absolute temperature (PTAT) and the other is complementary to absolute temperature (CTAT). In the proposed BGR, the PTAT is the voltage difference between two BJTs, Q_1 and Q_2, and the CTAT is V_{BE1}. The BGR circuit does not operate properly if V_{BIASU} and V_{BIASL} follow the V_{DD} voltage because the bias current would become zero. This situation may happen during power-up by capacitive coupling between these nodes and V_{DD}.

That is the reason a start-up circuit is needed for the proposed BGR as shown in Fig. 2. During power-up, if V_{BIASU} of the circuit is larger than (V_{DD} – $|V_{TP}|$), the PMOS transistor, MP1, is OFF and the NMOS transistor, MN1, becomes ON as the gate voltage of the MN1 is raised along with V_{DD}. Once the MN1 is turned on, the V_{BIASU} is discharged to ground. The V_{BIASL} acts similarly and the V_{BIASU} and the V_{BIASL} of the BGR guarantees proper bias operation.

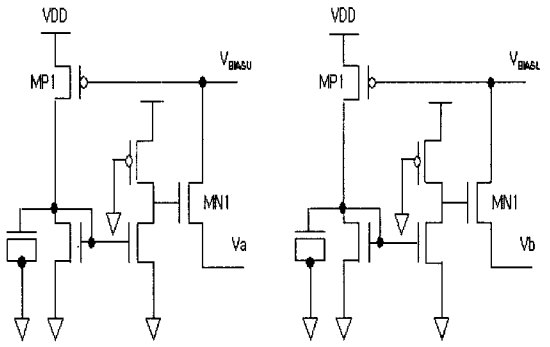


Fig. 2. Start-up circuit for the proposed BGR.

3. EVALUATION RESULTS

3.1 Test chip and V_{ref} distribution

The proposed BGR is fabricated using the Hynix 0.18 μm triple-well CMOS logic process that provides only normal V_{TH} transistor. Fig. 3 shows the photograph of the proposed BGR test chip.

The distribution of the measured V_{ref} with 120 samples is shown in Fig. 4. The measurement is taken at the V_{DD} of 2.5 V and room temperature. The average V_{ref} was 759 mV with σ = 25.4 mV. The use of a resistive material with narrow width accounts for the wide distribution, since a narrower design is more affected by the process variation.

Fig. 3. Photograph of the test chip.

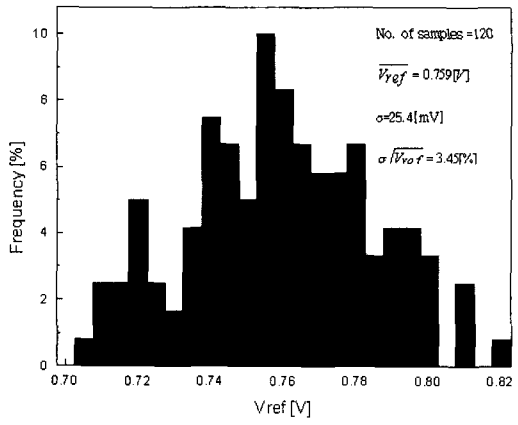


Fig. 4. Measured distributions of V_{ref} for 120 samples at the V_{DD} (2.5 V) and the temperature (25 °C).

3.2 Voltage and temperature characteristics

The voltage and temperature characteristics of the proposed BGR were evaluated by both simulation and measurement as shown in Fig. 5. And the results were all summarized in Table 1. and 2.

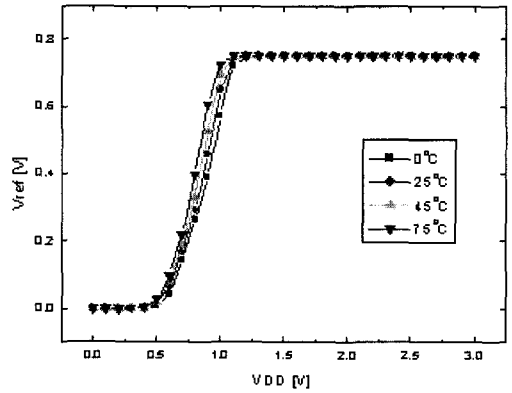
Through the simulation as shown in Table 1, the conventional BGR used single current mirror shows the V_{ref} (max) variation of 0.5 V, but 0.09 V in the proposed BGR.

This is because that the cascode current mirror supplies a stable current having no concern with the variation of the output voltage in case of increasing the output resistance of the current source. The recommendable current sources to increase the output resistance of the current source are the Wilson mirror and the regulated cascode current mirror in addition to the cascode current mirror[5].

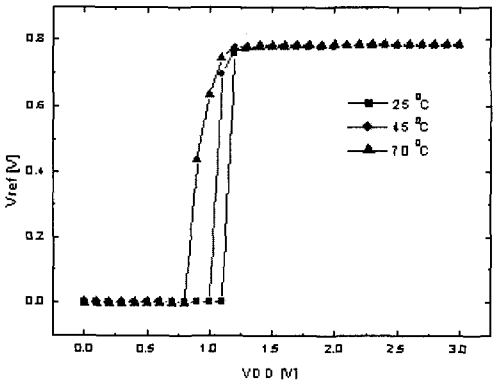
The measured temperature characteristic shows that the BGR starts operating at around 1.0 V, the temperature coefficient of the BGR is 0.2 mV/°C, and the operating current is sub-10 μA.

The maximum V_{ref} from the test result is 6 mV, which is much greater than 0.17 mV from the simulation. This is due to the fact that the temperature coefficients of the BJTs and the resistors of the fabricated test chip are slightly different than those of the model parameters used in simulation.

The starting point seems to vary about 0.3 V over the specified temperature range, which is not captured in the simulation result. This may be due to the unstable operation of the start-up circuit within that voltage range. But since that range is far below to target operation voltage range, this phenomenon should be of no problem.



(a) Simulation results of the proposed BGR.



(b) Measurement results of the proposed BGR.

Fig. 5. Simulation and test results under voltage and temperature variations.

Table 1. Voltage characteristic (Unit: mV).

V_{ref} / V_{DD}	Simulation		Test
	Conv.	Proposed	(Proposed)
2.0V	749.95	750.55	750
2.5V	750.2	750.60	751
3.0V	750.45	750.64	753
V_{ref} (max)	0.5	0.09	3

Table 2. Temperature characteristic (Unit: mV).

V_{ref} / Temp.	Simulation	Test
25 °C	750.60	751
45 °C	750.77	752
70 °C	750.67	757
V_{ref} (max)	0.17	6

3.3 Radiation responses of the BGR

The radiation response is evaluated by using Co-60 gamma source in KAERI experiment setup. The source to wafer distance was 16 cm and the dose rate was 5 krad/hr. The V_{ref} at each cumulated dose was measured using HP4155A-semiconductor parameter analyzer in the probe station at the V_{DD} of 2.5 V and room temperature. Test result is shown in Fig. 6 and is summarized in Table 3. Compared to the results of the voltage and temperature characteristics, the radiation response of the V_{ref} was relatively more severe.

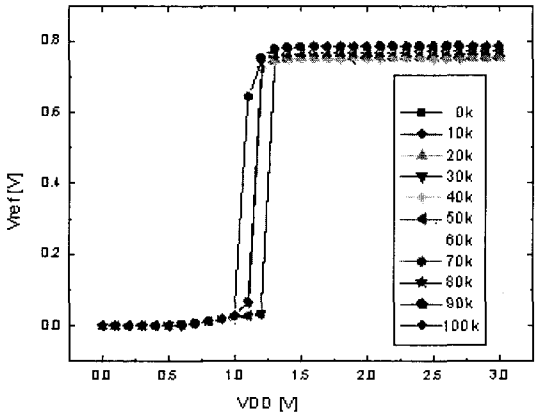


Fig. 6. Test result of radiation response at each cumulated dose.

Table 3. Radiation responses of the BGR (Unit: mV).

Dose / V_{ref}	0 krad	50 krad	100 krad	V_{ref} (max)
	751	779	784	33

Basically, the total ionization dose (TID) effect is the main reason for the radiation response of the BGR, since one of the cumulative effects in semiconductor devices for gamma irradiation is due to the charge trapping in the oxide layer[6].

In MOS devices, the TID effect induces mobility degradation, threshold voltage shift, and leakage current increase. Also in the BJT devices, the TID effect induces mobility degradation and leakage current increase, resulting in degradation of the gain. Therefore, the electrical characteristics of the devices may be the result of the combination of the internal structure and the amount of the TID[7-9].

In the BGR, however, the combination of changed electrical properties of the discrete devices makes it more complicated to understand the V_{ref} change by the radiation dose. It is expected that the TID effect would shift the DC biasing point in the MOS differential amp. In Fig. 1, there can be a mismatch between the two threshold voltages, V_{TH1} and V_{TH2}, of the MOS transistors, T_1 and T_2, if the DC bias point is shifted by the increase of radiation dose, which would result in an offset variation. This also has influence on the precision of the cascode current mirror that should be operating in the saturation mode. The mismatch of other electrical parameters such as conductivity, threshold voltage, and gain can also induce current mismatch in the current mirror. In summary, the radiation dose would have heavy influence on the operation of the BGR, resulting in variation of V_{ref}.

4. CONCLUSION

This paper proposes a new BGR circuit which takes advantage of a cascode current mirror biasing to reduce the V_{ref} variation and a noble sizing technique, which utilizes two related ratio numbers k and N, to reduce the PNP BJT area.

The V_{ref} variation of the BGR has a maximum delta of 6 mV over the temperature range of 25 °C to 70 °C, and 33 mV over the radiation dose range of 0 krad to 100 krad.

Judging from the estimated overall variation over the given voltage, temperature, and radiation range, the proposed BGR can provide an adequate reference voltage to the 10 bit A/D (4-4-4 pipeline architecture) converter of the CMOS APS imager used in the field of X-ray imaging.

Although the V_{ref} variation of the BGR was relatively more severe than the swing of voltage and temperature, the BGR may guarantee its radiation hardness for its lifetime since the cumulative absorbed dose of 100 krad in X-ray imaging is not general before the failure of other function of the CMOS APS.

REFERENCES

[1] Andrea Boni, "Op-Amps and Startup Circuits for CMOS Bandgap References With Near 1-V Supply," IEEE J-Solid-State Circuits, Vol. 37, p. 1339, 2002.

[2] Hironori Banba, Hitoshi Shiga, Akira Umezawa, Takeshi Miyaba, Toru Tanzawa, Shigeru Atsumi, and Koji Sakui, "A CMOS Bandgap reference Circuit with Sub-1-V Operation," IEEE J-Solid-State Circuits, Vol. 34, p. 670, 1999.

[3] Arie van Staveren, Chris J. M. Verhoeven, Arthur H. M. van Roermund, "The Design of Low-Noise Bandgap References," IEEE Trans. Circuits and systems-I: Fundamental theory and applications, Vol. 43, p. 290, 1996.

[4] B. G. Rax, C. I. Lee, and A. H. Johnston, "Degradation of Precision Reference Devices in

Space Environments," IEEE Trans. Nucl. Sci., Vol. 44, p. 1939, 1997.
[5] D. Johns and K. Martin, Analog Integrated Circuit Design, John Wiley & Sons, p. 137.1997.
[6] Andrew Holmes-Siedle and Len Adams, Handbook of Radiation Effects, Oxford New York Tokyo, oxford University Press, p. 95, 1993.
[7] A. H. Johnston, "Radiation Effects in Advanced Microelectronics Technologies", IEEE Trans. Nucl. Sci., Vol. 45, p. 1339, 1998.
[8] A. H. Johnston, B. G. Rax, and C. I. Lee, "Enhanced Damage in Linear Bipolar Integrated Circuits at Low Dose Rate," IEEE Trans. Nucl. Sci., Vol. 42, p. 1650, 1995.