Current Status of Layer Transfer Process in Thin Silicon Solar Cell : a review

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Layer transfer process has emerged as a promising tool in the field of thin silicon solar cell technology. This process can use mono-crystalline silicon as a surface for the epitaxial growth of a thin layer of silicon. It requires some sort of surface conditioning of the substrate due to which the surface become suitable for homo-epitaxy and lift off after solar cell fabrication. The successful reuse of substrate has been reported. The use of the conditioned surface without any kind of epitaxial layer growth is also the issue to be addressed. This review paper basically describes the five most cost effective methods on which works are in progress. Several types of possible problems envisaged by different research groups are also incorporated here with necessary discussion. Work in Korea has already started in this area in collaboration IC Design and Fabrication Centre, Jadavpur University, India and that also has been mentioned.

Keywords : Solar cell, Layer transfer process, Silicon

1. INTRODUCTION

A major motivation for solar cell research and development is a reduction of material cost as well as reliability of the finished module. Today, several low cost promising materials except silicon may be used in the next generation of solar modules after crystalline silicon have been identified and intensively studied such as copper indium diselenide, cadmium telluride. In case of copper indium diselenide solar cells, they are likely to face substantial obstacles to his widespread deployment. Moreover, CdTe cells face a further obstacle due to the toxicity of cadmium. For these reasons, it is likely that c-Si cells will continue to play a dominant role in Solar Photovoltaic for decade to come. Presently about half the cost of a finish module is due to the material itself and around half of the silicon in a CZ- ingot is lost as saw dust. The potential for cost reduction when using material which does not require dicing is therefore substantial. Moreover, large part of the thickness is not needed for electronic performance of the cell. It only gives the cell a rigid structure. This has brought the concept of thin solar cell in the area of photovoltaic research and development. The basic idea in thin solar cell is use of a thin film or layer of active material of thickness of a few micrometers to about 50 micrometers on a low cost rigid substrate.

Layer transfer process in the area of thin silicon solar cell refers to the process wherein a monocrystalline or nearly monocrystalline layer of silicon is lifted off from a CZ- or FZ- silicon wafer before or after fabrication of solar cell and transferred to a low cost substrate. The technique may be more suitable when the device is fabricated before lift off, as all high temperature processes are concluded before transfer of the thin layer in that case. Simple pasting of the layer by transparent glue on any cheap substrate like window glass is possible in that case.

Layer transfer solar cell fabrication concept was introduced first by McClelland et. al.[1] to reduce the material cost of GaAs solar cells as GaAs is a very costly photovoltaic material. The process they introduced is termed CLEFT (Cleavage of Lateral Epitaxial Films for Transfer). It was back in 1980 and the method was not tried for silicon solar cell. Long after that, layer transfer process involving silicon has gotten attention in the

middle of last decade. Fabrication of silicon on insulator (SOI) structure was the primary motive for layer transfer processes developed at that time. VEST (Via hole Etching for the Separation of Thin film) process at Mitsubishi by Arimoto et. al.[2], ELTRAN (Epitaxial Layer Transfer) process at Canon byYonehara et. al.[3,4], SC (Smart Cut) process introduced by Bruel[5] achieved transfer of thin silicon layer successfully. But those are not of much importance in our present context as the costs of fabrication are much higher. However, of these processes, ELTRAN aimed at use of annealed porous silicon layer for epitaxial growth of silicon. This is an idea that has been developed and extended in some of the processes developed later for successful transfer of Si layer in methods which are promising for low cost fabrication of solar cells.

2. DIFFERENT LAYER TRANSFER PRECESS

Layer transfer process for fabrication of thin film silicon solar cell is the latest low cost technology for thin silicon solar cell. All over the world, researchers from different research institutes are deeply involved for the development of this new of area of solar cell technology such as SPS (Sintered Porous Silicon) process at Sony [6] and University of Stuttgart[7,8], PSI (Porous Silicon Process) developed at Bavarian Centre for Applied Energy[9-12], EL (Epi Lift) process developed at Australian National University[13,14]. QMS (Quasi Monocrystalline Silicon) process developed at University of Stuttgart[15,16] and SCLIPS (Solar Cells by Liquid Phase Epitaxy Over Porous Silicon process developed at Cannon[17]. We are trying some variety of QMS process of University of Stuttgart for a thin film layer transfer silicon solar cell[18] in collaboration with IC Design and Fabrication Centre, Jadavpur University, India. Also we have plans to work on SPS and PSI process involving LPE growth of silicon in horizontal slider boat.

2.1 Sintered Porous Si (SPS) Process

Tayanaka et. al.[6]at sony corporation introduced this process of layer transfer and solar cell fabrication by the use of a porous double layer structure on CZ-silicon. Fig.1 shows scheme of the process which reuses the initially taken Si wafer. They started with a 4 inch p-type <100> CZ silicon of resistivity 0.01 to 0.02 Ω.cm and anodized it in 50 % HF : ethanol (1:1) solution with current density and time variation, 1 mA/cm^2 for 8 min, then 7 mA/cm^2 for 8 min to 200 mA/cm^2 for a few (about 5) seconds. This produced 1.7 μm thick layer of 16 % porosity at the top of 6.3 μm layer of 26 % porosity, below which a layer of 0.8 μm of 40-70 % porosity was formed.

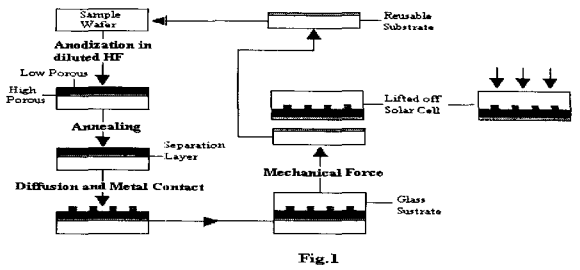


Fig. 1. Scheme of the steps employed for layer transfer in SPS process (PSI and QMS processes also have many similarities to this scheme).

The sample was then annealed in hydrogen up to 1100 °C resulting in recrystallisation of the porous layers. At 800 °C, microholes of diameter 10 to 30 nm started to melt. Finally in the upper low porosity layers the micropore structure changed to small circular pores and voids whose diameter were 10 to 200 nm. In the high porous region broad based pillars and wide voids were formed which converted the region into a separation layer.

After annealing, silicon epitaxial layer was grown in CVD reactor at atmospheric pressure at 1020 °C using SiH_4 gas and H_2-diluted B_2H_6 gas to get 11 μm p-layer (boron concentration 4×10^{17}–4×10^{16} /cm^3) on 1 μm p^+ layer (boron concentration $2\text{-}3\times10^{19}$ /cm^3). For cell fabrication phosphorous was diffused for n^+ layer emitter over the p-type epitaxial layer. For contact to the electrode n^+ diffusion was carried out locally. Then the surface was oxidized for surface passivation. TiO_x layer was formed as antireflection coating by sputtering and oxidation. Aluminum was used for the front electrode material.

A transparent plastic film was then adhered using an adhesive and the film was transferred on plastic substrate followed by dipping in a diluted HF and then silver was painted as the back electrode. The silicon substrate was used again after etching residual porous layer. Cells obtained in the method were tested in AM 1.5 (100 mw/cm^2). For 4.0 cm^2 cell area, V_{oc} of 623mV, J_{sc} of 25.480 mA/cm^2, FF 0.79 and efficiency 12.532 % were obtained.

At Institute of Physical Electronics, Stuttgart, Bergmann et. al.[7] used a similar method to get 14 % efficiency on 24.5 μm cell. Recently they have reported [8] thin film solar cell efficiencies of 15.4 % and 16.6 % for 24.5 μm and 46.5 μm thick cells respectively. They have used double layer porous Si film crystallized at elevated temperature and then deposited by high temperature CVD from $SiHCl_3$, at 1100 °C. 1.5 μm Si film of doping concentration 1×10^{19} cm^{-3} that acts as a back surface field was grown on recrystallised top

surface of 1.5 μm low-porous layer termed as quasi-monocrystalline silicon (QMS) layer. Then an absorber film with a thickness 21.5 μm was deposited to get 24.5 μm thick cell. In another scheme they deposited 5 μm thick BSF layer and then 40 μm thick absorber to get total thickness of 46.5 μm including 1.5 μm quasi-monocrystalline silicon layer. The absorber films have doping concentration of 7 to 9×10^{16} cm^{-3} and the highly doped QMS film did not contribute to photovoltaic current generation. Best solar cell data reported[8] for 4.017 cm^2 area cell are given in Table 1 which represents the best for thin layer transfer silicon solar cell reported so far.

Table 1. Best layer transfer thin silicon solar cell parameters reported from IPE, Stuttgart[8] in 2001.

Total Si film Thickness d(μm)	Cell area (cm^2)	V_{oc} (m)	J_{sc} (mA/cm^2)	FF (%)	η (%)
24.5	4.017	636	30.4	79.7	15.4
46.5	4.017	645	32.8	78.2	16.6

2.2 Porous Si (PSI) process

The porous silicon (PSI, ψ) process[9], called initially as perforated silicon process[10-12] was developed by Brendel. The process has lot of similarities with SPS process with the main difference that Brendel started with a typically textured wafer named waffle shape texture. In fact this process is the first demonstration of use of textured Si surface for layer transfer solar cell. The process was presented for the first time in 1997[10] and it is under development at Bavarian Centre for Applied Energy (ZAE Bayern) currently. In a recent communication[9] they have reported 12.2 % efficient solar cell on 15.5 μm thick transferred layer. This efficiency, although less than the Stuttgart group, is very good for a thin film solar cell which not only consumes less material but also takes low fabrication cost in consideration by avoiding photolithography.

The starting sample is again p^+-type, boron doped, monocrystalline Si substrate wafer that has a specific resistance of 0.01 ± 0.02 Ω.cm. Random pyramid texturisation with average height of 5μm was done by wet chemical etching in KOH solution. Then a porous double layer was developed by electrochemical etching in diluted HF. The surface layer of 20 % porosity was 1 μm thick and etched at a current density of 5 mA/cm^2. The buried separation layer was less than 300 nm thick, porosity above 50 % and etched at a current density of 300 mA/cm^2. The wafer was then annealed at H_2 ambient prior to epitaxy in order to close the pores of the surface as suggested experimentally by Yonehara et. al.[4] and others[15] and also confirmed by simulated modeling of Muller et. al.[18] In the process voids form in the low porosity layer and a separation layer is formed at the high porous region.

After annealing in a commercial CVD reactor at 1100 °C in hydrogen for 30 minutes, a 2μm-thick 5×10^{18} cm^{-3} boron doped back surface field layer was grown first and then a 14 μm-thick 1×10^{17} cm^{-3} boron doped base layer was grown using $SiHCl_3$ as source gas. Phosphorous diffusion from a solid source at 850 °C reduced sheet resistance to 35 Ω per square. A Ti/Pd/Ag grid was evaporated through a shadow musk. A poorly passivating dielectric layer was deposited for optical index matching. Then the cell was attached to a non-coated window glass by the use of a transparent glue [poly-ethylen-phtalate] and then mechanical stress was applied to separate it. The residual sintered porous silicon as well as about half the p^+ layer were etched off. The back surface was then fully covered by evaporated Al. The cell area of 2.1 cm^2 was defined by plasma etching. A section of the processed cell is shown in Fig. 2.

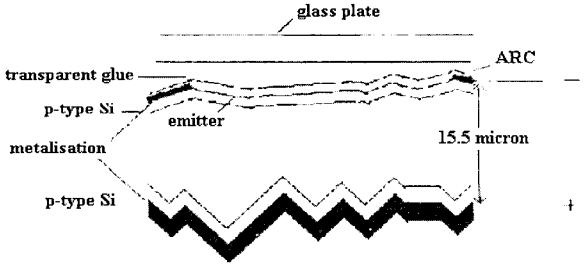


Fig. 2. A section of processed cell in PSI process.

Important characteristics of the epitaxial film obtained are: low defect density of only a few hundred per cm^2, minority carrier diffusion length L_b greater than (20±5) μm and the back surface recombination velocity S_b smaller than $(5\pm2) \times 10^3$ cm/sec. Solar cell characteristics obtained under AM1.5 at 25 °C are: open circuit voltage (600±3) mV, short circuit current density (25.6±0.6) mA/cm^2 and fill factor (79.2±0.8)%.

2.3 Epi Lift (EL) process

Weber et. al.[13,14] at Australian National University (ANU) introduced the epi lift technique. Highly doped <100> oriented Cz wafer was oxidized at first approximately to a depth of 60 nm. Then it was patterned in a square mesh to get oxide free lines of width 2.5-10μm by photolithographic technique. The lines ran in <110> direction and those were at spacing of nearly 100

μm. Epitaxial layer was grown by Liquid phase epitaxy in a tipping boat apparatus using 6 N pure In and UPH ambient. Epitaxial lateral overgrowth about the seed lines occurred and a film of thickness 50 μm to 100 μm was grown in the shape of a mesh as in the seed lines. Since surface energy is minimum for <111> oriented Si surface, the lines in epi-layer grown mesh was enclosed by <111> planes. The epilayer was grown in such a way that its initial section was heavily doped (greater than 10^{18} cm^{-3}) and remaining outer part lightly doped. Using an etchant [HF:HNO_3:CH_3COOH :: 1:3:8] that etches heavily doped silicon faster than lightly doped silicon, the epilayer was lifted off from substrate. Typical films were found to have average lifetime of 7 μs corresponding to minority carrier diffusion length of over 100 μm which is more than twice the thickness of epilayer. No cell efficiencies were reported to the best of our knowledge.

2.4 Quasimonocrystalline silicon (QMS) process

This process was introduced by Rinke et. al.[15,16] and they tried this method before the SPS process being developed at Stuttgart. Initially the group at Stuttgart reported this idea where bi-layer porous silicon was to be annealed and then the upper low porous layer would be used for device fabrication without any further epitaxy. Due to the existence of voids in the annealed low porous region they called it quasi-monocrystalline silicon. It was envisaged that the voids in the sintered layer would introduce sufficient light trapping[Fig. 3] in a device with planar surfaces, so that further texturing would not be needed.

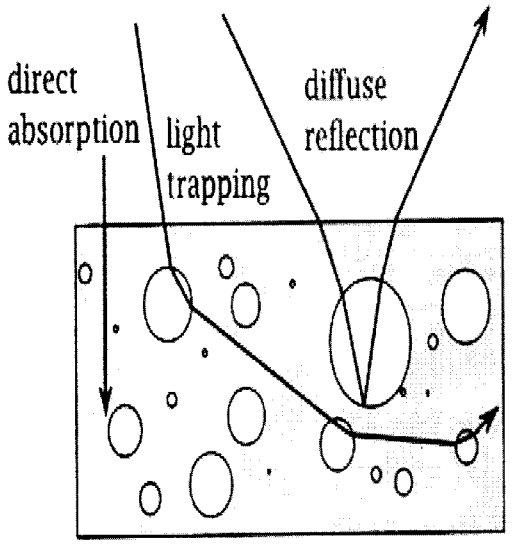


Fig. 3. A pictorial scheme of light trapping in voids of QMS layer as proposed by Bergmann et. al.

Minority carrier life time measurement revealed life times around 0.4 μs and demonstrated a high efficiency potential for solar cell using small amount of silicon and simple steps of fabrication. Transfer of 30 sintered porous layer on glass substrates from a single wafer of 500 μm thickness was reported. A short circuit current density of 11.1 mA/cm^2 was reported[20] in case of a 4 μm-thick sintered porous Si layer before lifting the layer off from a p-type wafer. Cell efficiency has not yet been reported to the best of our knowledge. However, the idea of using the QMS film directly as device layer appears to be in active consideration of the Stuttgart group[7,19].

2.5 Solar cells by liquid phase epitaxy over porous silicon (SCLI PS)

S. Nishida et. al.[17] developed a new apparatus for liquid phase epitaxy (LPE). The wafers were p^+ type, 0.01 - 0.02 Ω.cm resistivity and 12.5 cm diameter. Initially a porous layer of about 10 μm was grown on the substrate by anodizing in a HF solution in a current density of a few mA/cm^2 to 30 mA/cm^2. Over the porous layer 10 μm or more thick LPE layer was grown in 4N In solvent in quartz container in a modified dipping type LPE apparatus. In the apparatus the wafer carrier could hold several wafers at separations of 10 mm each at a small angle to the horizontal (Fig. 4).

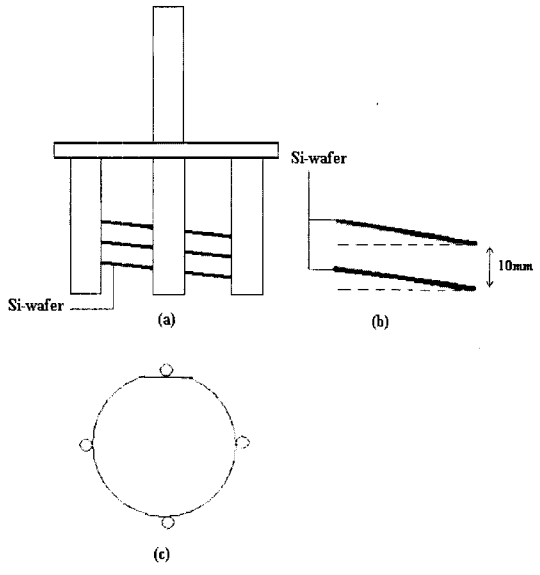


Fig. 4. Wafer carrier in improvised dipping boat used for LPE by Nishida et. al.
a) configuration of wafer in carrier (side view)
b) inclination of wafers to horizontal,
c) top view of a wafer placed on carrier

Melt removal and a batch process of LPE was thus done easily in the system. Higher growth thickness was observed on the lower side of the wafers as expected by other research groups also on the consideration of convection[22]. Diametrically across the 12.5 cm wafer, thickness of LPE layer was found to be somewhat higher near the edges compared to the center. Such thickness difference further increased on rotating the samples in the melt. However, epilayers were obtained in which thickness variation was less than 50 % of minimum thickness in the layer.

For a thick film, more than 80 μm, average value of life time found to be 10 μs. No significant contamination of undesired metals was observed despite using 4N Indium. Then n^+ layer was formed on the surface of p epilayer, front contact was made and the semi finished cell was then attached to a substrate by adhesive. Then the porous layer was sacrificed by chemical etching to get the cell on epi-layer lifted off from original wafer. Al-Si alloy layer was used for back metallization of the Si film. For a cell lifted by chemical etching method 9.5 % efficiency (V_{oc}=520 mV, J_{sc}=27.5 mA/cm^2, FF=0.663, cell area = 0.2 cm^2) was obtained. In this method, LPE layer was formed directly on porous silicon layer without any prebake and there was no double layer porous silicon.

3. DISCUSSION

All the processes discussed above are at developmental stage. Each research group is hopeful about the prospect of their method, albeit limitations. Following discussion is intended to summaries, compares and comment on different process aspects, viz., choice of substrates and initial surface conditioning, film growth, light trapping, cell processing, lift off procedures and cell parameters as obtained, in different methods.

3.1 Choice of substrate and initial surface conditioning

All the processes have considered highly boron doped low resistivity (10^{-1} Ω-cm to 10^{-3} Ω-cm) p^+ CZ <100> type silicon wafers. In all cases surfaces have been conditioned initially in one way or the other to facilitate layer transfer afterwards. Formation of porous silicon has been the done in all cases except EL process in which the surface has been selectively oxidized. In SPS and PSI process the porous silicon layers are double layer and those are sintered to get three main advantages, viz., better crystallinity of top surface of the substrate for epitaxial growth, development of small voids in the body of the low porous layer and development of a well defined separation layer at the high porous region which facilitates later lift off of the low porous layer. In QMS process this step is said to be still more important as the sintered low porous layer itself form the device layer. In SCLIPS process the porous layer is a single layer and the high temperature-annealing step is avoided. Some of these facts are summarized in Table 2.

The surface conditioning procedure followed in EL process seems to be expensive than that in other methods.

Table 2. Substrate and surface conditioning reported for different methods of layer transfer process.

Method (working group)	Substrate (Type, size, resistivity,Doping)	Porous Silicon Formation			Annealing	
		Electrolyte	Current density (time)	Thickness of porous layer (porosity)	Temp. (ambient)	Result of Annealing
SPS[6]	CZ-p^+<100> 10cm. dia., 0.01-0.02Ω.cm, boron	50% HF: ethanol(1:1)	1mA/cm^2 (8 min) 7mA/cm^2 (8 min) 200mA/cm^2 (5 Sec)	1.7μm (16%) 6.3μm (26%) 0.8μm (40-70%)	1100°C (H_2)	Closure of most of the surface pores. small voids in the body
SPS & QMS[15] (Stuttgart)	CZ-p^+<100> 10cm. dia., 0.01-0.5Ω.cm boron.	HF & ethanol	moderate High	1 to 8μm (20%) 1.5μm (40%)	1050°C (H_2)	Separation layer developed
PSI[9] (ZAE Bayern)	CZ-p^+<100> textured for random pyra- mid, 0.01 – 0.02Ω-cm, boron.	20% HF, 20% water and 60% Ethanonl	5mA/cm^2 300mA/cm^2	<1μm (20%)	1100°C (H_2)	
SCLIPS[17] (Canon)	p^+<100> 12.5 cm. dia., 0.01-0.02Ω-cm	HF solution	a few mA/cm^2 to 30mA/cm^2	≥10μm	No annealing	
EL[13] (ANU)	CZ p^+<100>	Oxidised and patterned into square mesh with oxide free lines of 2.5-10μm width spaced 100μm apart.				

3.2 Film growth

In the SPS and PSI processes epi-films have been grown under high temperature chemical vapor deposition at about 1050 °C. In some cases in PSI method ion assisted deposition technique has been employed as test cases but the films obtained have not been superior to CVD films. In EL and SCLIPS the growth method is Liquid Phase Epitaxy processes. In SCLIPS method the growth substrate used is just a porous silicon surface, which is not recrystallised by sintering. QMS process avoided epitaxy. Considering cost factor one must like QMS process. However, this choice could not be placed on a solid ground till cell reports based on this method were available. Appropriate optimization and batch processes can make either of CVD and LPE cost effective. IAD should be kept out of consideration from the view point of cost effectiveness also.

3.3 Light trapping

Good light trapping is a very important feature for thin film solar cells. In the PSI process textured film is taken as starting substrate with this factor in mind. The porous silicon layer on which epilayer grows in this method provides a back surface which increases light trapping to some extent as demonstrated by the Zettner et. al[23]. In SPS process also back surface reflector is used by the Stuttgart group. In fact, importance of using diffuse optical scatterers at both front and rear surfaces has been duly emphasised by them. It has been envisaged in their theoretical modeling that[22] with other parameters remaining same, a 20 μm thick cell could produced 15 % efficiency for both surfaces flat cell, 16.5 % efficiency for cell with front surface flat but back surface with diffuse reflector and 18 % efficiency for cell with both rear and front surfaces with diffuse optical scatterers. The QMS film serves as a source of diffuse reflection[25] of light at the back of epilayer. In EL process the Si mesh serves the purpose of acting as good light traps. In SPS process the epilayer has a sintered porous silicon layer under the top epilayer. This layer has many voids, which may trap light. However, the effect of such voids in actual solar cells is not yet clearly understood. Presently reported SPS method of Stuttgart group considers texturing the epilayer by anisotropic etching in KOH-Isopropanol solution for random pyramid formation to be attractive. No special light trapping arrangement has been reported in SCLIPS method.

In QMS method the internal voids should be effective in light trapping. It was envisaged that the voids of diameter 100 nm to 1 μm would be created by annealing at high temperature and those would help light trapping. Experimentally it was found that QMS film of thickness 4 μm would increase the optical absorption by a factor of ten[16] at a photon energy hν=1.5 eV (Fig. 5).

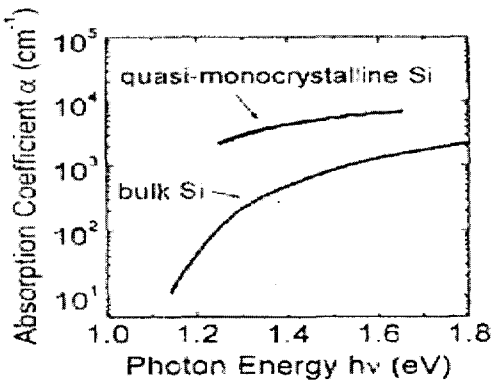


Fig. 5. Higher optical absorption in QMS layer (found experimentally for a 4 μm QMS layer) compared to crystalline (bulk) Si as reported in ref.15,16.

In fact, this prompted the idea of using QMS layer directly for solar cell fabrication. Although, it was found later[19] that the average diameter of the voids were in the range of 30nm to 80nm depending on annealing temperature, the experimental result of higher absorption stands. Also, a model of light trapping has been proposed [26,27] for such layers, which explains light trapping by small voids. May be the smaller voids would also be advantageous in so far as carrier mobility is considered. Realization of this concept of internal light trapping mechanism without sacrificing in mobility and lifetime of carriers may possibly be one of the milestones in ultimate success of this method.

3.4 Cell Processing and lift off

Cell processing has been reported in SPS, PSI and SCLIPS process. Oxidation, window opening to define cell area, texturisation, diffusion for emitter formation, photolithography, antireflection coating are the steps in SPS process. PSI process does not use texturisation after film growth. For low cost cells simpler cell processing would be needed. One step towards simplification is to grow emitter by epitaxy, which is faster than diffusion [17]. Avoiding photolithography would be another step to reduce cost of processing. To lift the thin film solar cell, method adopted in SPS, PSI and QMS processes use a superstrate and transparent glue. In SPS process of Stuttgart group 30 thin layers are reported[25] to have been lifted off from the 500μm wafer. However, in QMS process lift off after cell fabrication is not reported. It seems to be a difficult task in our experience[18] also. However, lifting off the QMS layer using glass superstrate before cell fabrication and reuse of the substrate have been demonstrated[15] as in SPS process of the Stuttgart group. Lift off has been reported in EL process using the method of chemical etching. The layer

is thicker when compared to other processes. In SCLIPS method also, the lift off procedure uses chemical etching. In PSI, SPS, EL and SCLIPS processes also viability of reuse of the substrate have been envisaged. For PSI method possibility of at least ten fold reuse of the substrate is claimed to be easy.

3.5 Cell parameters

As per the best information available to us, cell parameters have been reported for SPS processes of Sony and Stuttgart, PSI process of ZAE Bayern and SCLIPS process of Cannon. Stuttgart group has improved upon the performances at regular intervals. The group at ZAE Bayern claims that the efficiency of 12.2 % achieved by them by PSI method is of high importance as their method considers low cost processing by avoiding photo-lighography[9]. Reported efficiencies and other cell parameters are listed in Table 3.

For 46.5 μm thick cell someone may object to it being called a true thin cell. In that sense highest efficiency achieved till date is 15.4 % with 24.5 μm cell. However, by device simulation Bergmann et. al.[8] have shown that efficiency above 20 % is achievable in 20 μm cell if both Si surfaces are textured to give 90 % lambertian scattering.

The projection is indicated in Fig. 6 where the proposed device structure is also shown. Brendel et. al[9] have pointed out that a surface textured at front side of the device would be better than their device with random pyramid texture at the back surface. In that case the front surface will receive the random pyramid texture and back surface contact by Al would be taken on top of the p-layer before detachment of the cell. These steps, as envisaged, would improve efficiency further while reducing processing cost.

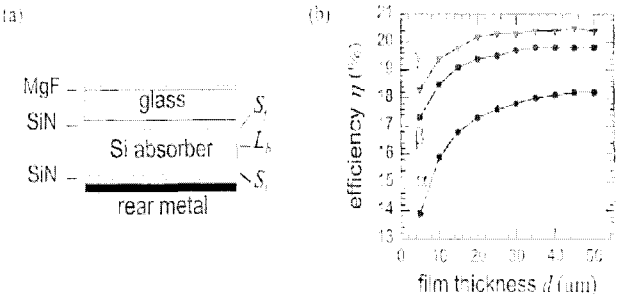


Fig. 6. Best layer transfer cell parameter projected by Bergmann et. al. as reported in ref 8.

a) Schematic cross section of the device structure for device modeling using a front surface recombination velocity of S_f=5000 cm/s, a rear surface recombination velocity of S_r=100 cm/s and a volume diffusion length L=100 μm. Doping of the p-type base is set to 3 x 10^{17} cm^{-3}, while the n^+-type emitter has a sheet resistance of 100 Ω/square. The MgF layer has a thickness of 90 nm. The simulation includes a shading loss of 2.5 %.

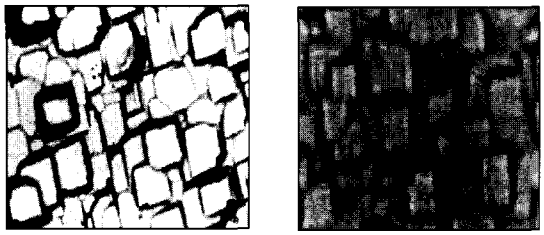
b) Results of device modeling. Curve (α) flat Si surfaces, curve (β) rear Si surface has 90 % Lambertian reflection, curve (γ) front and rear Si surface with 90 % Lambertian reflection.

Table 3. Cell parameters for thin silicon layer transfer solar cells.

Method (Group and Year of Report)	Total Si film thickness (μm)	Cell area (cm^2)	V_{oc} (V)	J_{SC} (mA/cm^2)	FF	η (%)
SPS[6] (Sony 1998)	20	4.0	0.623	25.480	0.790	12.532
SPS[23 (Stuttgart 1999)	49	1.001	0.594	21.27	0.733	9.26
SPS[19] (Stuttgart 2000)	23	4	0.632	26.7	0.805	13.6
SPS[8] (Stuttgart 2001)	24.5 46.5	4.017 4.017	0.636 0.645	30.4 32.8	0.797 0.782	15.4 16.6
PSI[9] (ZAE Bayern 2001)	15.5	2.1	0.600	25.6	0.792	12.2
SCLIPS[17] (Canon 2001)	--	0.2	0.52	27.5	0.663	9.5

4. OUR RESEARCH PREGRAM

In our collaborative research programme, we have called these layers Quasi Monocrystilline Porous Silicon (QMPS) layer. We have successfully separated QMPS layers[18]. Fig. 7a and Fig. 7b show photomicrographs of an annealed porous silicon layer and a lifted off annealed porous silicon layer of thickness about 5 μm.



(a) (b)

Fig. 7. (a)Photomicrograph of a double layer porous silicon surface before annealing (b)Photomicrograph of an annealed quasi monocrystalline porous silicon (QMPS) surface lifted on glass plate.

The lifted off layer has dusty porous silicon of the separation layer. Also we have been able to separate QMPS layer after diffusion and metallization of the top surface of the QMS layer. But we have faced problem in soldering on the metal contact over emitter layer[18]. Further optimization of the processes of porous silicon formation, annealing process, solar cell fabrication on the QMPS layer, soldering and lift off after metal contact formation are under study.

We have proposed a model of light trapping[26,27] in the QMPS layer to get better insight into its light trapping mechanism. The possibility of higher absorption at all ranges in the full solar spectrum is discussed there, while experimental evidence of higher light trapping is available for photon energy in the range of 1.25 eV to 1.75 eV. The theoretical model shows that the absorption coefficient remains high in the full spectrum of importance. Effect of changing the porosity of low porous layer, size of voids and thickness of QMS layer on light trapping are also taken into consideration. It is seen that smaller voids would be more helpful for light trapping. Thus it has been important to find methods of making QMPS layers with small voids and measure the absorption coefficient of those. However, it is also important to study the effect of size of voids in the QMPS layer for carrier mobility and other electronic parameters important for solar cell. Annealing temperature and ambient might have some effect on the size of the voids and electronic quality of the annealed layer. Thus, experimental work and theoretical modeling may also help better understanding of electronic quality of the QMPS layer. So, we are aiming such theoretical optimization of annealing temperature to get best of both optical trapping and carrier mobility. Also we are studying the annealing ambient and temperature experimentally. The substrate wafer used for QMPS film is highly boron doped. The QMPS layer obtained is also highly boron doped. So, some phosphorous doping to the whole thickness of QMS layer after high temperature annealing may be beneficial before emitter formation at the top. Effect of some organic vapour incorporation to the QMS layer may also be studied for better result.

We have a horizontal slider boat LPE facility improvised for use in a sandwich method of growth[22] of silicon and we are planning to try SPS process also using LPE.

5. CONCLUSION

Though the layer transfer process is relatively new in the field of thin film silicon solar cell it has emerged as a promising process with a large number of advantages over thin film techniques. t needs homoepitaxy. Not only seeding problems of heteroepitaxy but also problem of polycrystalline films with grain boundaries is solved. The recombination loss is considerably avoided due to this improvement. Achievement of 15.4 % efficiency for a cell of 24.5 μm thin film is a good progress indeed. Additional improvements especially with back surface reflection arrangement and simplified process techniques are still under consideration. Better understanding of mechanisms of the process such as porous silicon formation, annealing of the substrate and light trapping would give further insight into the process and devices related to layer transfer. The feasibility of producing a cell with 20 % efficiency was demonstrated using optical and electrical modeling. A real thin film solar cell of thickness below 10 μm could be realized if QMPS layer could come fairly good in electronic quality with very high absorption co-efficient. So, the researchers working in this field are extremely hopeful for approaching a new era of thin film solar cell technology based on transfer of mono-crystalline Si-layers.

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