Characteristics of a High Power Factor Boost Converter with Continuous Current Mode Control

Cherl-Jin Kim* and Jun-Young Jang*

Abstract - Switching power supply systems are widely used in many industrial fields. Power factor correction (PFC) circuits have a tendency to be applied in new power supply designs. The input active power factor correction (APFC) circuits can be implemented in either the two-stage approach or the single-stage approach. The two-stage approach can be classified into boost type PFC circuit and dc/dc converter. The power factor correction circuit with a boost converter used as an input power source is studied in this paper. In a boost power factor correction circuit there are two feedback control loops, which are a current feedback loop and a voltage feedback loop. In this paper, the regulation performance of output voltage and compensator to improve the transient response presented at the continuous conduction mode (CCM) of the boost PFC circuit is analyzed. The validity of designed boost PFC circuit is confirmed by MATLAB simulation and experimental results.

Keywords: Active power factor correction (APFC), Continuous conduction mode (CCM), Power factor correction (PFC), single-stage and two-stage, transient response.

1. Introduction

Conventional Switched Mode Power Supplies (SMPS) with diode-capacitor rectifier front-ends have distorted input current waveforms with their high harmonic content. Typically, these SMPS have a power factor lower than 0.65.

To deal with this problem, the input APFC of SMPS needs to be introduced. APFC techniques are used in the majority of applications due to their superior performance. The input APFC circuits can be implemented in either the two-stage approach or the single-stage approach. In the single-stage approach, the PFC switch and controller are saved. The single-stage approach may be attractive for applications at lower power levels. However, unlike in the two-stage approach, the dc voltage on the energy-storage capacitor in a single-stage PFC circuit is not regulated. As a result, in universal-line application, the energy-storage capacitor voltage varies with the load and line variation. In the case of the two-stage approach, the dc voltage is regulated throughout the entire line input voltage range from 90Vac to 265Vac. The two-stage approach is the one most commonly used. In this approach, an APFC stage is employed as the front-end in order to force the line current to track the line voltage [1]. The two-stage approach can be classified into boost type PFC circuit and dc/dc converter. In a PFC circuit there are two feedback control loops. One loop is a current feedback loop that controls the instantaneous input current to maintain the same shape as the instantaneous input voltage. The other loop is a voltage feedback loop that adjusts the overall amplitude of the input current to keep the output voltage constant.

In this paper, the regulation performances of the output voltage and the compensator are investigated to improve the transient response presented at the CCM of the boost PFC circuit.

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2. Power Factor Correction Approach

2.1 Single-Stage Approach

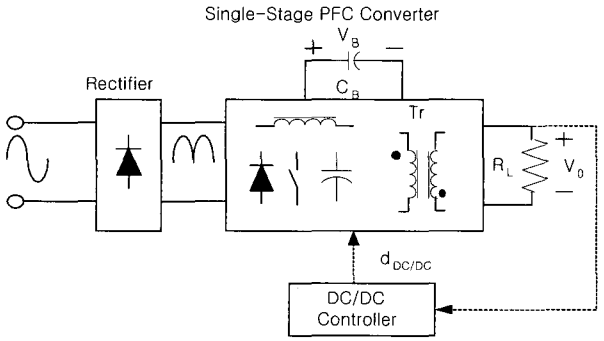


Fig. 1 Structure of single-stage PFC circuit.

The structure of the single-stage PFC circuit is shown in Fig. 1. The single-stage approach uses only one switch and a controller to shape the input current and to regulate the output voltage. The single-stage approach has the advantage of reducing the number of components.

However, the energy storage capacitor voltage (V_B) is no longer loosely regulated at a constant value because the controller is used to regulate the output voltage, not the V_B. As a result, in universal line application (90~265Vac), the storage capacitor voltage varies with the load and line variation. The wide voltage range has a detrimental effect on the conversion efficiency, and it requires a high voltage rating component compared to the two-stage PFC circuit. The total loss in the single-stage approach may be higher than in the two-stage approach. Therefore, the efficiency of the single-stage approach may be lower than that of the two-stage approach. The single-stage approach may be more useful for applications at lower power levels. At lower power levels, the overall cost of the single-stage approach may still be lower than that of the two-stage approach.

According to the continuity of the input inductor current, the single-stage PFC circuits can be classified into discontinuous conduction mode (DCM) and CCM. Typically, the DCM single-stage PFC circuits are simpler than their CCM counterparts. As a result, the implementation of the DCM is low cost. However, it requires a larger input EMI filter and has lower efficiency due to higher current stress. Thus, the DCM implementations are usually suitable for low power applications [1].

2.2 Two-Stage Approach

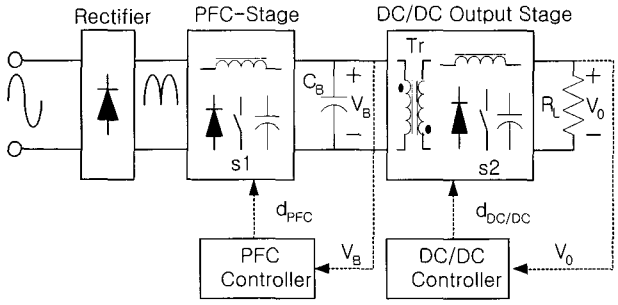


Fig. 2 Structure of two-stage PFC circuit.

The structure of the two-stage PFC circuits is shown in Fig. 2. There are two independent power stages in the two-stage PFC circuits. One is a boost type PFC circuit and the other is a dc/dc converter. The dc voltage is typically regulated at around 400Vdc in the entire line input voltage range from 90Vac to 265Vac. The high bus voltage V_B minimizes the bulk capacitor value for a given hold-up time. The PFC circuit senses the line voltage waveform and forces the input current to track the line voltage to achieve the unit input power factor. They are able to meet the European line current harmonic regulations defined in the IEC 61000-3-2 documents. The boost topology is well suited for PFC since the boost inductor is in series with the ac power line. This results in minimum conducted EMI at the line when the circuit operates in CCM. For high power levels, the two-stage PFC approach is more beneficial.

3. Structure of the Boost PFC Circuit

The CCM boost converters are controlled with peak, average and hysteretic current mode control methods. They require a smaller input EMI filter and have higher efficiency due to lower current stresses. The CCM boost is well suited for medium and high-power applications.

The DCM boost PFC circuit with variable frequency control method operates in the critical conduction mode. It switches on when the inductor current reaches zero and switches off when the inductor current meets the desired input current reference voltage. This operates right on the border between continuous and discontinuous current mode, which results in variable frequency operation. The operation principle of the constant frequency control method is the equally variable frequency control method. The variable frequency control method has a zero current detection circuit. Unlike in the CCM boost, the limitations have high current stresses. But its advantage is that it operates without use of an oscillator. Zero current switching (ZCS) is essential to reduce switching loss. Also, the advantage is simplicity of control, absence of diode reverse recovery related problems, etc.

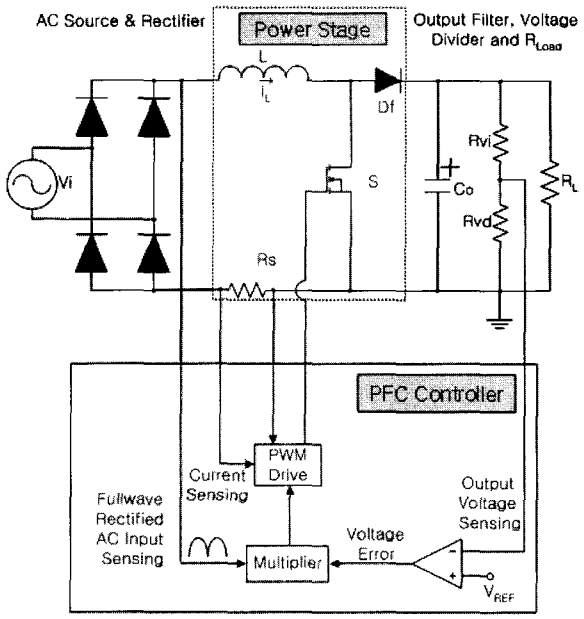


Fig. 3 Average current mode controlled CCM boost PFC circuit.

Fig. 3 shows a simplified CCM boost PFC circuit of average current mode control. In the peak current mode control method, the switch is turned on at constant

frequency and remains on until the sensed current reaches the commanded value, at which time it is turned off. Control can be based on either the switch current or the inductor current. This is the most popular type of current mode control in typical dc-to-dc converters. However, it has some limitations when it is used in power factor preregulators (PFPs). Thus, it is difficult to implement external ramp compensation. Moreover, some distortion in the input current is inherent to this control method.

The variable hysteresis control method works by comparing the inductor current against the commanded value with a hysteretic comparator. The advantage of variable hysteresis control lies in its implementation, in which only a hysteretic comparator is needed, in addition to its ability to produce low distortion in the input current waveform. The main disadvantage of this method is that it operates at variable switching frequency that must be limited near time voltage zero crossing.

The average current mode control method allows a better input current waveform. Here the inductor current is sensed and filtered by a current error amplifier whose output drives a pulse width modulation (PWM) method. In this way the inner current loop tends to minimize the error between the average input current and its reference. This control scheme inherently provides constant frequency operation. The advantages of average current mode control in PFPs are related primarily to its ability to produce a lower distortion rate in the input current waveform than in the above case [2, 3].

4. Model Analysis

Model analysis is performed to use the modeling and small-signal analysis of the controlled on-time boost power-factor-correction circuit [4]. The controlled on-time boost PFC circuit has been widely used for low-power applications. It is analyzed in relation to the regulation performance of the output voltage and compensator to improve the transient response presented at the CCM of the boost PFC circuit. The boost PFC circuit is confirmed by MATLAB simulation.

Fig. 4 shows the boost PFC circuit using simulation. Initially, the PFC circuit assumes an on-time operation where the switch is turned on and the ramp signal, v_{ramp}, increases with the slope of s_e. When the v_{ramp}, reaches the control voltage, the comparator resets the latch and the PFC circuit commences the off-time operation by turning the switch off and resetting the v_{ramp}. When the inductor current is reduced to zero, the zero-current detector sets the latch and the PFC circuit resumes its on-time operation.

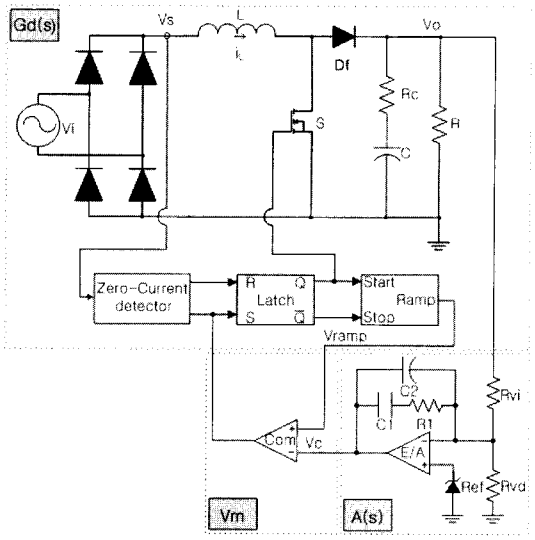


Fig. 4 Simulated controlled on-time boost type PFC circuit.

The PFC circuit assumes that rectified line voltage, output voltage, and control voltage remain constant within each switching period because switching frequency is higher than line frequency. The average model of the power stage and modulator presents to be v_c.

4.1 Average Model

The PWM switch combined with an inductor is shown in Fig. 5. The average expression for the voltage across the switch can be given by

$$V_{ba}(t) = (1-d)V_{pa}(t) \tag{1}$$

Where d represents the duty of the switch $V_{pa}(t)$ represented the time-averaged value for the respective voltage. By applying the power balance condition to Fig. 5, it follows that

$$I_p(t) = (1-d)I_L(t) \tag{2}$$

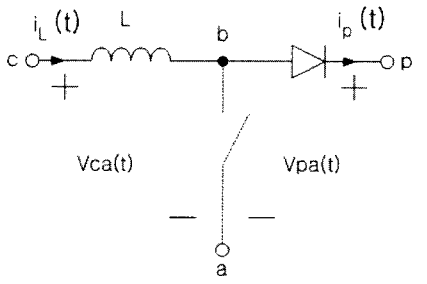


Fig. 5 PWM switch with inductor.

Referring to Fig. 6, the slope of the ramp signal (s_e) can be written as

$$s_e = \frac{v_c}{dT_s} \tag{3}$$

And the on-time slope (s_n) and off-time slope (s_f) of the inductor current can be given as

$$s_n = \frac{v_s}{L} \tag{4}$$

$$s_f = \frac{(v_o - v_s)}{L} \tag{5}$$

The time-averaged value of the inductor current can be found to be

$$i_L = \frac{T_s}{2}[s_n d^2 + s_f (1-d)^2] \tag{6}$$

Which gives an expression for the duty cycle as

$$d = 1 - \frac{2Ls_e i_L}{v_c v_o} \tag{7}$$

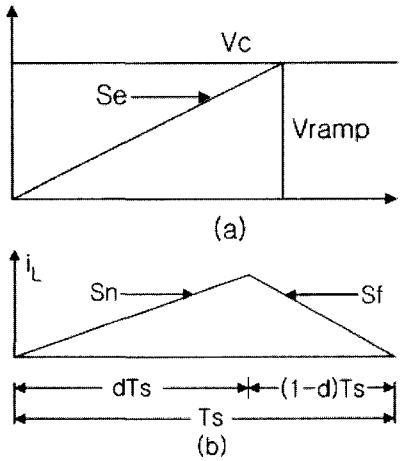


Fig. 6 Theoretical waveforms. (a) The slope of the ramp signal; (b) The on-time and off-time slope of the inductor current.

4.2 Small-Signal Model

The small-signal model of the PFC circuit can be obtained, in principle, by linearizing the average model. However, unlike cases for dc-to-dc converters, the operating conditions of PFC circuits vary extensively within each line period. One simple solution to this problem is to consider the PFC circuit as a dc-to-dc converter with an equivalent dc input that corresponds to the *rms* of the rectified line voltage.

Assuming the input of the power stage is a dc voltage identity to the *rms* value of the rectified line voltage, (1) and (2) can be linearized to be

$$\hat{v}_{ba} = (1-D)\hat{v}_{pa} = V_{pa}\hat{d} \tag{8}$$

$$\hat{i}_p = (1-D)\hat{i}_L = I_L \hat{d} \tag{9}$$

With $D=(V_o - V_{rms})/V_o, V_{pa} = V_o, I_L = I_o/(1-D)$.

where V_o is the average value of the output voltage, I_o is the average of the load current, and V_{rms} represents the *rms* value of the rectified line voltage.

In the case of the small-signal modulator model, by linearizing (7), the small-signal duty ratio can be expressed as a linearlization to be

$$\hat{d} = \frac{1-D}{V_c}\hat{v}_c + \frac{1-D}{V_o}\hat{v}_o - \frac{2Ls_e}{V_c V_o}\hat{i}_L \tag{10}$$

With, $V_c = 2Ls_e I_L/(1-D)V_o$.

From the following equation (11), (12) can be found to perform the control-to-output transfer function.

$$\begin{aligned} \hat{v}_o &= \frac{R(1+sCR_c)}{1+sC(R+R_c)}\hat{i}_o \\ \hat{i}_o &= (1-D)\hat{i}_L - \frac{Vo}{R(1-D)}\hat{d} \\ \hat{i}_L &= \frac{V_o}{sL}\hat{d} - \frac{1-D}{sL}\hat{v}_o \end{aligned} \tag{11}$$

Equation (10) can be rewritten as

$$\hat{d} = \frac{1-D}{V_c}\hat{v}_c + \frac{1-D}{V_o}\hat{v}_o - \frac{R(1-D)^2}{V_o}\hat{i}_L \tag{12}$$

The control-to-output transfer function can be written as

$$\frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{V_o}{V_c}\frac{(1+sCR_c)}{(2+sC(R+2R_c))} \cdot F_{pz}(s) \tag{13}$$

Where $F_{pz}(s) = \{R(1-D)^2 - sL\}/\{R(1-D)^2 + sL\}$.

The $F_{pz}(s)$, a polynomial consisting of the right-half-plane (RHP) zero and left-half-plane pole (LHP) located at the same frequency does not affect the magnitude of v_o/v_c yet introduces a 180° phase delay around $w_{pz} = R(1-D)^2/L$.

The simulation waveform of control-to-output transfer function is shown in Fig. 7.

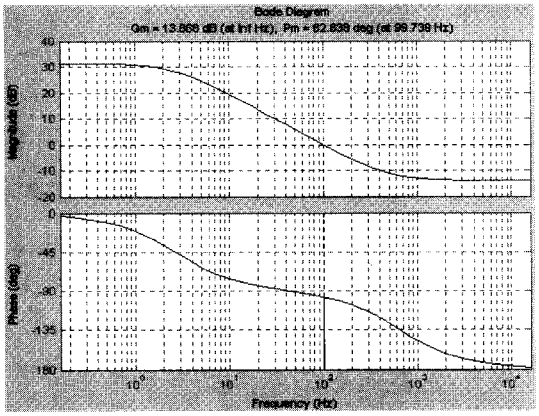


Fig. 7 Simulation waveforms of control-to-output transfer function.

The transfer function of voltage error amplifier can be written as

$$A(s)=\frac{v_c}{v_o}=\frac{(1+sC_1R_1)}{s(C_1+C_2)R_{vi}\left\{1+s\dfrac{C_1C_2}{(C_1+C_2)}R_1\right\}} \quad (14)$$

Where, zero point frequency: $fz=1/(2\pi C_1R_1)$ and pole point: $fp=(C_1+C_2)/2\pi C_1C_2R_1\cong 1/2\pi C_2R_1$.

The simulation waveform of voltage error amplifier gain is shown in Fig. 8.

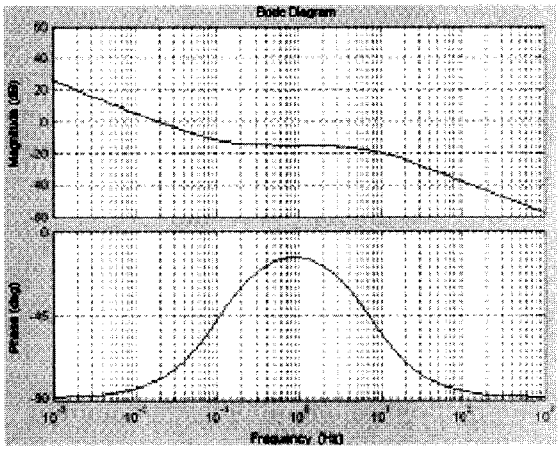


Fig. 8 Simulation waveforms of voltage error amplifier gain.

The voltage control loop gain can be given by

$$T_v(s)=G_d(s)\cdot\frac{1}{V_m}\cdot A(s) \quad (15)$$

Where, $A(s)$ is the gain of voltage error amplifier, $1/V_m$ is the gain of comparator, $V_m=5.4$.

The simulation waveform of voltage control loop gain is shown in Fig. 9.

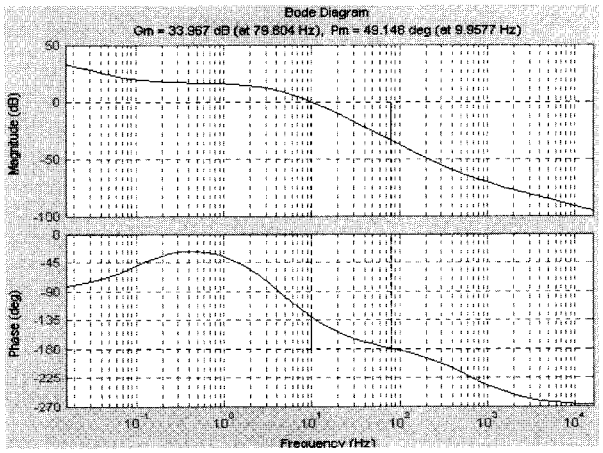


Fig. 9 Simulation waveform of voltage control loop gain.

In conventional designs, the elimination of the even harmonics of the line frequency from the voltage loop is accomplished by closing the voltage loop at a low frequency (usually 10-20Hz), which is significantly lower than the frequency of the second line harmonic. As a result, the dynamic response of the low-bandwidth voltage controller is poor and over-design of the power stage as well as a downstream DC-DC converter may be required to account for increased voltage overshoots and dips during transients. The phase margin is 45°-60° by good transient response. Design reference of voltage control loop gain is presented in Table 1.

Table 1 Design reference of voltage feedback loop gain

Compensator R1	Pole frequency	Gain Margin (GM)	Phase Margin (PM)	Crossover Frequency (fc)
56kΩ	18.94Hz	40dB	94.8°	5.73Hz
100kΩ	10.79Hz	36.6dB	66°	8.73Hz
150kΩ	7.19Hz	34dB	49.1°	9.96Hz
200kΩ	5.39Hz	32.2dB	40.1°	10.4Hz
250kΩ	4.32Hz	31dB	34.6°	10.7Hz

5. Experimental Results

In this paper, Fig. 3 shows the design of the CCM boost PFC circuit with average current mode control. The designed boost PFC circuit is an experimental 2[kW] prototype converter [5]. The parameters of the manufactured boost PFC circuit are shown in Table 2.

Fig. 10 shows the organization of the experimental device that is designed and manufactured with the boost type PFC circuit.

Table 2 Parameters of the Experiment and Simulation.

Input voltage (Vi)	110/220[V]
Output voltage (Vo)	320[V]
Line frequency (f)	60[Hz]
Switching frequency (fs)	25[KHz]
Output capacitor (Co)	1500[uF]
[illegible] (L)	917[uH]
[illegible] load (RL)	6A
[illegible] device (S)	VCES =600V, IC=20A
[illegible] diode (Df)	VR =600V, IF (AV) =15A
Rs	0.22[Ω]
R1, Rvd	820[KΩ], 8.2[KΩ]
R1	56[KΩ]→100[KΩ]→150[KΩ]
C1, C2	10[uF], 150[nF]

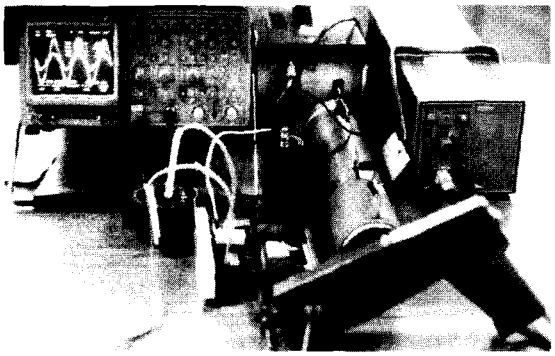


Fig. 10 The organization of experimental device for the boost type PFC circuit.

Fig. 11 shows the simulation waveform of input voltage and current by PSPICE TOOL. The equivalent circuit of PFC circuit by the PSPICE simulation is referred to in the parameters in Table 2.

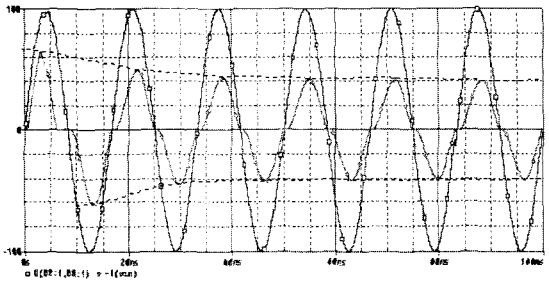


Fig. 11 The simulation waveform of input voltage and current.

Fig. 12 shows the input voltage and the current waveform of the CCM boost PFC circuit with average current mode controller.

Fig. 13 depicts the Fast Fourier Transform (FFT) measured at the input current of the boost type PFC circuit by digital oscilloscope. By the measurement of harmonics, we found that all harmonics after the 9th are so weak that they don't have any effect on the circuit.

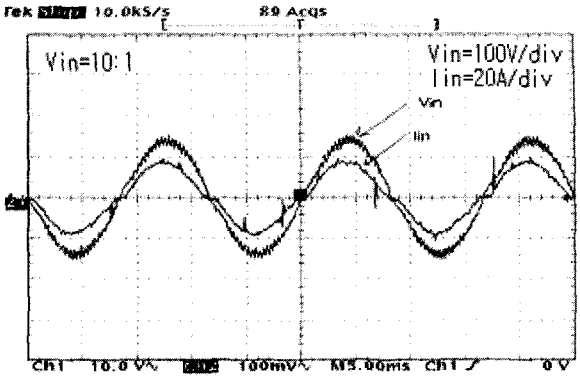


Fig. 12 Input voltage and current waveforms of average current mode controlled CCM boost PFC circuits.

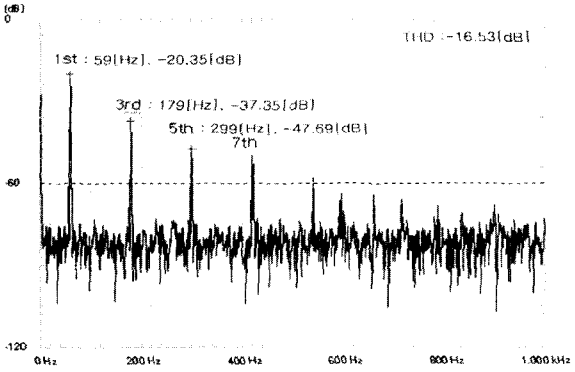


Fig. 13 *The analysis of FFT by input current after power* factor improvement.

Fig. 14 shows the PSPICE FFT analysis and experimental FFT analysis of the input current. The total harmonic distortion (THD) is -16.4[dB] and the improved power factor (PF) is 0.998.

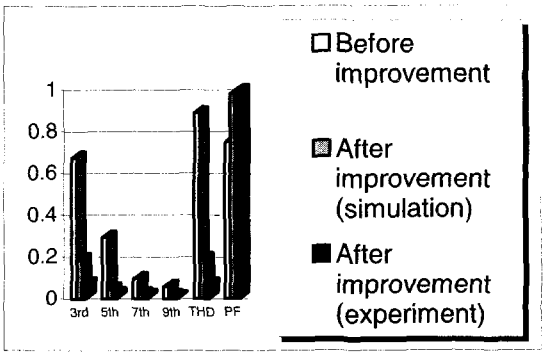


Fig. 14 FFT analysis of simulation and experiment.

Fig. 15 shows the compensation network of the voltage feedback loop.

Fig. 16(a) shows response characteristics of the designed boost type PFC circuit. The response characteristic is located in the high frequency area of the bandwidth to show pole variation of compensation network. The phase margin is 94.8° and the response time is not fixed.

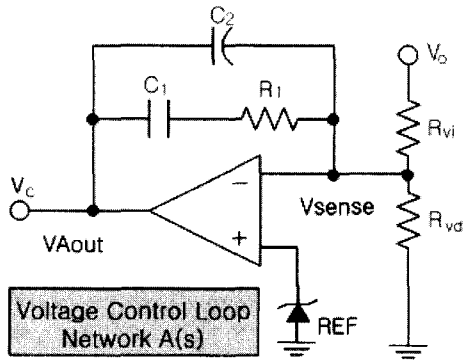
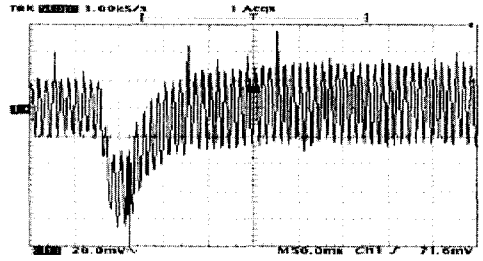


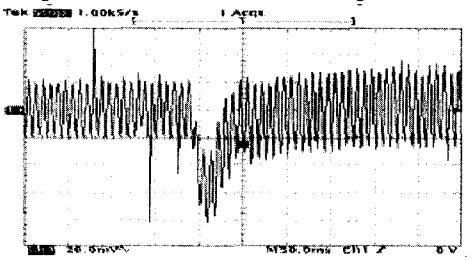
Fig. 15 Compensation network of the voltage feedback loop.

Fig. 16(b) shows transient response characteristic to load variation. The load variation is represented from 65% load to rated load (6A) with a response speed of 50[ms].

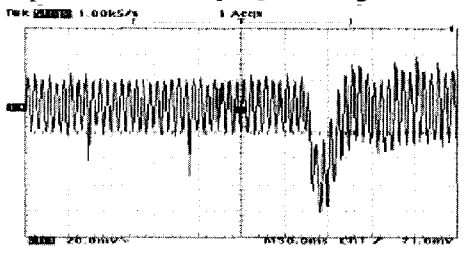
Fig. 16(c) depicts response characteristic of the designed boost PFC circuit. The response characteristic is located in the low frequency area of the bandwidth to show pole variation of compensation network. It has an improved response time of approximately 20[ms]. In addition, phase margin is 49.1° and crossover frequency is 10Hz.



(a) Compensator R1=56[kΩ] of voltage control loop;



(b) Compensator R1=100[kΩ] of voltage control loop;



(c) Compensator R1=150[kΩ] of voltage control loop.

Fig. 16 Transient response of experimental load variation on voltage control loop to the CCM boost PFC circuit.

6. Conclusions

In this paper, the regulation performance of output voltage and compensator has been analyzed to improve the transient response presented at CCM of the boost PFC circuit. The validity of the designed boost PFC circuit is confirmed by MATLAB simulation and experimental results of the 2 [kW] prototype converter.

The third and fifth harmonic components of the input current are decreased to -17[dB] and -27[dB], respectively. THD is -16.4[dB] and the improved PF is 0.998.

The response characteristic is located in the low frequency area of the bandwidth to show the pole variation of compensation network by design reference of voltage control gain. It has the improved response speed at about 20[ms]. The phase margin of the voltage control loop is represented by good characteristics at about 50°. Furthermore, the crossover frequency of the voltage control loop is 10Hz and the gain margin is 34[dB].

Experimental results of the CCM boost PFC circuit correspond with the theoretical concept well, and expect to have a wide application in many industrial fields.

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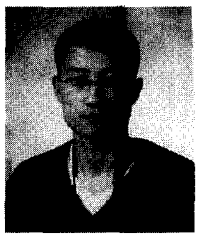

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