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Nonvolatile Semiconductor Memories Using BT-Based Ferroelectric Films

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ABSTRACT

Report ferroelectric memories based on 0.35 μm CMOS technology ensuring ten-year retention and imprint at 175°C. This excellent reliability resulted from newly developed BT-based ferroelectric films with superior reliability performance at high temperatures, and also resulted from robust integration schemes free from ferroelectric degradation due to process impurities such as moisture and hydrogen. The superior reliabilities at high temperature of ferroelectric memories using BT-based films are due to the random orientation by special bake treatments.

Key words : Ferroelectric, BT, Memory, Orientation, Reliability

1. Introduction

The remarkable growth of wireless communication systems such as mobile telephony, internet appliances, and personal digital assistants has been forecasted within a few year. The device performance such as low power consumption, fast operation, and small volume has been required for these systems. These requirements have accelerated the development of nonvolatile emerging memories such as Ferroelectric Random Access Memories (FeRAM), Magnetic Random Access Memories (MRAM), and Phase Change Memories (PCM). Among them, FeRAMs, which were already commercialized for low-density level, have been one of promising candidates for the new systems, due to their superior low-voltage and high-endurance operations to nonvolatile flash memories, and also their fast operation matched for static random access memories. However, one of crucial issues for realization of the commercial megabit FeRAM has been reliabilities, especially retention and imprint at high temperatures that should be upgraded.[1-3] For the reliability on the level of FeRAM commercialization, the selection of ferroelectric films is important. Furthermore, integration processes causing electrical degradation such as RIE, interlayer dielectrics, passivation, and packaging should be optimized.[4-6] In this paper, it is demonstrated that highly reliable packaged 1Mbit ferroelectric memories with 0.35 μm CMOS technology ensuring ten-year retention and imprint at 175°C have been successfully developed using $(Bi_{1-x}La_x)_4Ti_3O_{12}$ (BLT) films.

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2. BLT Films and Integrations

It was recently reported that BLT thin films doped with La in $Bi_4Ti_3O_{12}$ (BTO) were free from fatigue using Pt electrodes.[7] However, the electrical properties of the BLT films by a pulsed laser deposition should be further optimized for commercialization. BTO films with Bi-layered perovskite structure have been well known to have a strong anisotropic polarization. The directional polarization along a- or b-axis and c-axis is approximately 50 and 4 μC/cm^2, respectively.[8] Unfortunately, BTO films also have a strong tendency to have anisotropic crystallization along c-axis.[9] Therefore, the key capacitor process for superior electrical properties is on the randomly oriented crystallization. Newly developed BLT films were spin-coated using MOD sources. A special bake treatment at oxygen ambient (O_2 flow rate : 10 *l*/min) and 300°C for 5 min in a bake oven during BLT capacitor process provides the randomly oriented crystallization on Pt electrode as shown in x-ray diffraction measurement of Fig. 1, compared to normal bake processes without oxygen ambient. This treatment results in high polarization and excellent reliabilities even at low crystallization temperatures less than 650°C, compared to $SrBi_2Ta_2O_9$ (SBT) films with 800°C.[10,11] Analyses of Fourier Transform Infrared (FTIR) spectrometry show that special baking processes provide almost complete removal of organics remained in the BLT films, as shown in Fig. 2. It is believed that the free organics and the remained oxygen within films during the baking process provide increased nucleation sites on rapid thermal treatments up to 600°C and thus higher volume of the a- or b-axis oriented films during crystallization annealing at 650°C for 60 min. Consequently, we believe that it is important to eliminate the remained organics and diffuse oxygen into BLT films before nucleation and growth in order to

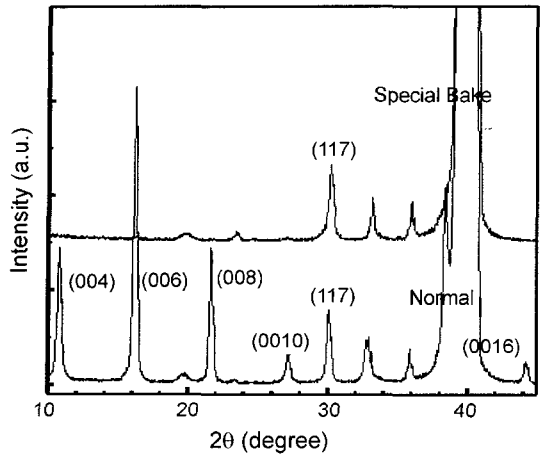

Fig. 1. The special baking treatments result in randomly oriented crystallization as shown in x-ray diffraction patterns.

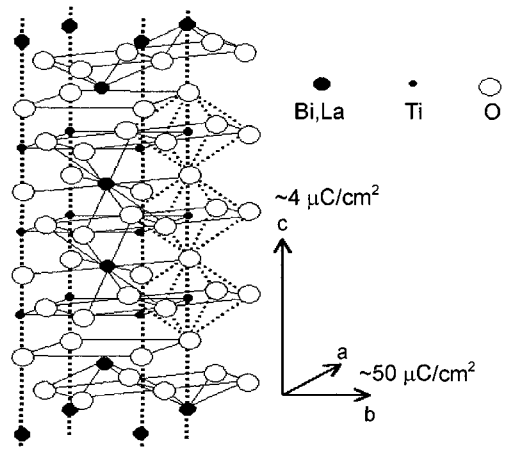

Fig. 3. Anisotropic polarization in an unit cell of $Bi_4Ti_3O_{12}$ doped with La showing higher remnant polarization in the direction of a or b-axis.

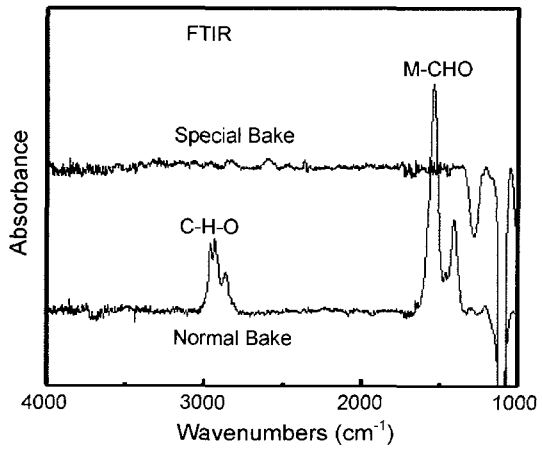

Fig. 2. Comparison results of FTIR analyses for specially and normally baked BLT films.

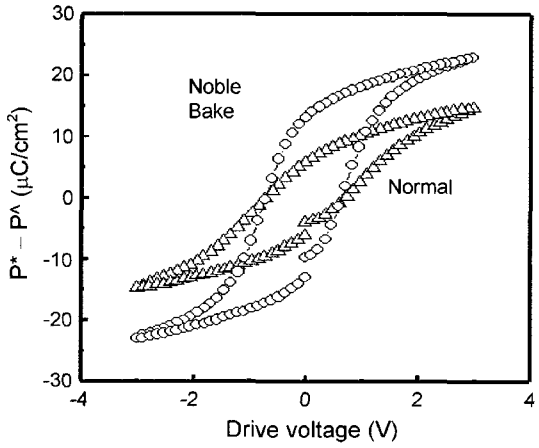

Fig. 4. The special baking treatments result in randomly oriented crystallization as shown in hysteresis loop measurements.

form the random oriented and dense BLT films. The oxygen effects on the randomly oriented crystallization during the special baking process are under investigation for publication.

The selection of capacitor materials is most important in terms of reliable performance of ferroelectric memories. One of advantages for the BLT over other ferroelectric films is on simplicity of cell schemes. For examples, BLT capacitors do not require such the complicate barriers in Capacitor Level Dielectrics (CLD) as preventing PZT films from chemical interactions with dielectrics. Additionally, BLT capacitors are not fatigued with Pt electrodes, while PZT films require the complicate metal-oxide electrodes to overcome the endurance. It was recently reported that BLT films were free from fatigue using Pt electrodes.[9] However, the electrical properties of the BLT films by a pulsed laser deposition, which are low polarization and low squareness in hysteresis loop, should be further optimized for the level of commercialization. BTO films with Bi-layered perovskite structure have been well known to have a strong anisotropic polarization. The polarization of BTO films significantly depends on the crystalline direction. The directional polarization along a- or b-axis and c-axis[10] is approximately 50 and 4 $\mu C/cm^2$, respectively, as shown in Fig. 3. Therefore, the key capacitor process for superior electrical properties is on the a- or b-axis oriented crystallization and/or the randomly oriented crystallization. Unfortunately, however, BTO films have a strong tendency to have anisotropic crystallization along c-axis.[11] The a- or b-axis oriented films have the highest polarization values, but there have been technical difficulties to make the epitaxial or highly oriented films with the a- or b-axis. It is believed that the remained oxygen within films during the baking process provide for increased nucleation sites on rapid thermal treatments up to 600°C and thus, higher volume of the a- or b-axis oriented films during crystallization annealing at 650°C for 60 min. The random crystalline of BLT film results in superior polarization to the c-axis oriented BLT films, which was processed by normal bake, as shown in Fig. 4, due to the anisotropic polarization of BLT films.

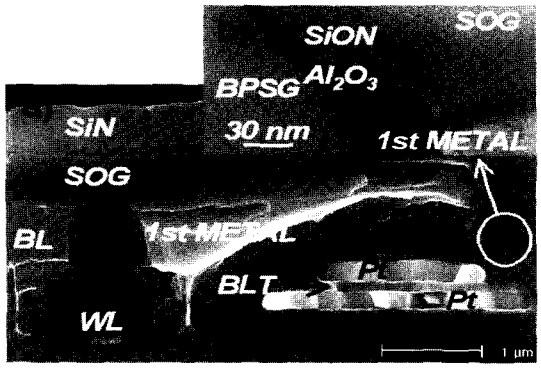

Fig. 5. (a) cross-sectional SEM photograph of a fully processed FeRAM cell and (b) cross-sectional TEM photograph showing alumina hydrogen barrier film on 1st metal line.

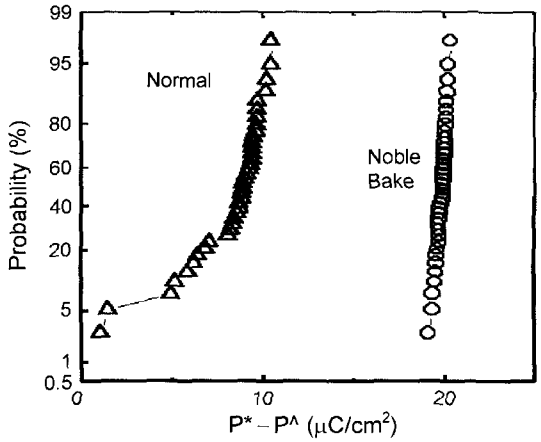

Fig. 6. Cumulative pulse polarization for full dies in 8-inch wafer of 32 K-array BLT capacitors after passivation.

3. Reliability Properties and Device Performance

Ferroelectric memories (FeRAM) have been fabricated on 0.35 μm CMOS technology as shown in Fig. 5. The detail integration process can be found in references.[12,13] Polarization changes (ΔP) for the capacitors using the randomly-oriented BLT films show higher remnant polarization and superior uniformity of full dies, compared to those processed by the normal bake as shown in Fig. 6, when fabricated up to passivation process. Consequently, the cost effective FeRAM using the well-developed conventional integration processes was successfully developed through the usage of newly developed BLT films. The sequence for retention and imprint tests was performed as follows : First, DATA "1" and DATA "0" were equally written in half of the cells, respectively. Second, the devices were stored at 175°C for some time. Third, DATA "1" and DATA "0" were written again for all cells, respectively. Finally, the V_{BL} distributions were measured by reading the DATA "1" and DATA "0" for all cells, respectively. The V_{BL} distributions of DATA "1" and DATA "0" in 4 K bits blocks, selected randomly from the 1 Mbit cells, are measured at Room Temperature (RT) and

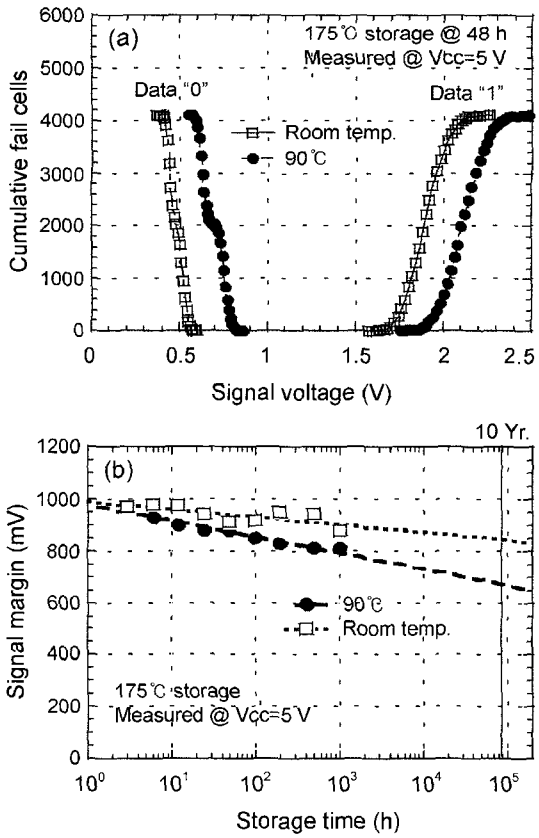

Fig. 7. Characteristics of memory performance using BLT capacitors. (a) distribution of bit line voltage measured at room temperature and 90°C after 48-h storage at 175°C and (b) sensing signal margin measured at room temperature and 90°C as a function of the storage time at 175°C.

90°C, and 5 V of operating voltage (Fig. 7(a)), after the 175°C storage for 48 h.

As increasing the measurement temperature, the signal margin of BLT memories is only slightly decreased. The signal margin, the difference between the highest signal voltage of Data "0" and the lowest one of Data "1", measured at RT is slightly larger than one at 90°C (Fig. 7(a)). The repeated measurements of the signal margin as a function of the data storage time at 175°C provide life estimations on the device level for 10-year retention and imprint as shown in Fig. 7(b). The extrapolation of the measured data at 90°C as well as at RT indicates enough signal-margin (670 mV) at 10 years. In the retention and imprint tests using 129 packages, no fail devices were observed after baking at 175°C for 1008 h. These excellent reliabilities are consequent to the newly developed BLT capacitors and the degradation-free integration schemes. The access time for the 2T/2C 1 Mbit FeRAM packaged with TSOP 32 pins was 100 ns at 5 V. The cycle time at 5 V and operating current is 170 ns and 25 mA, respectively. We believe that the feasibility for ferroelectric memories with higher density over 16 megabits is confirmed through this demonstration.

4. Summary

It was demonstrated that 1 Mbit FeRAMs with highly reliable characteristics at high temperature were successfully developed using 0.35 μm CMOS technology and newly developed BLT films. The superior reliabilities at 175°C operation temperature resulted from both the randomly oriented BLT films and the integration schemes free from process degradation of ferroelectric capacitors.

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