Circuit Modeling of 3-D Parallel-plate Capacitors Fabricated byLTCC Process

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A novel method of high speed, accurate circuit simulation in 3-dimensional (3-D) parallel-plate capacitors is investigated. The basic concept of the circuit simulation methods is partial element equivalent circuit model. The three test structures of 3-D parallel-plate capacitors are fabricated by using multi-layer low-temperature co-fired ceramic (LTCC) process and their S-parameters are measured between 50 MHz and 5 GHz. S-parameters are converted to Y-parameters, for comparing measured data with simulated data. The circuit model parameters of the each building block are optimized and extracted using HSPICE circuit simulator. This method is convenient and accurate so that circuit design applications can be easily manipulated.

Keywords : LTCC, integrated passives, capacitor model, circuit modeling

1. INTRODUCTION

In radio frequency integrated circuits (RFICs) and microelectronic circuits, passive components have important parts. With advances in technology, there is a continuous thrust toward higher levels of system integration and miniaturization. The technology is allowed for the transferal of passive components away from on top of a printed circuit board to within the substrate[1]. Embedded passives have many advantages such as improving packaging ratio and higher performance, reducing the use of print wire board real estate, eliminating assembly to board, minimizing solder joint failure and enhanced reliability[2].

In recent technology, low temperature co-fired ceramic process (LTCC) is desirable for radio frequency modules and multi-chip modules with embedded passive components. LTCC process give low resistance metallization using high conductivity metals such as gold and excellent high frequency characteristics using ceramic tape[3]. Integrating passive components such as resistors, capacitors, inductors and et al., are produced printing in the stack of metal or inserting capacitors tapes between ceramic tapes[4,5].

Among many passive elements in RF modules or MCM (multi-chip modules), parallel-plate capacitors and inter-digital capacitors are very widely used. For successful design of embedded parallel-plate capacitors, the library is necessary which contains circuit model parameters, capacitances, quality values and resonant frequency in the variation of plate width, length, and upper to lower distance, and etc.

In this paper, the circuit modeling methodology that based on partial elements equivalent circuits model is investigated. The parallel-plate capacitor test structures are fabricated in multi-layer LTCC process and their S-parameters are measured. To perform electro-magnetic (EM) simulations, the EM simulated data and the measured data is compared. In addition to, the circuit model parameters of the capacitor test structures, which are based on the using partial element equivalent circuits are extracted and optimized using HSPICE circuit simulator. After extracting the model parameters, the characteristic of different test structures is performed to verify the circuit model parameters.

2. TEST STRUCTURE DESCRIPTION

Test structures were fabricated in multi-layer LTCC process. All test structures were designed to have an upper and a lower conductor on different layers. Both conductors were separated by alumina substrate. The bottom conductor had a layout with angle to facilitate connections between via stacks connecting the layers. The complete test structure coupon is shown in Figure 1 and the geometry description can be seen in Figure 2. The test structures are categorized by size of plate. The plate is a perfect square. Each of the plate size of three test structures is shown in Table 1.

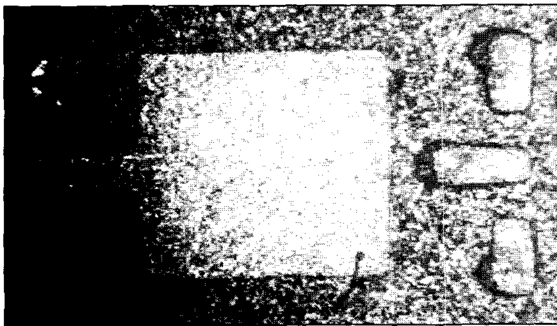


Fig. 1. The test structure image of parallel-plate capacitor.

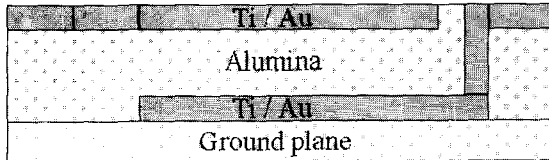


Fig. 2. The schematic diagram of test structure.

Table 1. The plate size of three test structures.

Size	Description
0.5 mm × 0.5 mm	Test Structure 1
1.0 mm × 1.0 mm	Test Structure 2
2.0 mm × 2.0 mm	Test Structure 3

3. PROCESSING AND MEASUREMENT

The LTCC structure was physically designed using integrated circuit design tools within the Cadence Virtuoso design environment. The design was fabricated at the National Semiconductor Corporation LTCC fabrication facility. The size of the completed coupon was approximately 22 mm × 18 mm.

The test structures were measured using standard network analysis techniques. Since very low loss metal was used in the manufacturing process, DC resistance measurements were unreliable and not used. For high-frequency measurements, an HP 8510C network analyzer was used in conjunction with a Cascade Microtech probe station and ground-signal-ground configuration probes. Calibration was accomplished using a standard substrate and utilization of the line-reflect-match (LRM) calibration method. The S-parameters were collected for each of the test structures between 50 MHz and 5 GHz.

4. MODELING SCHEME

The three structures of 3-d parallel-plate capacitors were physically designed and simulated within commercial field simulator. The simulated data was gathered for each test structure between 50MHz and 5 GHz.

A novel method of full 3-D parallel-plate capacitor modeling and simulation has been utilized. This method is based on the generation of passive circuit element models [6,7]. This approach first determines a set of fundamental circuit building blocks for the capacitors, and then test structures are designed, fabricated, and their S-parameters are measured up to a desired frequency. Afterwards, the electrical contribution to the overall capacitor response by individual building blocks is determined. Partial equivalent circuit models of each building block are then extracted using a hierarchical extraction procedure. These building block equivalent circuits are then used to construct a 3-D parallel-plate capacitor circuit that is geometrically comprised of the blocks. Simulation of the constructed circuit using the HSPICE circuit simulator provides an accurate prediction of the behavior of the test structure in a fraction of the time and using far fewer resources than the traditional EM/RF solution methodology[8]. The model of the test structure is then verified experimentally by comparing the predicted response with that measured directly from the manufactured structure.

The first step involved in the modeling procedure was a determination of what types of structures and geometries were to be modeled. As mentioned above, three test structures with different dimension were considered. Modeling of 3-D parallel-plate capacitor is very important to ensure that they function as intended at high frequencies. Parallel-plate capacitors modeling using the hierarchical technique required only four building blocks: a probe pad, plate, link, and the 3-D link block that composed of 2 link blocks. From the viewpoint of partial element equivalent circuit model, a plate of the smallest parallel-plate capacitor of the test structures is a standard equivalent circuit. So, to simulate

the other capacitors that have larger plate, we connect series and parallel circuit according to the size of the plate block. The standard partial element equivalent circuit is illustrated in Fig. 3. In addition, the mutual capacitance between two plate building blocks can be considered. But inductance, which had the plate, was ignored. As a result, mutual capacitance (C_{mut}) is added between the two plate building blocks.

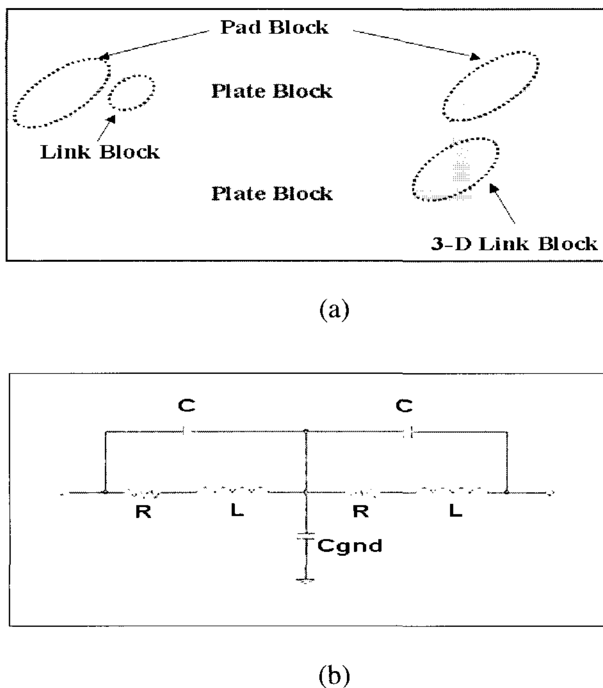


Fig. 3. Basic building block definition and its partial element equivalent circuit: (a) schematic diagram of basic building blocks (schematic) and (b) partial element equivalent circuit.

The equivalent circuits of building blocks are symmetry structures and the equivalent circuit of all basic building blocks was same structure. All test structure's parameter extraction and optimization that composed of each building block is achieved in conducting a capacitor.

The extraction of the circuit model parameters was achieved compared with measured and the modeled S-parameters by the HSPICE circuit simulator on Sun Ultra-Sparc workstation. Three test structures were optimized with respect to measured S-parameter, and their individual building block equivalent circuit model parameters were extracted. However, for capacitors, input admittance parameters (Y-parameters) are more informative than S-parameters. Therefore, Y-parameters for all test structures were calculated using S to Y conversion equations[9,10].

5. RESULTS AND DISCUSSION

A total of three 3-D parallel-plate capacitors were fabricated and S-parameters were taken. The measured S-parameters were used to extract the components of partial element equivalent circuit model. And EM-field simulation and circuit simulation were performed and compared with measured data each other.

Figure 4, 5, and 6 shows the measured versus optimized results of input admittance for test structure 1, 2, and 3. As seen in the plots, very good agreement has been obtained for both magnitude and phase of Y_{in} for all the test structures. As size of parallel-plate is increased, these structures behave as a capacitor in the different frequency ranges. It is due to inductive and other parasitic effects at the higher frequencies. And the size increased, capacitance also increased which is affected by parallel-plate size. As seen in the plots, Y_{in} magnitude is increased according to the increment of the plate size. The extracted circuit model parameters and the statistics are summarized in Table 2.

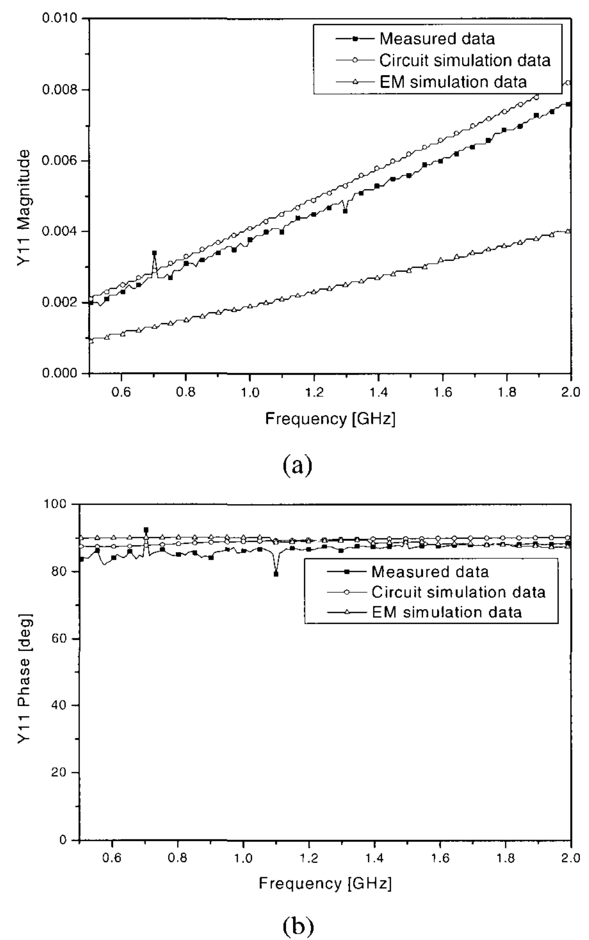
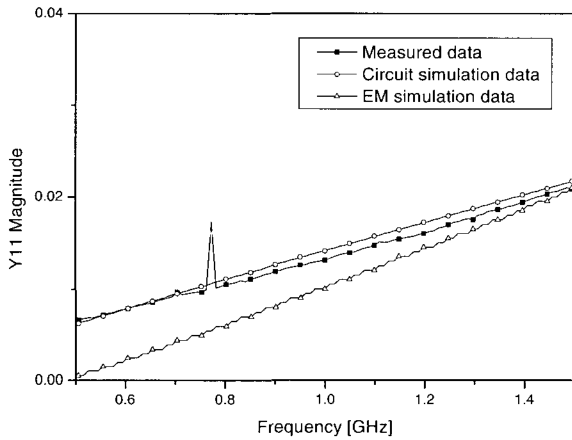


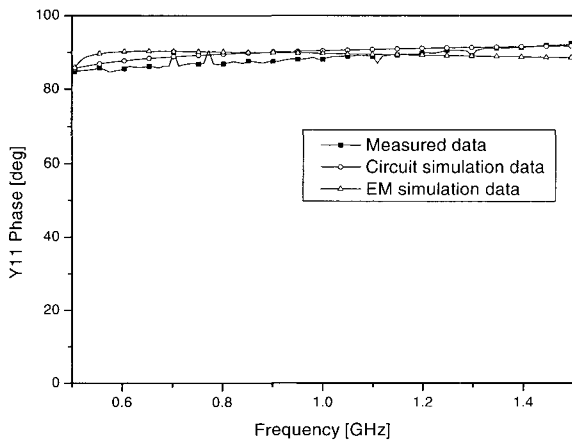
Fig. 4. Test structure 1 optimization results: (a) Yin (magnitude) and (b) Yin (phase).

Table 2. The optimized and extracted circuit model parameters.

	Test structure 1	Test structure 2	Test structure 3	Mean	Std_Dev
Rpad	5.60E-05	9.10E-05	1.00E-05	4.77E-05	3.44E-05
Lpad	5.57E-13	1.18E-10	5.52E-10	1.97E-10	2.43E-10
Cpad	1.20E-11	2.92E-11	1.60E-11	2.24E-11	9.98E-12
Rlink	1.56E-01	1.00E-02	1.00E-03	5.32E-02	7.13E-02
Llink	9.13E-07	7.08E-07	5.17E-07	6.23E-07	2.41E-07
Clink	3.28E-11	1.06E-11	5.02E-11	2.60E-11	1.92E-11
Rplate	1.45E-03	1.00E-03	1.09E-03	1.14E-03	2.12E-04
Lplate	8.46E-10	9.39E-10	4.67E-10	5.91E-10	3.78E-10
Cplate	7.83E-11	7.26E-11	2.20E-11	4.94E-11	3.02E-11
Cmut	1.64E-12	6.32E-10	9.99E-10	6.46E-10	4.59E-10
Cgnd	1.00E-13	1.00E-13	1.00E-13	1.00E-13	0

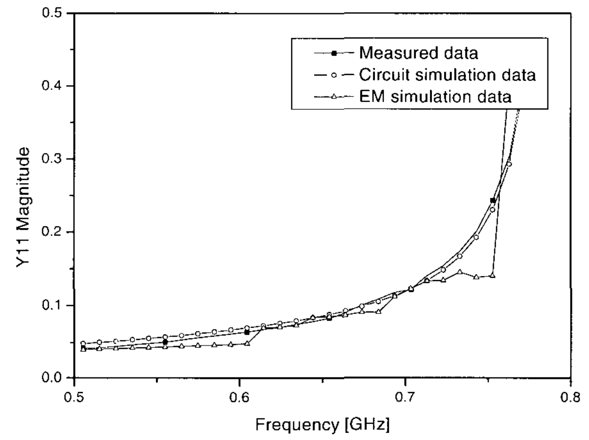


(a)

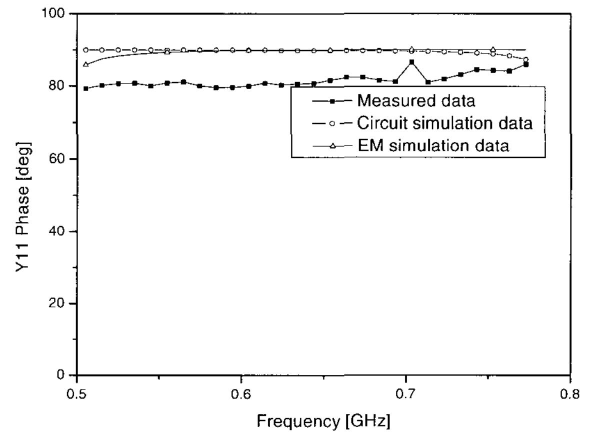


(b)

Fig. 5. Test structure 2 optimization results: (a) Yin (magnitude) and (b) Yin (phase).



(a)



(b)

Fig. 6. Test structure 3 optimization results: (a) Yin (magnitude) and (b) Yin (phase).

6. CONCLUSION

In this paper, a novel method of circuit modeling of 3-D embedded parallel-plate capacitors has been investigated using PEEC method. The three test structures of 3-d parallel-plate capacitors were fabricated in multi-layer LTCC process. In accordance with parallel-plate size, building blocks of test structure were composed.

The EM-field simulation performed to correlate simulation results with measured data for circuit modeling verification. The extraction of the circuit model parameters was achieved in the HSPICE circuit simulator.

This approach could potentially be extended to allow device designers to predict the performance and parametric yield of a given device. Furthermore, even a small number of test structures provide the relevant circuit model to allow accurate circuit modeling.

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