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Step-One in Pre-regulator Boost Power-Factor-Correction Converter Design

Mohamed Orabi†, and Tamotsu Ninomiya

Dept. of Electrical and Electronics Systems Eng., Kyushu University, Fukuoka, Japan

ABSTRACT

The output storage capacitor of the PFC converters is commonly designed for the selected hold-up time or the allowed output ripple voltage percentage. Nevertheless, this output capacitor is a main contribution factor to the PFC system stability. Moreover, seeking for a minimum output storage capacitor that assures the PFC desired operation under all condition, and providing the advantage of a small size and low cost is the main interesting target for engineering. Therefore, in this issue the design steps of the PFC converter have been discussed depending on three choices, output ripple, hold-up time, and stability. It is cleared that any design must take the minimum required storage capacitor for stability prospective as step-1 in deign, then apply for any other specification like hold-up time or ripple percentage.

Keywords : Power-Factor-Correction (PFC), stability, bifurcation, boost converter

1. Introduction

The harmonic reduction requirements imposed by regulatory agencies (IEC 1000-3-2) have accelerated interest in active Power-Factor-Correction (PFC) converter for switching power supplies. Many converter topologies have been proposed, which provide almost unity power factor line current. The most popular PFC converter is the boost type operating at continuous -conduction-mode CCM [1]. The boost PFC converter with average current mode control performs the advantage of perfect PFC such as the continuous current voltage [2, 3]. General operation of the boost PFC converter and the ability to shape the input current to trace the input is well described in details in many literatures [4-8]. However, the few have attempted to analyze the stability of this system. Most of literatures studied PFC converter based on linear methods, however PFC converter is a nonlinear circuit due to multiplier using and large duty cycle varia tion. In these prior linear regimes, the storage capacitor had been chosen depending on the required hold-up time or the allowed ripple percentage on the output voltage. However, the output capacitor was assumed as an infinity value to consider the output voltage as a constant value, and the time-varying input voltage was replaced by its root-mean-square (rms) value ignoring the time-varying effect in stability analysis. All these assumptions forced the nonlinear system to be linear and made the design far from straightforward. Then, the small and large signal equivalent circuits were derived and stability was discussed according to these assumptions [5, 6].

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† Corresponding Author : orabi@ckt.ees.kyushu-u.ac.jp
Tel: +81- 92-642-3938, Fax: +81-92-642-3957

Other new research have been taken in consideration the effect of PFC nonlinearity on the high frequency band [9, 10], however they do not detect the unstable phenomena on the low (line) frequency band. They have detected new fast scale instability phenomena in PFC converter circuit that affect the input power factor with a slightly decrease. On the other hand, new low-frequency instability phenomena in the PFC circuit have been introduced recently by the authors. These phenomena have been detected experimentally and verified by simulation [11, 12]. Moreover, a new nonlinear criterion has been proposed [13, 14]. It is cleared that these low frequency instabilities can break the PFC operation with getting down the power factor from unity to its half value.

From this new nonlinear viewpoint, it is emphasized that the storage output capacitor has a big contribution to the PFC system stability. Therefore, this paper highlights two important and basic points in PFC design. First is, choosing the minimum output capacitor, which gives the advantage of low size and cost. That is one of the most important targets for engineering. Second is, assuring system stability for the chosen output storage capacitor based on new nonlinear criterion.

In the first part, boost PFC converter operating at continuous-conduction-mode CCM operation is described. Second, a fast review of the prior linear regime with choosing the output storage capacitor depending on a hold-up time or an allowed ripple percentage is listed and its invalidity is highlighted from the stability point of view. Third, the instability phenomena in PFC boost circuit have been explained and their affected parameters have been pointed out. Fourth, nonlinear model is proposed to declare a new criterion for choosing the minimum required output storage capacitor that assures the boost PFC converter stability under all conditions. Lastly, the conclusion takes its place.

2. System Description

Boost PFC circuit consists of a main power circuit and a control circuit. The detailed circuit conFiguration parameters is shown in Fig. 1 The main feature of this system is the output bulk capacitance and using multiplier and two control loops, feedback and feed-forward, in

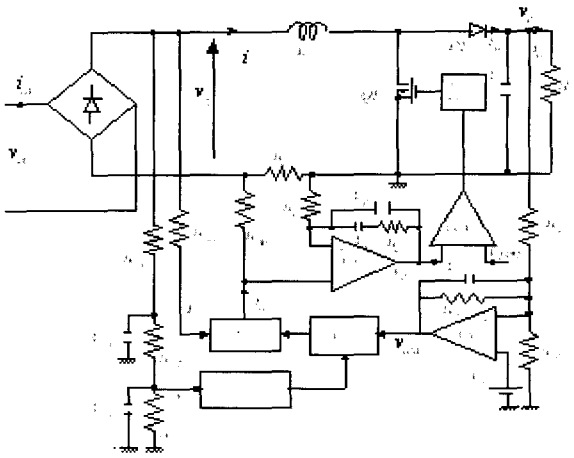


Fig. 1. Boost PFC with average-current-mode.

control circuit. That assures the non-linearity of the PFC converter. The main power circuit is constructed of full diode bridge circuit follows by boos dc/dc boost converter. The control circuit is the known used UC-3854A that operates at average current mode control [15]. The basic circuit of the converter consists of inductor L, diode $D1$, switch $Q1$ and capacitor C connected in parallel to load R.

The switch $Q1$ and the diode $D1$ are always in complementary operating states during the continuous -conduction-mode CCM operation. Essentially, it is a typical current- programmed boost converter, with the inductor current i_l chosen as the programming variable and the programming template I_{ref} being the input voltage waveform. Obviously the average input current is program mmed to track the input voltage, and hence the power factor is kept near unity. In addition, a feedback loop comprising a first-order filter serves to control the output voltage v_c. In brief, this done by adjusting the amplitude of the reference current I_{ref}, which is tracking the shape of the input voltage waveform v_{in}. Although a generalized discussion is introduced, a case study is analyzed. Here, three PFC example modules (100, 200, 500 watt) will review their design parameters using both linear and nonlinear analysis to compare the resultant performance.

The general specifications of the modules to be designed are variable ac input voltage 70-120 volts, variable input frequency 50-60 Hz, and required fixed dc output voltage 180 volts at the load output. The high lighted parts of the design are the storage capacitor value and the feedback voltage loop.

3. Previous Linear Design Regimes

The most concern is to determine the PFC system stability. Here, the linear regime of PFC converter is examined to prove its invalidity. Fig. 1 shows the boost PFC converter with average-current-mode control circuit. Stability of this circuit was explained by the prior researches using a simple linear model. They assumed a huge capacitance at the output terminal, replaced the time-varying input voltage with its rms value to ignore the nonlinear terms, and derived a small-signal equivalent circuit. In the small-signal equivalent circuit, the nonlinear system was linearized around an operating point and so the derived equivalent circuit had to be valid only for small deviations from that operating point. Therefore, it had a shortcoming to apply to all PFC operating points with the large variation in the input voltage. Results obtained in [4-6] showed that the total transfer function for the boost PFC converter with resistive load is as follows:

1) The converter power-stage transfer function of the small signal output voltage $\hat{v}_c$ to the small signal feedback voltage $\hat{v}_{vea}$ is given as:

$$\frac{\hat{v}_c}{\hat{v}_{vea}} = \frac{V}{\sqrt{KV_{vea}R}} \frac{R}{2+sCR} \tag{1}$$

2) The small signal feedback voltage to the small signal output capacitance voltage transfer function (Feedback equation) is:

$$\frac{\hat{v}_{vea}}{\hat{v}_c} = -\frac{R_{vf} / R_{vi}}{1 + sC_{vf}R_{vf}} \tag{2}$$

Then, the total system transfer function T_{total} is calculated from (1) and (2) as:

$$T_{total} = -\frac{VR_{vf}R / R_{vi}}{\sqrt{KV_{vea}R}} \frac{1}{(2+sCR)(1+sC_{vf}R_{vf})} \tag{3}$$

where, K can be assumed as a constant and it is expressed as:

$$K = \frac{R_{mo} / R_s}{v_{ff}^2 R_{vac}} \tag{4}$$

where, V, V_{vea}, R_{vf}, R_{vi}, R_{vd}, and C_{vf} are the DC value of the input voltage, the DC values of the feedback voltage, the feedback gain resistance, the feedback voltage divider resistors, and the feedback capacitance, respectively. From (3), it is clear that this system is stable for all cases and conditions, however new nonlinear phenomena have been encountered in these considered stable regions as will be explained in the next chapters.

3.1 100 watt model

For the 100 watt model, the design procedure steps in brief, are:

1- Choose switching frequency f_s equals to 100 KHz. (5)

2- Choosing the boost inductor that assures the operation in CCM. Then, the peak inductor current is:

$$I_{pk} = \frac{\sqrt{2}P_{in}}{V_{in,\min}} = \frac{\sqrt{2}*100}{70} = 2.02\ Amp \tag{6}$$

where, P_{in}, $V_{in,\min}$ are the input power (100 watt) and the minimum input voltage value (70 volt), respectively. Then, ripple inductor current is:

$$\Delta I = 0.3 * I_{pk} = 0.606\ Amp \tag{7}$$

So, the maximum duty cycle is:

$$D = \frac{V_c - V_{in,pk}}{V_c} = \frac{180 - \sqrt{2}*70}{180} = 0.45 \tag{8}$$

where, V_c, $V_{in,pk}$ are the DC output voltage and the peak of the minimum input voltage Then, the boost inductor is:

$$L = \frac{V_{in,pk} D}{f_s \Delta I} = \frac{\sqrt{2} * 70 * 0.45}{100000 * 0.606} = 735\ \mu H \qquad (9)$$

T hen, $700\mu H$ inductor can be chosen.

3- T he storage capacitor can be calculated depending on one of these required options:

i) Hold-up time:

$$C = \frac{2P_{out}\,\Delta t}{V_c^2 - V_1^2} = \frac{2*100*.01}{(180)^2 - (150)^2} \cong 200\mu F \qquad (10)$$

where, P_{out}, V_1, and Δt are the output power (100 watt assuming an ideal operation), the lowest permitted DC output voltage, and the required hold-up time, respectively.

ii) 10% ripple:

$$C = \frac{P_{out}}{2\pi f_r V_c V_{c,ripple}} = \frac{100}{2\pi * 120 * 180 * 18} \cong 40\mu F \qquad (11)$$

where, $f_r, V_{c,ripple}$ are the output ripple frequency (double line frequency) and the output ripple voltage value (ac voltage on the DC required output voltage), respectively.

4- S tability Discussion of Linear Model

T here are two loops in the PFC circuit, inner current loo[and outer voltage loop. Inner current loop deals with swi ching frequency and outer voltage loop deals with low (lin( ) frequency.

i) Design for the voltage loop:- This low response loop (low cut off frequency) is the main effected loop on these instability and so we will review its design in details. Choose divider resistors as $R_{vi} = 590K\Omega$, $R_{vd} = 10K\Omega$ to have 3 volt as reference voltage V_{ref}. Also choose a feedback capacitor $C_{vf} = 47nF$ to have a suitable feedback ac gain and suitable output voltage regulation. Then the unity gain frequency of the total voltage loop:

$$f_{vi} = \sqrt{\frac{P_{in}}{\Delta V_{vea} V_c R_{vi} C C_{vf} (2\pi)^2}} \qquad (12)$$

From (12), the unity gain frequency equals to $f_{vi} = 25Hz$ in case of using hold-up time and $f_{vi} = 56Hz$ in case of using 10% ripple. Therefore, the feedback resistor can be calculated to obtain cut off frequency within these unity gain frequency. A feedback resistor $R_{vf} = 183K\Omega$ (higher enough to assure a regulated output voltage) is chosen that gives a cut off frequency 18.5 Hz (less than line frequency to attenuate the effect of the output ripple on the input current distortion).

ii) Design of the current loop:- This design must be adjusted to have a near 45-degree phase margin by setting a zero at the loop crossover frequency. This design has a high relation to the switching frequency, but the detected instability here are at line frequency not switching frequency as will be explained later. Then, we will go over the details of the current loop design.

For the two design examples listed before, hold-up time and 10% ripple, the gain and phase margin of the PFC system have been plotted using (3) (depending of these linear regime). Fig. 2 shown the bode diagram for these two cases. It is cleared that both of them are stable with a sufficient phase margin (47 degree in hold-up time and 40 degree in 10% ripple case). This assures that any selected output capacitor between these two points will be stable also. However, later in the next chapters, unstable phenomena will be cleared inside these regions that were predicted as stable system by these linear regimes.

3.2 High watt models

Another two high watt modules, 200 and 500 watts, have been tested. Also, the storage capacitor chosen values are the highlighted part for design. From (10) and (11), it is cleared that, the relation between the choosing storage capacitor and the module power are linear. Hence, the choosing output storage capacitor is duplicated as the system power is duplicated in the two cases, hold-up time

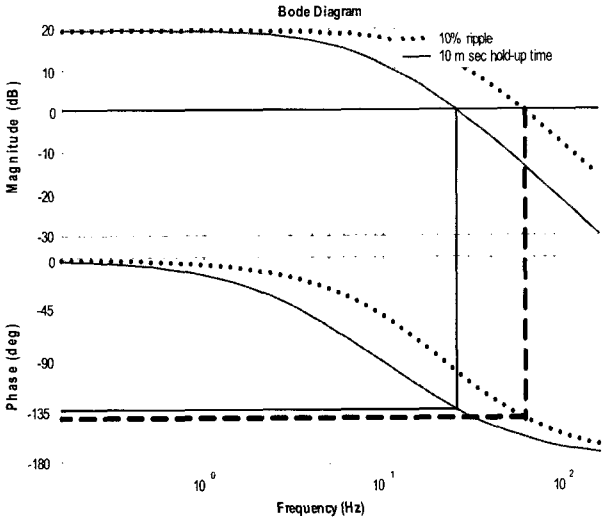


Fig. 2. Bode diagram of transfer function of the boost PFC converter from the linear analysis regime.

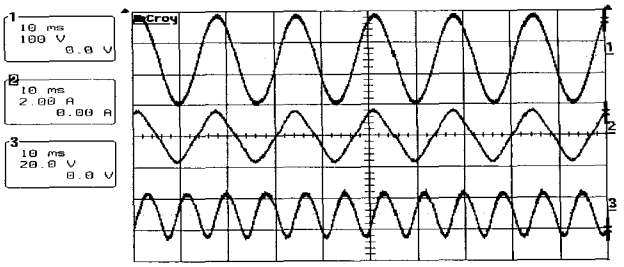
Table 1. Experimental circuit parameters values.

P_{in}	100 W	f_s	100 kHz
v_{in}	70 – 120 Vac	R_{ff1}	820 k ohm
V_c	180 Vdc	R_{ff2}	82 k ohm
f	50/60 Hz	R_{ff3}	22 k ohm
L	700 μH	C_{ff1}	100 nF
C	22 / 47 / 60 / 100 μF – 400V	C_{ff2}	470 nF
R (load)	324 ohm (100%) - 5% load	R_{vac}	680 k ohm
R_s	0.235 ohm	R_{mo}	2.7 k ohm
R_{vi}	590 k ohm	R_i	2.7 k ohm
R_{vd}	10 k ohm	R_z	24 k ohm
R_{vf}	183 k ohm	C_z	470 pF
C_{vf}	22 / 47 / 100 nF	C_p	68 pF

and 10% ripple. Therefore, the total system transfer gain will be the same as explained in (3).

4. PFC Converter Instability

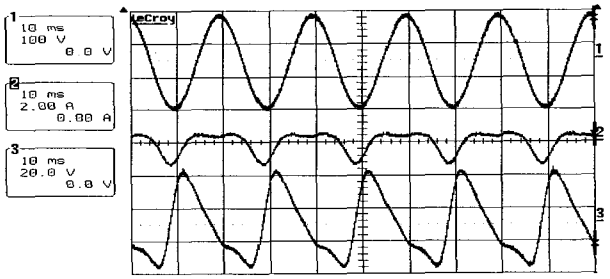
For the same PFC circuit shown in Fig. 1, a prototype has been constructed in laboratory. The design parameters used in experiment are shown in Table. 1. Many operating points have been tested experimentally to investigate the boost PFC converter. New unstable phenomena have been encountered in the PFC circuit, period doubling bifurcation and chaos. That has pointed out the limitation of the linear model. Here, a few operating points will be shown to explain the unstable phenomena. Output capacitance C = 60 μF (less than the required output capacitor for 10 msec hold-up time and more than the required capacitor for 10% output ripple)



1. The input voltage v_{in}. 2. The input current i_{in}.

3. The output ripple voltage Δv_c.

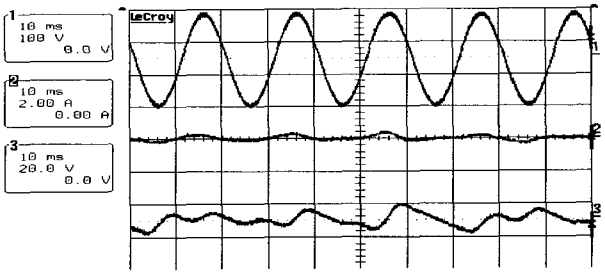
Fig. 3. The input voltage, input current, output ripple voltage response at full load in stable case (Experimental result).



1. The input voltage v_{in}. 2. The input current i_{in}.

3. The output ripple voltage v_c.

Fig. 4. The input voltage, input current, output ripple voltage response at 50% load in period doubling bifurcation case (Experimental result).



1. The input voltage v_{in}. 2. The input current i_{in}.

3. The output ripple voltage v_c.

Fig. 5. The input voltage, input current, output ripple voltage response at 10% load in chaotic instability case (Experimental result).

and feedback capacitance, C_{vf} = 47 nF (same as used in calculation) have been engaged as one comparison point to the prior linear regime. Figures 3, 4 and 5 show three different operating modes, stable, period doubling bifurcation and chaos, which are encountered in the PFC

circuit for these chosen operating parameters. First, in case of a stable operation, the input current, i_{in} is periodically, sinusoidal, and in phase with input voltage, v_{in} as shown in Fig. 3. In this case, the test parameter is full load. The output voltage ripple, Δv_c is periodic with double frequency of the input line voltage. The resultant power factor is very high (0.98). Second, Fig. 4 shows the unstable period-2 phenomena. The operating parameters are the same as the stable case in Fig. 3 with only decreasing the load to 50%. The output voltage ripple period moves to be double of the stable case period. The power factor is lessened to a low value (0.67), which is worse than the conventional capacitor-diode rectifier. A chaotic phenomenon appears clearly in Fig. 5 with non-repeating waveforms at C = 47μF, C_{vf} = 47nF, and 10% load. As a result, this system is globally unstable. Also, it is cleared that, the old design regime fails to perform the global system stability. Therefore, we are in need for a new design criterion that can offer a good design, which can assure global system stability. Besides, the contribution of the load parametric is made clear, where PFC converter becomes more susceptible to instability as the operation moves towards light loads.

5. Nonlinear Analysis Criterion

In this section, the boost PFC converter is studied from the nonlinearity viewpoint. From a practical aspect, a general design method must be driven to check the whole system stability under all operating conditions. The whole system stability can be proved by checking the stability of every operating point under different operating conditions using experiment and/or simulation, which needs a lot of effort and time. Moreover, calculating the minimum required output capacitor to achieve PFC converter stability under different operating condition is practically a major target aimed by designers. Hence, a new criterion is proposed here for boost PFC converter stability. The nonlinear criterion based on the instantaneous power equation of the boost PFC converter, which is given at the MOSFET switch *Q1* (Fig.1) by:

$$v_c(t)C\frac{dv_c(t)}{dt}+\frac{v_c^{\,2}(t)}{R}=v_{sw}(t)i_l(t) \tag{13}$$

$$v_{sw}(t)=v_g(t)-L\frac{di_l(t)}{dt} \tag{14}$$

where, v_c and v_{sw} are the output capacitor voltage and the voltage across the MOSFET switch. The feed-forward voltage signal obtained from a second-order filter can be assumed to be constant. Therefore, the reference current (multiplier output) I_{ref} can be calculated as:

$$I_{ref}(t)=\frac{(v_{vea}(t)-1.5)I_{ac}(t)}{v_{ff}^{\,2}(t)}=\frac{(v_{vea}(t)-1.5)v_g(t)}{v_{ff}^{\,2}(t)R_{vac}}$$

$$=K_1(v_{vea}(t)-1.5)v_g(t) \tag{15}$$

$$\text{where, } K_1=\frac{1}{v_{ff}^{\,2}(t)R_{vac}} \tag{16}$$

where, v_{vea}, I_{ac}, v_{ff}, v_g, and R_{vac} are the feedback voltage, the instantaneous programming current sensing the rectified voltage, the feed-forward voltage, the rectified input voltage, and the programming resistance, respectively. The factor 1.5 is used for gaining the feedback as explained in the used control circuit UC 3854-A [15]. Towards the simplification of this nonlinear model, an assumption is introduced that can simplify the solution. The current error amplifier gain is assumed to be very high, and then the following equation for the inductor current is obtained:

$$i_lR_s=I_{ref}R_{mo} \tag{17}$$

where, R_s and R_{mo} are the sense resistance and the multiplier resistance, respectively. Substituting (15) and (16) into (17), the inductor current is expressed as:

$$i_l(t)=\frac{R_{mo}}{R_s}I_{ref}(t)=K(v_{vea}(t)-1.5)v_g(t) \tag{18}$$

$$\text{where, } K=\frac{R_{mo}/R_s}{v_{ff}^{\,2}(t)R_{vac}} \tag{19}$$

Then, substituting (14) and (18) into (13), the main equation of the simplified nonlinear model, power stage equation, is developed as:

$$v_c(t)\left(\frac{d v_c(t)}{d t}+\frac{v_c(t)}{RC}\right)= \frac{V^2K}{C}(1-\cos(2\omega t))(v_{vea}(t)-1.5)-\frac{\omega LK^2V^2}{C} \sin(2\omega t)(v_{vea}(t)-1.5)^2-\frac{K^2LV^2}{C} (1-\cos(2\omega t))(v_{vea}(t)-1.5)\frac{d v_{vea}(t)}{d t} \quad (20)$$

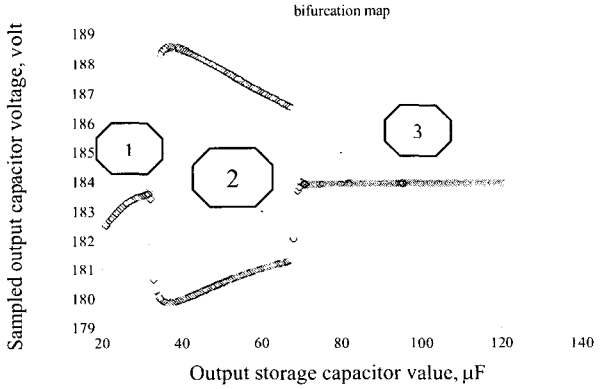
Also, the feedback voltage error amplifier equation is expressed as:

$$\frac{d v_{vea}(t)}{dt}+\frac{v_{vea}(t)}{C_{vf}R_{vf}}=\left(\frac{1}{R_{vf}C_{vf}}+\frac{R_{vd}+R_{vi}}{R_{vd}R_{vi}C_{vf}}\right)V_{ref}-\frac{v_c(t)}{R_{vi}C_{vf}} \quad (21)$$

where, $V_{ref}=3\ volt$ and $v_g(t)=\sqrt{2}V|Sin\omega t|$. (20) and (21) construct the main equations for the PFC boost converter nonlinear model. The performance of the PFC converter can be investigated through this nonlinear model. Then, the minimum required output capacitor for stability can be calculated using (20) and (21) as will be explained in the next section.

6. Output Capacitor Design

The contribution of the output storage capacitor on the system stability has been made clear through the experi ment. In this section, a new criterion to determine the minimum required output capacitor for system stability is proposed using the two nonlinear equations listed (20) and (21). The proposed design criterion is based on bifurcation analysis. In the bifurcation analysis, the output voltage sampled over half line period is chosen as the judgment signal for stability. As mentioned before, in stable operation, the output voltage is periodic with double line frequency (120/100 Hz). Then, choosing any point and checking its value every half line period gives the same value for stable operation (period-1 operation). That results in one line for different operation values. On the other hand, in unstable operation, period doubling bifurcation, the output voltage is periodic with line frequency (60/50 Hz). Hence, two lines are appeared in period-2 bifurcation case. Therefore, choosing the output voltage on the storage capacitor as an indicator for the system stability is an excellent detection. To determine the minimum required output capacitor for stability, the bifurcation diagram is drawn between the sampled output voltage every half-line period and the output storage capacitor. Solving (20) & (21) using a FORTRAN program with applying voltage sampling and changing the storage capacitor value, the bifurcation map is provided. Figure 6 shows the bifurcation map for the boost PFC to explain the effect of the storage capacitor. The chosen parameters for these operating points are 100 volts, 60 Hz, 10% load, and feedback capacitor of 47 nF. From the result in Fig. 6, it is cleared that, at higher values of the storage capacitor, one fixed value of the output voltage is obtained, fixed line. That means that the system is periodic every 120 Hz. Hence, the PFC system stability is assured. Beside, at medium values of the output storage capacitor, the system moves to have two values of the output voltage. This means that, the output voltage period is doubled and so the resultant system is unstable. Moreover, at very lower values of the output storage capacitor, the system is stable but with non-sinusoidal input current (high distorted area) due to the high output ripple as the used output capacitor is very small. At these regions, the sampled output voltage indicator gives lower values as shown in the same Figure. Figures 7, 8, and 9 show the waveforms of the input voltage v_{in}, the input current i_{in}, and the output capacitor voltage v_c in each case of these three operating



1. non-sinusoidal current area 2- unstable area 3-stable area

Fig. 6. Bifurcation map between the sampled output voltage and storage capacitor.

mod s, stable, period doubling bifurcation instability, and high distorted area, respectively. Figure 7 shows the stabl e operation for one point inside region-3, C = 100 μF. Figu e 8 shows the unstable operation where the output volt ge changes its periodic frequency to its half. Then, thro gh the feedback loop, the output voltage distorts the inpu current resulting in low power factor. For this result in F g. 7, the chosen operating point inside region-2 is C = 60 μF. Then, the data from output capacitor, C = 22 μF, high distorted area, is provided to give an example of regi n-1 operating mode as shown in Fig. 9. The most imp rtant region is the borderline between stable and unst ble operation, where the minimum capacitance is chos en. Besides, the PFC converter stability must be inve tigated at light load becomes it becomes more susc ptible to the instability as the operation move tow rds light loads. In this paper, light load 10% is assu ned for the program to determine the minimum requ red output capacitor value, which assures the system stab lity under all operating conditions. Figure 10 shows the bifurcation map for 100 watt module at the same prev ous selected parameters. It is cleared that 70 μF stor ge capacitor can satisfy for all loads stability. Fig. 11 s ows the same procedure for 200 watt, which results in 1 10 μF as a minimum storage capacitor to assure the syst m stability. Lastly, for 500 watt module, a 350 μF is d clared as a minimum storage capacitor as shown in Fig. 12. Therefore, as the module power increases, the requ red minimum storage capacitor increases also. This pow r relation is the same as mentioned in linear models, but he linear model has the limitation for the ability to cho se minimum required capacitor for stability purpose.

A s a conclusion, Fig. 13 shows a comparison between thes linear and nonlinear models for the three tested mod ules (100, 200, and 500 watt). The first columns of each watt module are the 10% ripple chosen module (line ar analysis). The last columns of each watt module are the 10 m sec hold-up time (linear analysis). The mid le columns of each watt module are the minimum requ red storage capacitor to achieve system stability. Then, the first linear design (10% ripple) is practically unst ble however it was deigned to be stable depending on the l near model (Fig. 2 shows it as stable system and Fig. 6 and Fig. 8 shows it as one unstable operating point. This proves the limitation of the linear analysis. The second linear design (10 m sec hold-up time) appears as st

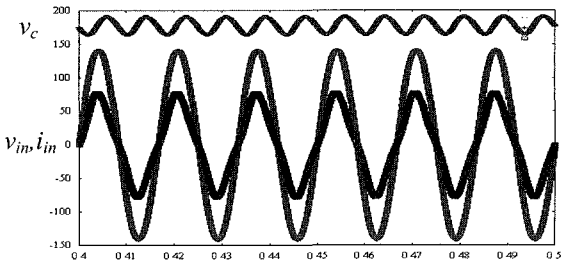


Fig. 7. Input voltage, input current, and output voltage ripple response in stable case (area 3 in Fig. 6).

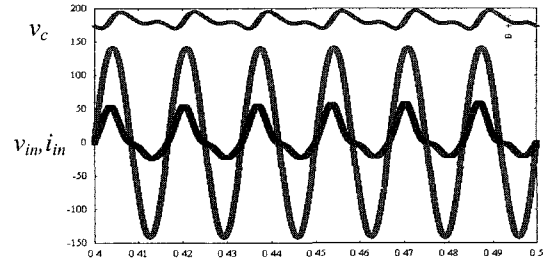


Fig. 8. Input voltage, input current, and output voltage ripple response in period-2 case (area 2 in Fig. 6).

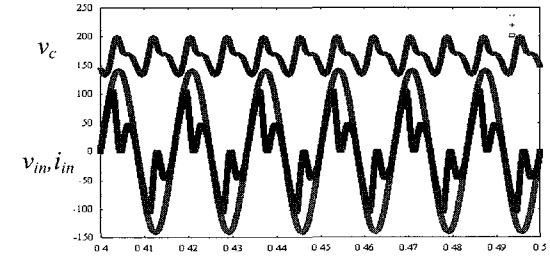


Fig. 9. Input voltage, input current, and output voltage ripple response in high distorted current case (area 1 in Fig. 6).

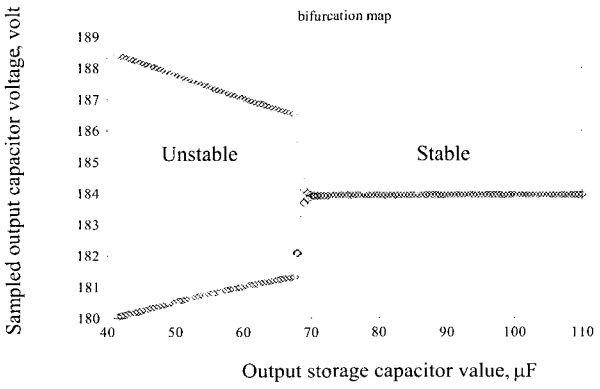


Fig. 10. Bifurcation map between the output voltage and storage capacitor at 100 watt module.

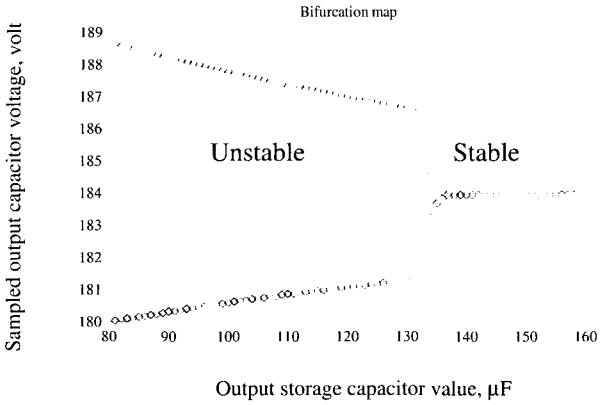


Fig. 11. Bifurcation map between the output voltage and storage capacitor at 200 watt module.

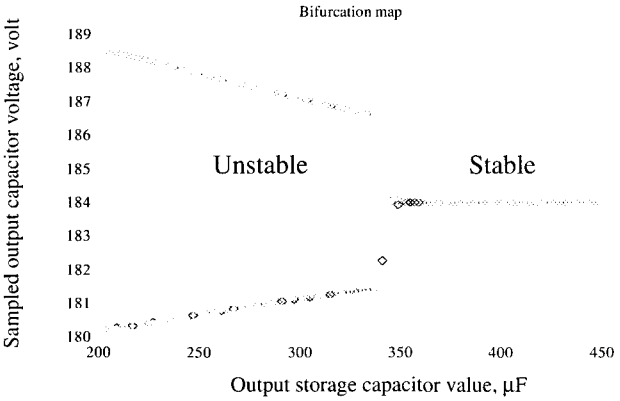


Fig. 12. Bifurcation map between the output voltage and storage capacitor at 500 watt module.

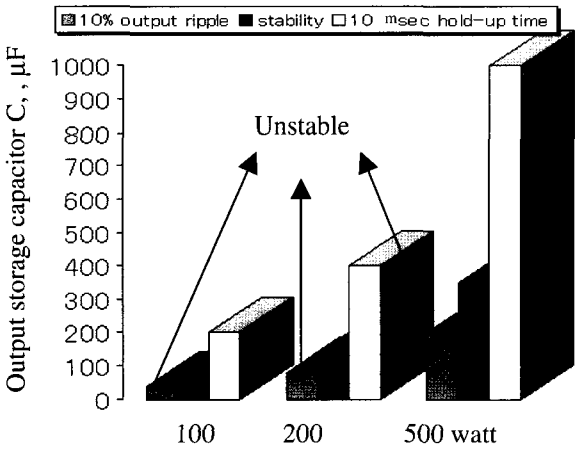


Fig. 13. The required storage capacitor at every module for every design method and stability target.

-able system but this depending on the chosen hold-up time. Therefore, in case of choosing a lower hold up time, the system can be unstable. It is important to make clear that the minimum required capacitor must be determined depending on the stability at first and then taking on the consideration the other required specification like the percentage of the output ripple or the hold-up time. If the calculated required output capacitor depending of the required hold-up time or the allowed ripple percentage is higher the designed minimum output storage capacitor for stability, then there is no problem of using it. Otherwise, if it is lower than the designed minimum output storage capacitor for stability, the designed output capacitor must be used to assure system stability.

7. Conclusions

New unstable phenomena have been detected in the PFC converter, period doubling bifurcation and chaos. An accurate comparison between the prior linear and nonlinear methods is introduced to prove the limitation of the linear regimes. A proposed nonlinear method is proved to solve the stability target and to determine of the minimum required storage capacitor that assures system stability under all load conditions. It is cleared that choosing the output capacitor must be judged depending on the stability condition as step 1. Then, taking in the consideration the other required specification like the output ripple percentage or the hold-up time. This new criterion to determine the minimum output storage capacitor for PFC converter stable operation provides an important methodology for engineering designer, having the advantage of low cost and small size output capacitor.

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Mohamed Orabi was born in Kena, Egypt, in 1974. He received the B.S. and M.S. degrees in electrical engineering from Elmi nia University, Elminia, Egypt, in 1996, and 2000, respectively. Since 1998 he has been associated with the Department of Electrical Engineering, Faculty of Enginee ring in Aswan, South Valley University, first as Administrator and since 2000 as Research Assistant. Since the 2001, he has been a Ph. D student in the Department of Electrical and Electronic Systems Engineering, Kyushu University, Japan.

His research interests include developing and designing of switched-mode power converters and their application to power factor corrections, stability problems, nonlinear phenomena, chaos, and period doubling bifurcation.

He published more than 20 papers. He received The 2002 Excellent Student Award of The IEEE Fukuoka Section, The Best Paper Award of 28th Annual conference of the IEEE Industrial Electronics Society 2002 and The IEEE_IES Student Grant from 2003 IEEE International Symposium on Industrial Electronics.

Tamotsu Ninomiya received the B.E., M.E., and Dr.Eng. degrees in electronics from Kyushu University, Fukuoka, Japan, in 1967, 1969, and 1981, respectively. Since 1969 he has been associated with the Department of Electronics, Kyushu University, first as Research Assistant and since 1988 as Professor. Since the re-organization in 1996, he has been a Professor in the Department of Electrical and Electronic Systems Engineering of the Graduate School of Information Science and Electrical Engineering.

He has been a specialist in the field of power electronics, inclu ding the analysis of switching power converters and their electro magnetic interference problems, the development of noise suppr ession techniques, and the piezoelectric-transformer converters.

He served as a member of Program Committees for PESC and APEC, as Program Vice Chairman for 1988 PESC, and General Chairman for 1998 PESC. He was a member of the Admi nistrative Committee of IEEE PELS from 1993 through 1998. In January 2001, he was awarded as IEEE Fellow.