A Highly Linear CMOS Baseband Chain for Wideband Wireless Applications

Seoung-Jae Yoo and Mohammed Ismail

The emergence of wide channel bandwidth wireless standards requires the use of a highly linear, wideband integrated CMOS baseband chain with moderate power consumption. In this paper, we present the design of highly linear, wideband active RC filters and a digitally programmable variable gain amplifier. To achieve a high unity gain bandwidth product with moderate power consumption, the feed-forward compensation technique is applied for the design of wideband active RC filters. Measured results from a 0.5 µm CMOS prototype baseband chain show a cutoff frequency of 10 MHz, a variable gain range of 33 dB, an in-band IIP3 of 13 dBV, and an input referred noise of 114 µVrms while dissipating 20 mW from a 3 V supply.

Keywords: Baseband chain, VGA, active RC filter, feed-forward compensation.

Manuscript received Feb. 25, 2004; revised May 4, 2004.

Seoung-Jae Yoo (phone: +1 614 292 2977, email: yoo_seoungjae@hotmail.com) and Mohammed Ismail (email: Ismail@ee.eng.ohio-state.edu) are with Analog VLSI Lab, Department of Electrical Engineering, The Ohio State University, USA.

I. Introduction

The past few years have witnessed a rapid growth of wireless standards for a wide channel bandwidth and high data rate capability such as Wideband Code Division Multiple Access, IEEE projects 802.11a and b, and so on. Cost considerations favor integrated CMOS transceiver realizations using direct conversion radio architectures. In such architectures, channel selection is done after a down conversion from RF to DC by means of highly linear, wide-bandwidth integrated low pass filters. Active RC filters are typically preferred due to their higher linearity compared to Gm-C (transconductance-C filter) implementations.

Unfortunately, the need to drive resistive loads makes an active RC wideband design a challenging task. Typically, large bias currents are used to achieve a high op-amp open-loop unity gain frequency [1]. However, the use of the above mentioned standards in battery operated portable applications places a great premium on device power consumption [2]. Therefore, novel circuit techniques are required that enable the realization of highly linear wideband active RC filters with moderate power consumption.

In this paper, we introduce the use of feed-forward compensated amplifiers in a wideband filter design. We implemented a fourth-order low-pass Butterworth filter with a cut-off frequency of 10 MHz by cascading two Tow-Thomas biquads. Additionally, we realized a variable gain amplifier (VGA) with a gain range of 33 dB. For DC offset cancellation, we implemented a first-order high-pass filter with a cutoff frequency of 30 kHz at the first stage of the baseband chain. The measured results of a prototype CMOS implementation in a 0.5 µm technology indicate the possible utility of the designed filter in an IEEE 802.11a analog receiver baseband chain.

II. Feed-Forward Compensated OTA

An accurate operation of active RC filters requires a large gain-bandwidth amplifier [3]. Conventionally-used two-stage operational amplifiers employ capacitive frequency compensation and hence suffer from a limited gain-bandwidth. In contrast, a feed-forward compensated amplifier is capable of simultaneously achieving a large gain-bandwidth product and open loop gain [4]. Figure 1(a) shows a simplified block diagram of the feed-forward compensated operational transconductance amplifier (OTA), and Fig. 1(b) shows a fully differential feed-forward compensated OTA. Transistors $M_1 - M_5$ shown in Fig. 1(b) constitute the input stage of the main amplifier, which is equivalent to the first stage shown in Fig. 1 (a). $M_{f1} - M_{f3}$ in Fig. 1(b) constitute the feed-forward amplifier, which is equivalent to the feed-forward stage in Fig. 1(a). The shared output stage, $M_6 - M_9$ in Fig. 1(b), is equivalent to the second stage in Fig. 1(a).

If we assume each stage in Fig. 1(a) to have a single pole, then each stage is modeled in [4] and [5] as

$$A_{in}(s) = \frac{A_1}{1+\frac{s}{\omega_{p1}}}, A_{out}(s) = \frac{A_2}{1+\frac{s}{\omega_{p2}}}, A_f(s) = \frac{A_f}{1+\frac{s}{\omega_{pf3}}}. \quad (1)$$

Here $A_{in}(s)$, $A_{out}(s)$, and $A_f(s)$ are the transfer functions of the first, second, and feed-forward stages of the OTA shown in Fig. 1(a), respectively. A_1, A_2, and A_f are the DC gains of $A_{in}(s)$, $A_{out}(s)$, and $A_f(s)$, respectively, and ω_{p1}, ω_{p2}, and ω_{pf3} are the poles of $A_{in}(s)$, $A_{out}(s)$, and $A_f(s)$. The transfer function of Fig. 1(a) can be derived as

$$\begin{aligned} V_{out}/V_{in} &= A_1A_2 \Big/ [(1+\tfrac{s}{\omega_{p1}})(1+\tfrac{s}{\omega_{p2}})] + A_f \Big/ (1+\tfrac{s}{\omega_{pf3}}) \\ &= \frac{A_1A_2(1+\frac{s}{\omega_{pf3}}) + A_f(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{pf3}})}. \end{aligned} \quad (2)$$

If the second stage pole, ω_{p2}, and the feed-forward stage pole, ω_{pf3}, are both designed to have the same value, the transfer function now becomes

$$\frac{V_{out}}{V_{in}} \approx \frac{A_1A_2 + A_f\left(1+\frac{s}{\omega_{p1}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}. \quad (3)$$

From the above transfer function, the open loop gain and left half plane (LHP) zero are

$$\text{Open loop gain} \approx A_f + A_1A_2 \quad (4)$$

$$\text{LHP zero} \approx -\omega_{p1}\left(1+\frac{A_1A_2}{A_f}\right). \quad (5)$$

If the LHP zero is designed to be equal to the second pole, ω_{p2}, (3) becomes

$$\frac{V_{out}}{V_{in}} = \frac{(A_1A_2 + A_f)}{\left(1+\frac{s}{\omega_{p1}}\right)}, \quad (6)$$

which is a one-pole amplifier. In this case, a large phase margin is obtained without sacrificing the gain-bandwidth (GBW) product [4]. Also, compared to a Miller compensated two-stage amplifier, the open loop gain is increased by A_f, the gain of the feed-forward stage. Moreover, the feed-forward compensation scheme leaves the dominant pole unchanged, thus realizing a larger 3 dB bandwidth.

The compensation scheme used in Fig. 1(b) employs two feed-forward amplifiers, M_{f1} and M_{f2}, to create LHP zeros. The positive phase shift of LHP zeros is used to compensate the negative phase shift due to the poles. Since the OTA in Fig. 1(b) does not use any Miller capacitor, the dominant pole is not pushed to lower frequencies, and a higher unity gain bandwidth product can be achieved. For proper operation of the feed-forward compensation scheme, the signal polarity at the output of the second and feed-forward stages should be same. To keep the same signal polarity, V_{in+} is applied to M_{f2} and M_1, and V_{in-} is applied to M_{f1} and M_2. Two common mode feedback amplifiers, CMFB1 and CMFB2, are used to ensure the common-mode voltages of the input and output stages.

An imperfect cancellation between the second pole and the LHP zero results in the decrease of the phase margin. To minimize the effect of the imperfect pole-zero cancellation, the cancellation must occur at high frequencies and the second and feed-forward stages should not include a non-dominant pole until the arrival of the overall unity gain bandwidth product [5]. The second and feed-forward stages must be optimized for a high bandwidth, and the first stage needs to be designed to have a high gain and small load capacitance. The transconductances of the individual gain stages are determined based on (4) and (5). For example, the transconductance of the second stage can be determined after the LHP zero is decided because the second pole should be equal to the LHP zero for the pole-zero cancellation.

The open loop gain of Fig. 1(b) can be approximated as

$$\text{open loop gain} = \frac{g_{m6}}{(g_{dsf1}+g_{ds6}+g_{ds7})}\left(\frac{g_{mf1}}{g_{m6}} + \frac{g_{m1}}{(g_{ds1}+g_{ds3})}\right), \quad (7)$$

where g_{m1}, g_{m6}, and g_{mf1} are the transconductances of transistors M_1, M_6, and M_{f1}; and g_{ds1}, g_{ds3}, g_{dsf1}, g_{ds6}, and g_{ds7} are the small signal channel conductances of M_1, M_3, M_{f1}, M_6, and M_7 from Fig. 1(b), respectively.

If the feed-forward and second stages are designed to have

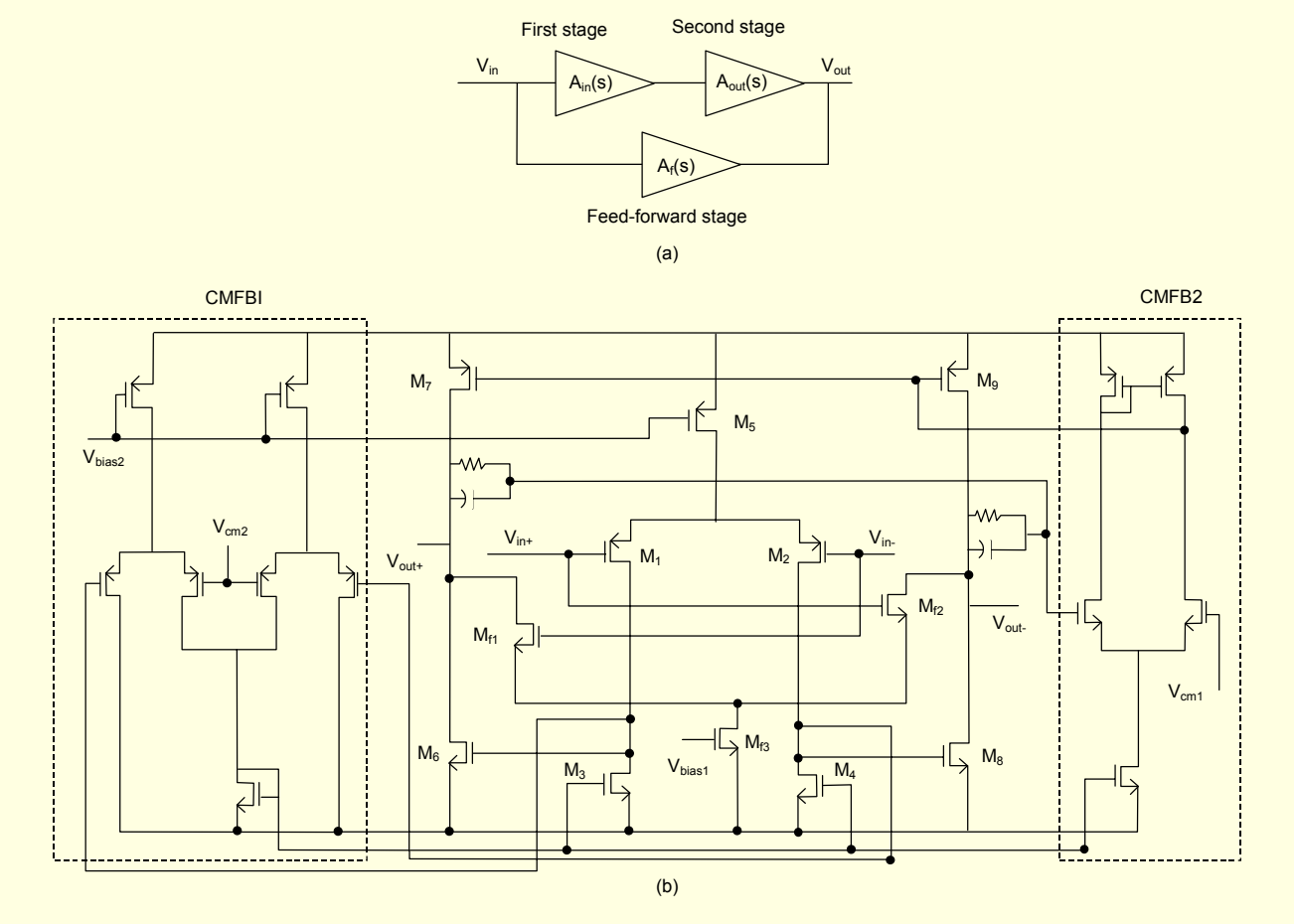

Fig. 1. The proposed DMB transmission system.

the same transconductance value, the open loop gain now becomes

$$\text{open loop gain} = \frac{g_{m6}}{(g_{dsf1}+g_{ds6}+g_{ds7})}\left(1+\frac{g_{m1}}{(g_{ds1}+g_{ds3})}\right). \quad (8)$$

The LHP zero is approximated as

$$\begin{aligned}\text{LHP zero} &\approx -\omega_{p1}\left(1+\frac{g_{m1}g_{m2}(g_{dsf1}+g_{ds6}+g_{ds7})}{g_{mf1}(g_{ds1}+g_{ds3})(g_{dsf1}+g_{ds6}+g_{ds7})}\right)\\ &= -\frac{g_{ds1}+g_{ds3}}{C_{gs6}}\left(1+\frac{g_{m1}g_{m2}}{g_{mf1}(g_{ds1}+g_{ds3})}\right)\\ &= -\frac{g_{ds1}+g_{ds3}+g_{m1}}{C_{gs6}},\end{aligned} \quad (9)$$

where C_{gs6} is the gate source capacitance of transistor M_6 in Fig. 1(b).

The major noise contributors of the OTA in Fig. 1(b) are the PMOS input differential pair, M_1 and M_2, and the NMOS current sink pair, M_3 and M_4. PMOS devices are selected for the input at the differential stage because of their lower 1/f noise. To evaluate the noise contribution of the feed-forward stage, we can compare the input referred noise of the OTA in Fig. 1(b) with the OTA without the feed-forward stage. Excluding the 1/f noise, the input referred thermal noise of the OTA in Fig. 1(b) is calculated as

$$\overline{V_{n,in}^2} = \frac{16kT}{3}\left(\frac{g_{m7}(g_{ds1}+g_{ds3})^2}{g_{m6}^2(g_{ds1}+g_{ds3}+g_{m1})^2}+\frac{2(g_{ds1}+g_{ds3})^2}{g_{m6}(g_{ds1}+g_{ds3}+g_{m1})^2}+\frac{(g_{m1}+g_{m3})}{g_{m6}(g_{ds1}+g_{ds3}+g_{m1})^2}\right). \quad (10)$$

In the above equation, the transconductances of the feed-forward and the second stages were assumed to have the same value.

Equation (11) shows the calculation of the input-referred noise of the OTA without the feed-forward stage:

$$\overline{V_{n,in}^2} = \frac{16kT}{3}\left(\frac{g_{m7}(g_{ds1}+g_{ds3})^2}{g_{m6}^2 g_{m1}^2}+\frac{(g_{ds1}+g_{ds3})^2}{g_{m6}g_{m1}^2}+\frac{(g_{m1}+g_{m3})}{g_{m6}g_{m1}^2}\right). \quad (11)$$

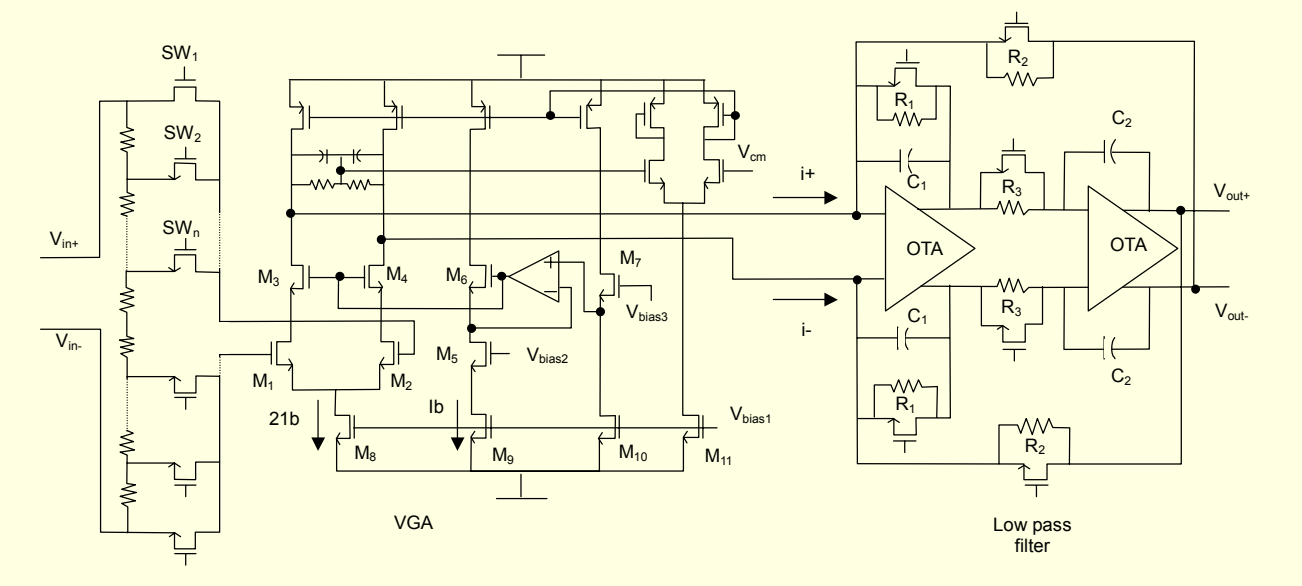

Fig. 2. The schematic realization of a VGA and Tow-Thomas low pass filter.

Comparing (10) to (11), the feed-forward stage does not increase the input-referred noise much if the second stage has a high transconductance value, which is required for the design of the second stage to obtain a high frequency bandwidth.

III. Design of Tow-Thomas Filter and VGA

Figure 2 shows the schematic of a low pass filter and VGA, while Fig. 3 shows the schematic of a high pass filter. The VGA is digitally programmable in steps of 3 dB and is realized using a switched resistor chain. The low pass filter is a Tow-Thomas biquad and allows for an independent tuning of the cut-off frequency and Q factor [6]. The active element is implemented using the OTA presented in the previous section.

In Fig. 2, transistors M_1 – M_4 constitute a transconductance stage that converts the input voltage signal into a current input to the filter. In order to enhance the linearity of this circuit, transistors M_1 and M_2 are operated in the triode region. Source degeneration techniques could be employed instead; however, the use of degeneration resistors leads to a loss of dynamic range [7]. Transistors M_3 and M_4 operate in the saturation region. To maintain the drain and source voltages of input differential pair M_1 and M_2 at a constant value, a bias tuning circuit is implemented [8].

Transistors M_1, M_2, M_5, and M_7 are all identical. Also M_3, M_4, and M_6 are identical transistors. Vbias3 is the same voltage as the input common mode voltage of input differential pair M_1 and M_2. Since the drain voltage of M_5 is designed to be equal to the drain voltages of M_1 and M_2, the gate voltage of M_3 and M_4 is adjusted to force the drain voltages of M_1 and M_2 to equal the source voltage of M_7, which results in the constant drain and source voltage of M_1 and M_2 [8]. The transconductance stage also includes a common mode feedback circuit to set the output common mode voltage to the desired value.

The filter tuning is achieved by using triode region transistors in parallel to resistors such as R_1, R_2 and R_3. The cutoff frequency and Q factor are given by the following expressions [6]:

$$\omega_0 = \sqrt{\frac{1}{R_2 R_3 C_1 C_2}},\ Q = \frac{R_1}{\sqrt{R_2 R_3}}\sqrt{\frac{C_1}{C_2}}. \qquad (12)$$

In direct conversion wireless receiver architectures, the DC offsets resulting from the self-mixing of the local oscillator must be removed to avoid saturating the baseband amplifiers [9]. In wideband systems, it is possible to use a high pass filter with a low corner frequency to filter out the DC offsets [10]. Figure 3 shows a circuit realization of a first order high pass filter. In Fig. 3,

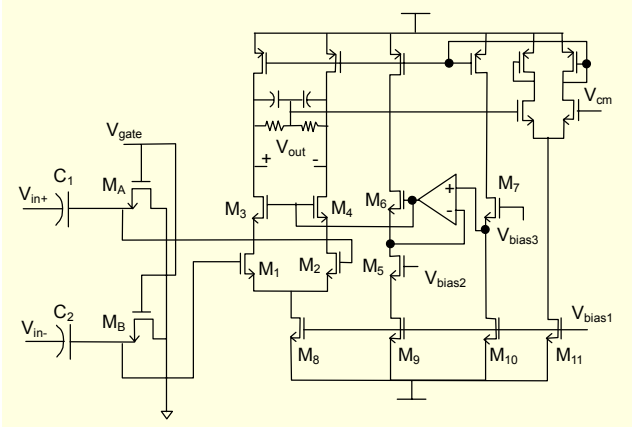

Fig. 3. A schematic realization of the high pass filter.

MOS transistors M_A and M_B operating in a deep triode region are used as resistive elements to save area and minimize parasitic capacitance. The active element is realized using an identical transconductance stage as that used in the VGA.

IV. Experimental Results

In order to realize a baseband chain for WLAN applications, a fourth order filter is used. Figure 4 shows the schematic of the proposed baseband chain.

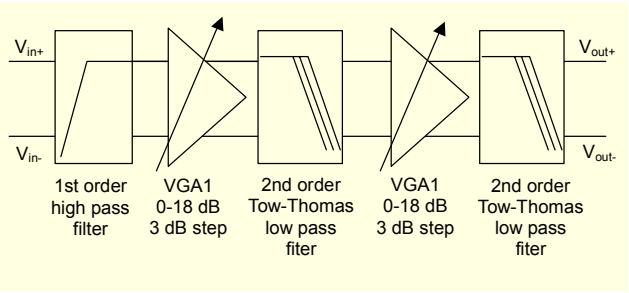

Fig. 4. A block diagram of the proposed baseband chain.

We fabricated a prototype in a 0.5 μm, double-poly, three-metal CMOS process. A microphotograph of the prototype is shown in Fig. 5. The chip size is 1.3 mm × 1.3 mm. The circuit operates at a supply voltage of 3 V, and the total power dissipation of the baseband chain is 20 mW.

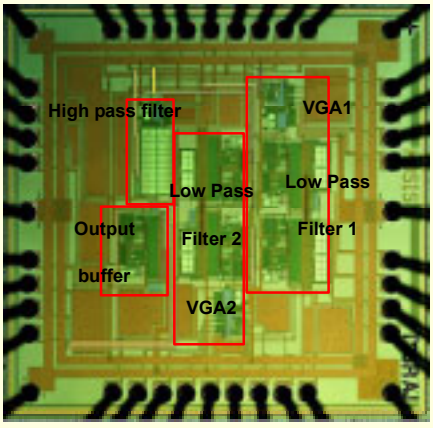

Fig. 5. The chip microphotograph (0.5 μm CMOS).

The overall frequency response of the baseband chain is shown in Fig. 6. The passband cut-off frequencies of the low pass and high pass filters are 10.1 MHz and 36 kHz, respectively. Stop band attenuation is larger than 45 dB. Table 1 shows the passive component values used in the design of low pass and high pass filters.

In order to evaluate the frequency and Q factor tuning capability of the filter, external tuning voltages were applied to the gates of the triode region transistors in parallel to R_1 and R_2, respectively, which are shown in Fig. 2. Figures 6(a) and 6(b) show the frequency and Q factor tuning capability of the prototype baseband chain.

Table 1. The passive component values.

Low pass filter	C_1 = 3 pF C_2 = 3 pF	R_1 = 4.2 kΩ, R_2 = 3.8 kΩ R_3 = 6.1 kΩ
High pass filter	C_1, C_2 = 11 pF	

Figure 7 shows the measured frequency response of the baseband chain for different gain settings. The measured VGA gain range is 33 dB tuned in steps of 3 dB.

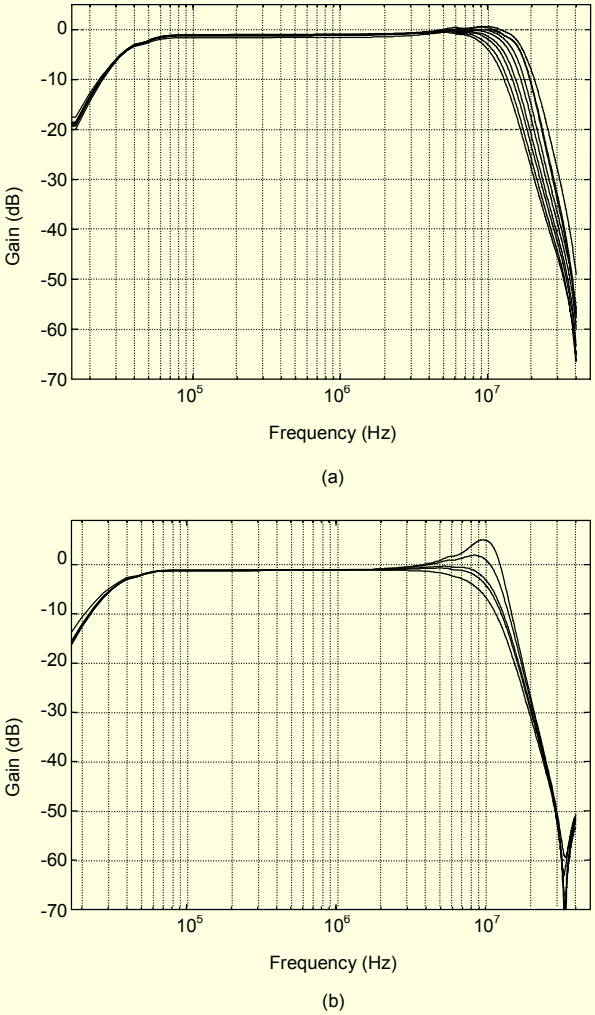

Fig. 6. (a) Measured frequency tuning (10 to 18.5 MHz) and (b) measured Q factor tuning of the baseband chain.

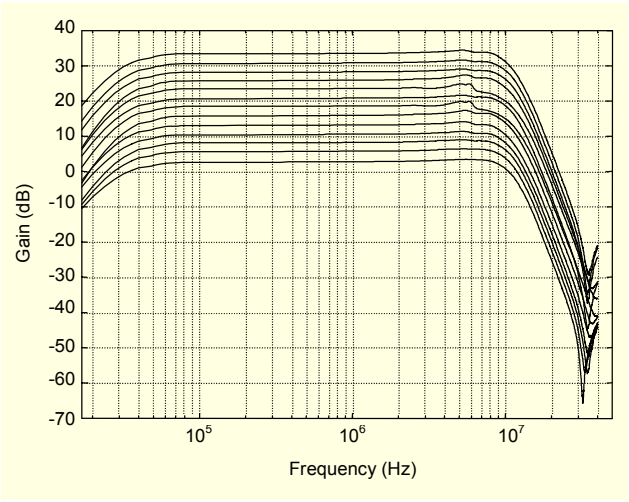

Fig. 7. Measured gain tuning range (33 dB in steps of 3 dB).

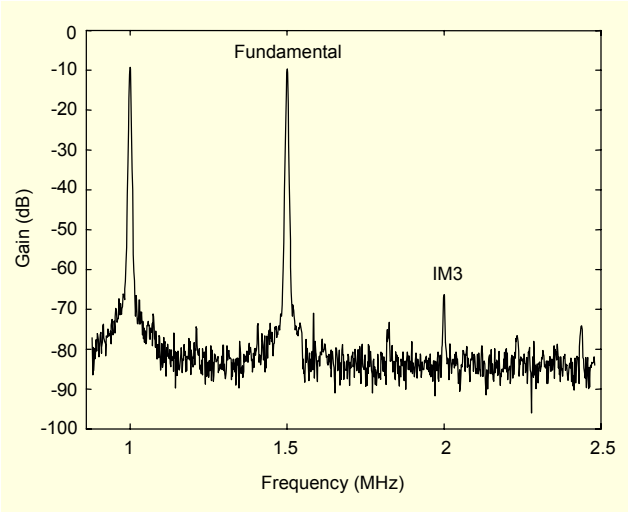

Fig. 8. Measured result of the two tone test of the baseband chain.

In order to evaluate the linearity of the baseband chain, a two-tone input at 1 MHz and 1.5 MHz is applied so that the resulting intermodulation products fall within the passband. When an input signal of 178 mV is applied, the third order intermodulation component at 2 MHz is found to be 55 dB below the fundamental signal. Figure 8 shows the measured result of the two-tone test.

Table 2 summarizes the measured performance of the proposed baseband chain.

V. Conclusion

The presented work shows the utility of feed-forward amplifiers in the realization of wideband baseband chains.

Two stage feed-forward compensated amplifiers provide wide gain bandwidth with moderate power consumption. The measurement results show that the wideband baseband chain only dissipates 20 mW to achieve the in-band linearity of 13 dBV. Measurement results from a prototype implementation indicate a possible use of the proposed baseband chain in WLAN receivers.

Table 2. Performance summary.

Technology	AMI 0.5 μm CMOS
Chip area	1300 μm × 1300 μm
Supply voltage	3.0 V
Power consumption	20 mW
Cut-off frequency	10 MHz
Signal amplitude (filter input)	1.6 Vpp differential
Input referred noise	114 μVrms
IIP 3 (in-band)	13 dBV
Stop band rejection	45 dB
DC component rejection	16 dB
Gain step	3 dB

References

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, New York, 2001.

[2] S.B. Hyun, G.Y. Tak, S.H. Kim, B.J. Kim, J. Ko, and S.S. Park, "A Dual-Mode 2.4-GHz CMOS Transceiver for High-Rate Bluetooth Systems," *ETRI J.*, vol. 26, no. 3, June 2004, pp. 229-240.

[3] D.A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New York, 1997.

[4] B.K. Thandri and J. Silva-Martinez, and F. Maloberti, "A Feedforward Compensation Scheme for High Gain Wideband Amplifiers," *Proc. IEEE Int'l Conf. on Electronics, Circuits and Systems*, Malta, Feb. 2001, pp. 1115-1118.

[5] B.K. Thandri and J. Silva-Martinez, "A Robust Feedforward Compensation Scheme for Multistage Operational Transconductance Amplifiers with No Miller Capacitors," *IEEE J. of Solid-State Circuits*, vol. 38, no. 2, Feb. 2003, pp. 237-243.

[6] R. Schaumann, M.S. Ghausi, and K.R. Laker, *Design of Analog Filters*, Prentice-Hall, Englewood Cliffs, NJ, 1990.

[7] K. Kolo and K. Halonen, *CMOS Current Amplifiers*, Kluwer Academic Publishers, Boston, 2002.

[8] B. Stefanelli and A. Kaiser, "CMOS Triode Transconductor with High Dynamic Range," *Electronics Lett.*, vol. 26, no. 13, June 1990, pp. 880-881.

[9] J. Jussila, J. Ryynanen, K. Kivekas, L. Sumanen, A. Parssinen, and K. Halonen, "A 22 mA 3.7 dB NF Direct Conversion

Receiver for 3 G WCDMA," *Proc. IEEE Int'l Solid-State Circuits Conf. Digest of Technical Papers*, Feb. 2001, pp. 264-285.

[10] B. Razavi, "A 2.4-GHz CMOS Receiver for IEEE 802.11 Wireless LAN's," *IEEE J. of Solid State Circuits*, vol. 34, no. 10, Oct. 1999, pp. 1382-1385.

Seoung-Jae Yoo received the BS, MS, and PhD degrees in electrical engineering from Ohio State University, Columbus, USA, in 1998, 2000, and 2004. His research interests are in low voltage, high speed CMOS analog circuit design.

Mohammed Ismail received the BS and MS degrees in electronics and telecommunications engineering from Cairo University in 1974 and 1978, and the PhD in electrical engineering from the University of Manitoba in 1983. He is a Professor with the Department of Electrical Engineering, Ohio State University and is Founder and Director of the Analog VLSI Lab. He has held several positions previously in both industry and academia and has served as a Corporate Consultant to nearly 30 companies in the United States and abroad. His current interests include low-voltage/low-power VLSI circuits, RF and mixed signal VLSI circuits for wireless communications, statistical computer-aided design and optimization, integrated circuits for image, video and multimedia applications and VLSI information processing systems. Dr. Ismail has been the recipient of several awards including the IEEE 1984 Outstanding Teacher Award, the NSF Presidential Young Investigator Award in 1985, the OSU Lumley Research Award in 1993, 1997, and 2002, the SRC Inventor Recognition Awards in 1992 and 1993, and a Fulbright/Nokia Fellowship Award in 1995. Dr. Ismail is a Fellow of IEEE.