A Numerically Controlled Oscillator with a Fine Phase Tuner and a Rounding Processor

In-Gi Lim and Whan-Woo Kim

ABSTRACT—We propose a fine phase tuner and a rounding processor for a numerically controlled oscillator (NCO), yielding a reduced phase error in generating a digital sine waveform. By using the fine phase tuner presented in this paper, when the ratio of the desired sine wave frequency to the clock frequency is expressed as a fraction, an accurate adjustment in representing the fractional value can be achieved with simple hardware. In addition, the proposed rounding processor reduces the effects of phase truncation on the output spectrum. Logic simulation results of the NCO using these techniques show that the noise spectrum and mean square error (MSE) for eight output bits of a 3.125 MHz sine waveform are reduced by 8.68 dB and 5.5 dB, respectively, compared to those of the truncation method, and 2.38 dB and 0.83 dB, respectively, compared to those of Paul's scheme.

Keywords—Numerically controlled oscillator (NCO), sine wave generator, look-up table, fine phase tuner, rounding processor.

I. Introduction

Numerically controlled oscillators (NCOs) are used in many digital signal processing applications including most recent communication systems. The most common technique for implementing an NCO is based on the look-up table (LUT). The LUT is used to store the sample values of a sinusoid signal, which are read out at appropriate time intervals to produce the sinusoidal signal.

Figure 1 shows the basic structure of an NCO based on an LUT. For each system clock (F_{clk}) period, the phase increment (S) is added to the L-bit phase accumulator. Only the M most significant bits out of the L-bit accumulator output represent the phase and address of the LUT, which converts the phase into the corresponding sine amplitude. The phase truncation (the difference of L-M) for reducing the size of the LUT yields the phase error.

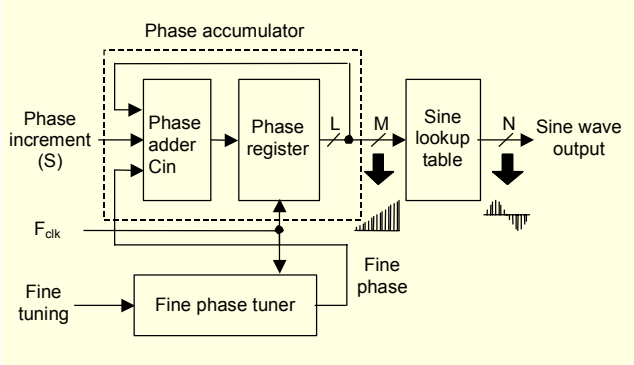

Fig. 1. The basic structure of an NCO based on LUT.

The phase increment (S) represents the amount of phase change in the output signal during each clock period. This value is related to the output frequency, which is given by

$$F_{out} = \frac{F_{clk}}{2^L} S \,, \qquad (1)$$

where F_{out} denotes the frequency of the output signal and S is a positive integer.

The LUT contains the sine amplitude values for only the phase range of 0 to $\pi/2$ but provides the sine wave values for the full range of 0 to 2π using symmetry. In this way, the required size of the sine LUT can be reduced to 1/4.

Various methods to reduce the LUT storage requirements for the first quadrant, $0 < \theta \leq \pi/2$, were introduced. One of the most effective methods is the Sunderland architecture that provides a

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way to reduce the LUT storage requirements by replacing one large LUT with two smaller LUTs [1]. Another approach is a sine-phase difference algorithm which provides a reduction in the LUT storage requirements by reducing the LUT output word-length [1].

As a conventional study related to the fine phase tuner in an NCO, R. Ertl [2] proposed a method of improving frequency resolution by cascading in K stages, in which the fine tuning circuits are made up of an adder and a D-flipflop. However, if the denominator in an arbitrary fraction B/A is not the power of two, accurate fine phase tuning is impossible and only an approximate solution is produced. Paul O'Leary proposed a modified direct-digital synthesizer which uses noise shaping to reduce the effects of phase accumulator truncation on the output spectrum [3].

II. Design of the Fine Phase Tuner

The output frequency of the NCO is equal to $S/2^L$ times the F_{clk} as provided in (1). However, in many practical situations, S should be expressed in terms of an integer plus a fraction. Then (1) is transformed as

$$F_{out} = \frac{F_{clk}}{2^L}\left(S' + \frac{B}{A}\right), \qquad (2)$$

where S', A, and B are positive integers, and B/A is an arbitrary fraction having a value smaller than unity. This fractional value requires the fine adjustment of phase, which is not provided by conventional NCOs. For this purpose, we propose a fine phase tuner.

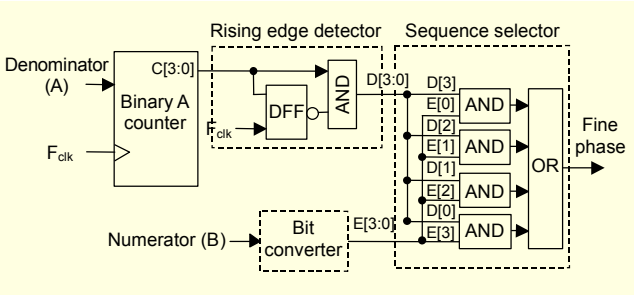

Fig. 2. The proposed fine phase tuner.

As an example of a detailed fine phase tuner proposed in this paper, Fig. 2 shows the case where denominator (A) and numerator (B) are expressed in 4-bit binary. Denominator A is inputted to binary-A counter and repeats the counting from 0 to A-1. The rising-edge detector generates each D of D[3:0] whose value is '1' during one clock period of F_{clk} at the rising edge of each C of C[3:0] from the counter. The bit-converter converts binary numerator B into the binary value E[3:0], which considers each bit's weight as the value of denominator A. The sequence selector output is given by D[3]•E[0] + D[2]•E[1] + D[1]•E[2] + D[0]•E[3], where • is logic *and* operation, and + is logic *or* operation. Hence, the proposed fine phase tuner generates the fine phase which has as much '1's as B during the A clock periods.

III. Design of the Rounding Processor

A new structure for a rounding processor is proposed to reduce both the effects of phase truncation on the spectrum of the output sine waveform and the MSE in the time domain. The proposed rounding processor has the same purpose as Paul's method. For noise shaping in Paul's scheme, the value of the L-bit phase accumulator is added to the value of L-M bits which is accumulated up to the previous clock time (i.e., $\sum_{k=0}^{n-1} x_{L-M}(k)$). However, the proposed rounding processor uses the value of L-M bits which is accumulated up to the present (i.e., $\sum_{k=0}^{n} x_{L-M}(k)$). According to the simulation results, the proposed method yields a better noise shaping than Paul's method.

Figure 3 shows the detailed block diagram of the rounding processor proposed in this paper. The output of the proposed rounding processor is given by

$$y_M(n) = trunc_{L-M}\left[x_L(n) + \sum_{k=0}^{n} x_{L-M}(k)\right], \qquad (3)$$

where $y_M(n)$ denotes the M-bit output of the rounding processor at time n, $x_L(n)$ denotes the L-bit output of the phase accumulator, $x_{L-M}(n)$ denotes the value of the L-M least significant bits of the phase accumulator, and $trunc_{L-M}(\bullet)$ denotes the truncation, which is accomplished by discarding the L-M least significant bits.

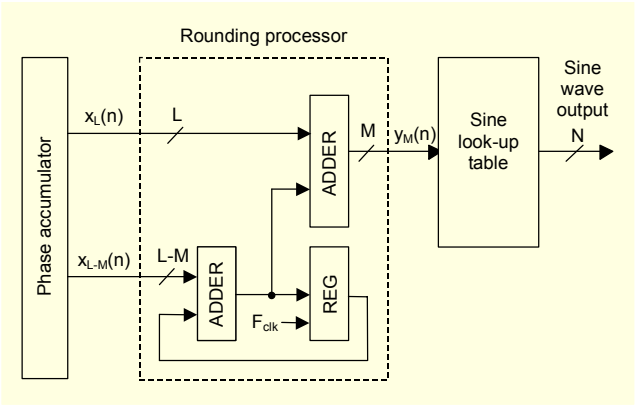

Fig. 3. The proposed rounding processor.

IV. Implementation of the NCO and Simulation Results

The fine phase tuner and the rounding processor proposed in

this paper are implemented in the NCO of the multi-carrier separation processor of the cdma2000 3X multi-carrier receiver system. The three digital sine waveforms that have to be generated in the NCO have a frequency of 0.625 MHz, 1.875 MHz, 3.125 MHz, and their relationship formulas to clock frequency 9.8304 MHz are shown below in (4), (5), and (6), respectively.

$$\frac{F_{out1}}{F_{clk}} = \frac{0.625\ \text{MHz}}{9.8304\ \text{MHz}} = \frac{520 + 5/6}{2^{13}} \tag{4}$$

$$\frac{F_{out2}}{F_{clk}} = \frac{1.875\ \text{MHz}}{9.8304\ \text{MHz}} = \frac{1562 + 3/6}{2^{13}} \tag{5}$$

$$\frac{F_{out3}}{F_{clk}} = \frac{3.125\ \text{MHz}}{9.8304\ \text{MHz}} = \frac{2604 + 1/6}{2^{13}} \tag{6}$$

According to the above formulas, the phase increment has three decimal values of "520", "1562" and "2604", and the phase adder and phase register have 13-bit resolution. Also, the fine phase tuner for adjusting the fine phase during the six clock periods has the binary-6 counter due to denominator 6 of the fractions, and the bit converter generates three binary values "111", "100" and "001" due to numerators 5, 3 and 1, respectively. Among the outputs of the 13-bit phase accumulator, only the eight most significant bits are used and the five least significant bits are discarded. The sine LUT makes use of 64 × 8 bits for the values of the first quadrant of the sine function.

Figure 4 shows the maximum noise spectrums as the number of sine LUT address bits varies. The proposed rounding processor yields a reduction of the noise spectrum by 8.68 dB compared to that of the truncation method and 2.38 dB compared to that of Paul's scheme for eight output bits of a 3.125 MHz sine waveform. Figure 5 shows the MSEs of the NCO outputs as the number of LUT's output bits changes. The MSE of the proposed NCO is improved by 5.5 dB compared to that of the truncation method and 0.83 dB compared to that of Paul's scheme with the same fine phase tuner and sine LUT.

V. Conclusions

A novel numerically controlled oscillator has been presented, which uses the fine phase tuner and the rounding processor to generate digital sine waveforms with a reduced phase error. By using the fine phase tuner presented in this paper, when the ratio of the desired sine wave output frequency to the clock frequency is expressed as a fraction, the fine adjustment value in B/A can be achieved using simple hardware. The proposed rounding processor reduces the effects of phase truncation on the output spectrum. The fine phase tuner and the rounding processor presented in this paper are implemented in the NCO of the multi-carrier separation processor of the cdma2000 3X multi-carrier receiver system. Simulation results of the NCO using these techniques show that the noise spectrum and the MSE of the NCO output are reduced compared to those using the existing methods.

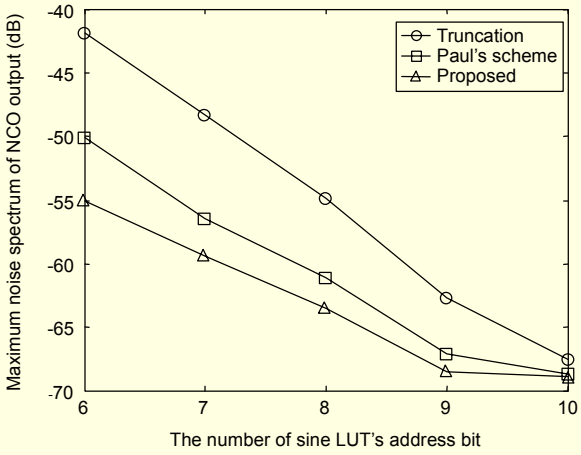

Fig. 4. Comparison of the maximum noise spectrums (F_{out} = 3.125 MHz, L = 13 bit, N = 8 bit).

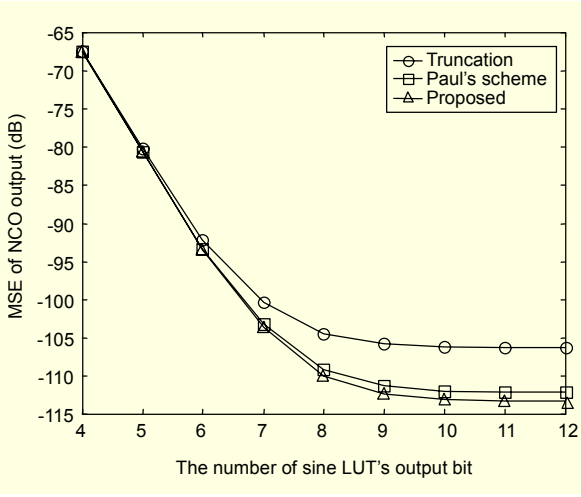

Fig. 5. Comparison of the mean square errors (F_{out} = 3.125 MHz, L = 13 bit, M = 8 bit).

References

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