A New SOI LDMOSFET Structure with a Trench in the Drift Region for a PDP Scan Driver IC

Won-So Son, Sang-Gi Kim, Young-Ho Sohn, and Sie-Young Choi

To improve the characteristics of breakdown voltage and specific on-resistance, we propose a new structure for a LDMOSFET for a PDP scan driver IC based on silicon-on-insulator with a trench under the gate in the drift region. The trench reduces the electric field at the silicon surface under the gate edge in the drift region when the concentration of the drift region is high, and thereby increases the breakdown voltage and reduces the specific on-resistance. The breakdown voltage and the specific on-resistance of the fabricated device is 352 V and 18.8 $m\Omega \cdot cm^2$ with a threshold voltage of 1.0 V. The breakdown voltage of the device in the on-state is over 200 V and the saturation current at V_{gs}=5 V and V_{ds}=20 V is 16 mA with a gate width of 150 μm.

Keywords: lateral double-diffused MOSFET (LDMOSFET), trench, silicon-on-insulator (SOI), power integrated circuit (PIC).

I. Introduction

Intelligent power integrated circuits have become increasingly popular for implementing system functions with improved performance, reduced size, low cost, and low power consumption. For example the flat panel display industry has made effective use of power integrated circuits (PICs) to offer improved features. In particular, a plasma display panel requires power devices with a breakdown voltage above 100 V in the data driver IC or 250 V in the scan driver IC [1]. Currently, a lateral double-diffused MOSFET (LDMOSFET) structure is commonly used in such circuits. Yet, in the case of LDMOSFET, the use of fine lithography cannot reduce the size imposed by the drift region, as the breakdown voltage of an LDMOSFET is a function of the doping and length of the drift region [2]. Many studies have reported on the specific on-resistance (R_{on}) and breakdown voltage improvement of LDMOSFET devices [3]-[7]. The silicon-on-insulator (SOI) has emerged as the technology of choice for fabricating PICs, because the buried oxide provides an effective way of isolating the low-power CMOS from the high-side and low-side power devices, thereby preventing such problems as induced over-voltages and latch-up, without having to resort to using expensive deep wells. This advantage has spawned a great interest in fabricating PICs with an SOI [8]-[10].

Accordingly, the current study proposes a new type of LDMOSFET, called a trench LDMOSFET, based on an SOI in which a trench is applied under the gate in the drift region, and the electric characteristics are investigated using a process simulation program, ATHENA, and a 2-D device simulation program, ATLAS. By including a trench in the device, the electric field under the gate edge is alleviated and the doping concentration of the n-drift region can be increased, thereby

Manuscript received Sept. 9, 2003; revised Nov. 7, 2003.

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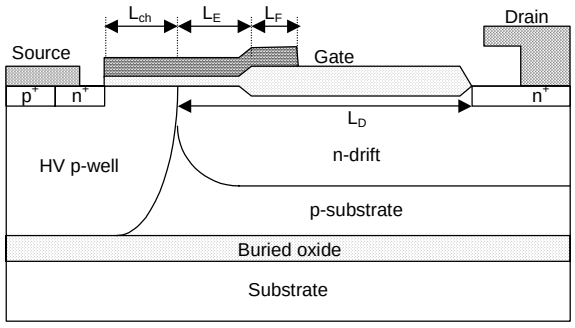
increasing the breakdown voltage and reducing the specific on-resistance. As a result, the trade-off between the breakdown voltage and the R_{on} is improved.

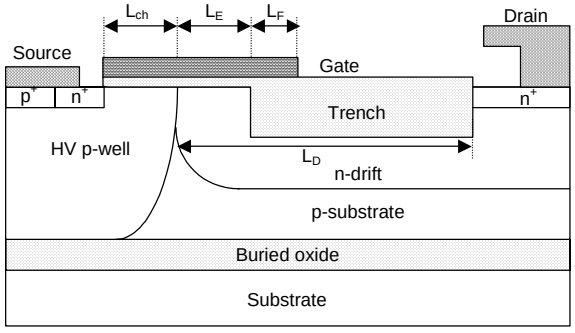
II. Device Structures and Simulation Results

Schematic cross sections of the conventional LOCOS LDMOSFET and the proposed trench LDMOSFET are shown in Fig. 1. Generally, the breakdown voltage of the conventional SOI LDMOSFET is limited by the buried oxide thickness, SOI thickness, the drift region length and the drift region concentration. To compare the characteristics of the proposed trench LDMOSFET with the conventional LOCOS LDMOSFET, the basic parameters of the structure, except the drift region dose and the trench depth, were fixed as follows.

We used an SOI silicon wafer with an 8 μm active layer on 3.0 μm buried oxide and a p-substrate with a concentration of 1×10^{15} cm^{-3}. Boron was doped with a dose of 5×10^{12} cm^{-2} for the high voltage (HV) p-well and the phosphorus was doped with the various doses for the n-drift region to achieve a maximum breakdown voltage. The channel length (L_{ch}) and gate extension (L_E) were 3 μm, the gate extension over the field (L_F) was 2 μm, the gate oxide thickness was 500 Å, and the drift region length (L_D) was 16 μm. The thickness of LOCOS

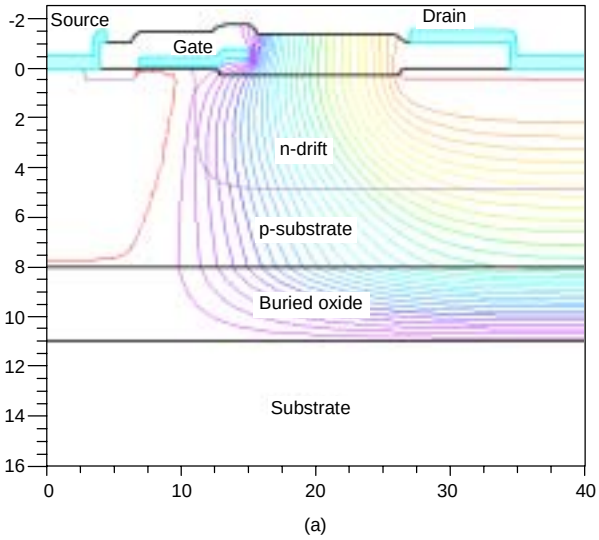


(a)

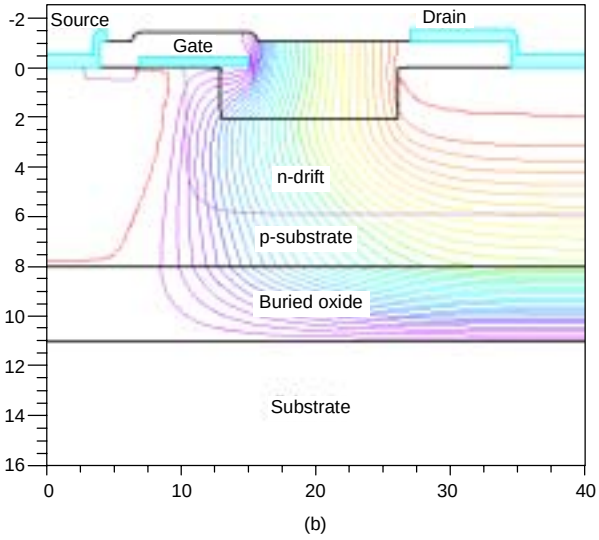


(b)

Fig. 1. The cross sections of (a) the conventional LOCOS LDMOSFET and (b) the proposed trench LDMOSFET.



(a)



(b)

Fig. 2. Potential distribution of (a) the conventional LOCOS LDMOSFET and (b) the proposed trench LDMOSFET at 305 V.

for the conventional LOCOS LDMOSFET was 6000 Å, while the trench depth was the key parameter for the proposed trench LDMOSFET when the trench width was fixed at 13 μm.

The main performance parameters for smart power devices are R_{on} and the breakdown voltage, which are inversely related to each other. As such, the optimum design between the breakdown voltage and the R_{on} is the main issue for high voltage LDMOSFET devices. A trench under the gate edge in the drift region can increase the breakdown voltage by reducing the electric field there, while slightly reducing the R_{on} by increasing the doping concentration of the drift region. Figure 2 shows the potential distribution of the conventional LOCOS LDMOSFET and the proposed trench LDMOSFET at 305 V, which is the breakdown voltage of the conventional LOCOS

LDMOSFET. In the conventional LOCOS LDMOSFET, the potential was crowded at the gate edge, resulting in a high electric field under the gate edge; however, the thickness of the LOCOS under the gate could not sufficiently reduce the electric field. Thus, to improve the breakdown voltage characteristics, the oxide thickness under the gate needed to be thicker than the LOCOS to reduce the electric field under the gate edge. One way to increase the oxide thickness would be to apply a trench. As in the conventional LOCOS LDMOSFET, the potential was crowded at the gate edge; however, the oxide thickness under the gate edge in the proposed trench LDMOSFET was thicker than that in the conventional LOCOS LDMOSFET so the potential crowding was reduced (Fig. 2 (b)) and the electric filed was reduced under the gate edge.

In the conventional LOCOS LDMOSFET, the breakdown voltage was 305 V with an optimized drift dose of 1.75×10^{12} cm^{-2} when the drift region length was 16 μm and the peak electric field was located at the edge of the drain. Yet, when the drift dose was increased to 2.0×10^{12} cm^{-2} to reduce the R_{on}, because the R_{on} for high voltage devices with a breakdown voltage over 100 V was mainly determined by the drift region resistance [11], the peak electric field position was changed to the gate edge and the breakdown voltage was drastically reduced to 258 V. Therefore, to increase the breakdown voltage with a higher dose than the optimal dose by alleviating the electric field at the gate edge, we created a trench under the gate in the drift region because oxide in a trench can withstand a higher voltage than silicon. In the proposed trench LDMOSFET, the optimized drift dose was 2.75×10^{12} cm^{-2} when the depth and the width of the trench were 1.25 and 13 μm, respectively, the total gate length was 8 μm, and the field plate on the trench was 2 μm. The peaks of the electric field within the trench

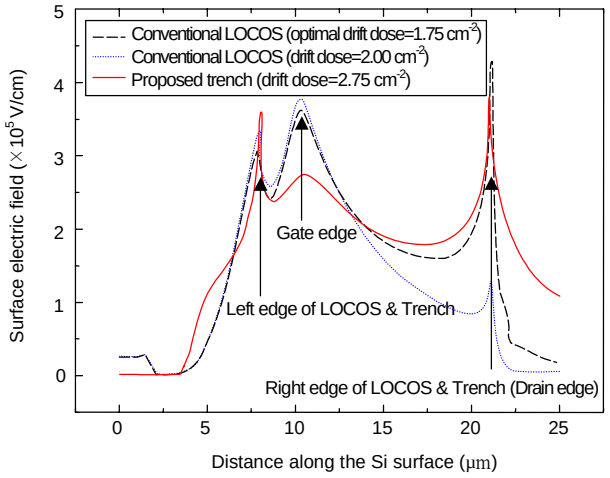


Fig. 3. Electric field distributions at the silicon surface of the conventional LOCOS LDMOSFET and the proposed trench LDMOSFET with trench depth of 1.25 μm.

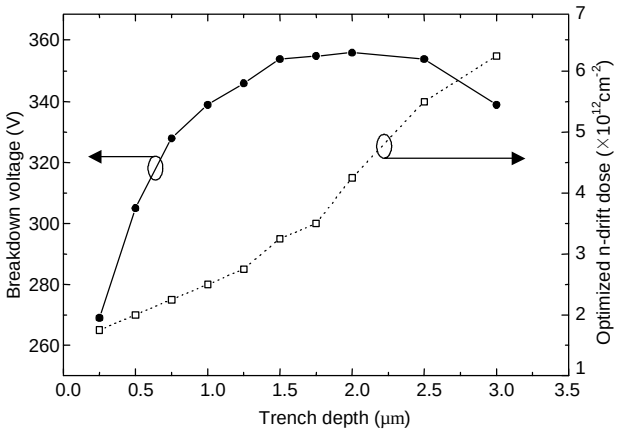


Fig. 4. Effects of the trench depth on the drift dose and the breakdown voltage.

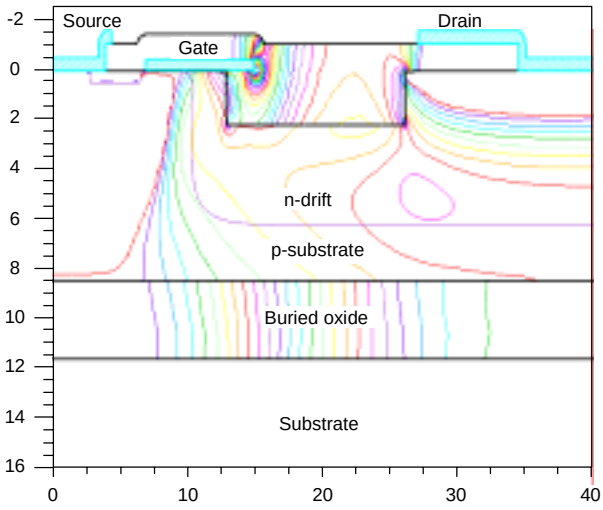


Fig. 5. Electric field distribution of the optimized trench LDMOSFET at breakdown.

LDMOSFET at breakdown were located at the right and left edges of the trench (Fig. 3). As a result, the breakdown voltage increased from 305 V for the conventional LOCOS device to 346 V for the trench device.

Figure 4 shows the effects of the trench depth and the drift dose on the breakdown voltage, both of which had a significant impact on the device characteristics. With the same doping concentration of the drift region, when the trench became deeper, the electric field at the right edge of the trench increased due to the potential crowding, and breakdown occurred. Therefore, to alleviate the electric field at the right edge of the trench, we needed to increase the drift doping concentration. With the same trench depth, when the drift dose was higher than the optimal dose, the breakdown occurred at the left edge of the trench, yet when the drift dose was lower than the optimal dose, breakdown occurred at the right edge of the

trench. The maximum breakdown voltage of 356 V was obtained when the trench depth was 2 μm and the drift dose was 4.25×10^{12} cm^{-2}, which was three times the drift dose of the optimized conventional LOCOS LDMOSFET. Under these conditions, the peak electric field moved to the bulk (Fig. 5). However, when the trench depth was over 2 μm, the breakdown voltage began to decrease; since the higher dose could not catch the trench depth, the electric field at the right edge increased due to the potential crowding.

The simulated breakdown voltages and the specific on-resistances of the LDMOSFET devices with the conventional LOCOS field oxide and the trench filled with oxide were 305 V, 356 V and 17.1 mΩ·cm^2, 16.6 mΩ·cm^2, respectively.

III. Device Fabrication and Results

We designed and implemented a new device for a 350 V SOI LDMOSFET for a PDP scan driver IC. We used a 2-D simulator ATHENA to design the various processing steps [12]. The starting SOI substrates had an 8 μm-thick silicon layer and 3 μm-thick buried oxide. The background doping concentration of the silicon layer was 1×10^{15} cm^{-3}. We used the standard CMOS process except for the trench formation process. The process began with ion implantation for the p-well and the n-drift region. The doses for the p-well and n-drift regions were 5×10^{12} cm^{-2} and 3.5×10^{12} cm^{-2}, respectively. The drive-in step was performed in an inert ambient at 1200 °C for a uniform drift region with a junction depth of 5.5 μm from the result of ATHENA. After that, we formed a trench by silicon etching using HBr/He-O_2/SiF_4 by MERIE (P-5000, AMK) [13]. To make the surface of the trench smooth, we performed wet oxidation for 10 min at 1000 °C. We used chemical mechanical polishing (CMP) for the planar process. The depth of the trench was 1.5 μm. We used silicon nitride of 4000 Å as the barrier during the CMP process. Figure 6 shows a cross section view of the trench after CMP.

The gate oxide of 500 Å was thermally grown and the poly-silicon of 5000 Å was deposited by LPCVD and doped with $POCl_3$. We then carried out a phosphorous implantation to dope the drain and the source regions with a dose of 3×10^{15} cm^{-2} and an energy of 80 keV. After this, we implanted boron to form the contact to the high voltage p-well next to the source with a dose of 5×10^{15} cm^{-2} and energy of 50 keV. Finally, metallization was followed by sputtering of Al to form metal electrodes. The wafer was then sintered for 30 min at 400 °C.

We used an HP4155A precision semiconductor parameter analyzer to measure the breakdown voltage, the threshold voltage, and the specific on-resistance, and a Tektronix programmable curve tracer 370A to evaluate the electrical characteristics.

Figure 7 shows the breakdown voltage characteristics according to the n-drift dose for the proposed trench LDMOSFET. The optimized dose was 3.25×10^{12} cm^{-2} with a breakdown voltage of 352 V.

Figure 8 shows the breakdown characteristics of the proposed trench LDMOSFET, and Fig. 9 shows the on-state characteristics. At V_{ds} = 0.1 V the threshold voltage was 1.0 V. At V_{gs} = 5 V, based on the current-voltage characteristics in Fig. 8, the calculated specific on-resistance for the device was 18.8 mΩ·cm^2 with the drain current of 168 μA at V_{ds} = 0.1 V when the area of the device was 3.15×10^{-5} cm^2.

$$R_{on} = 0.1\ V / 168\ \mu A \times 3.15\times10^{-5}\ cm^2 = 18.8\ m\Omega\cdot cm^2$$

The specific on-resistance of 18.8 mΩ·cm^2 was lower than any other published work for SOI LDMOSFET devices [14]-[15].

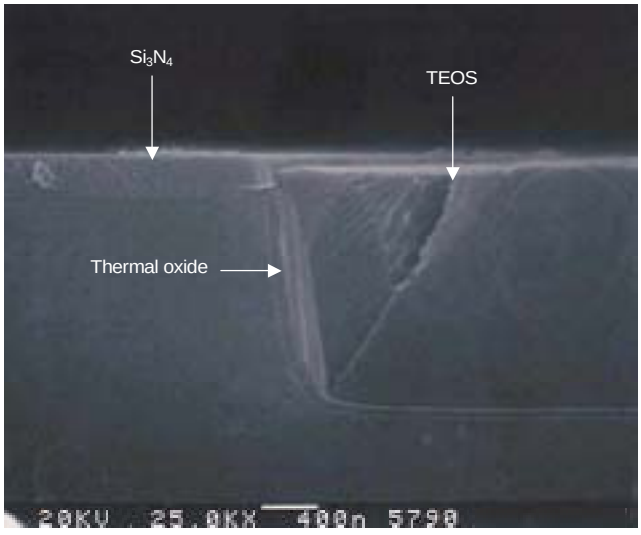


Fig. 6. Cross section of the trench after CMP process. The trench depth is 1.5 μm.

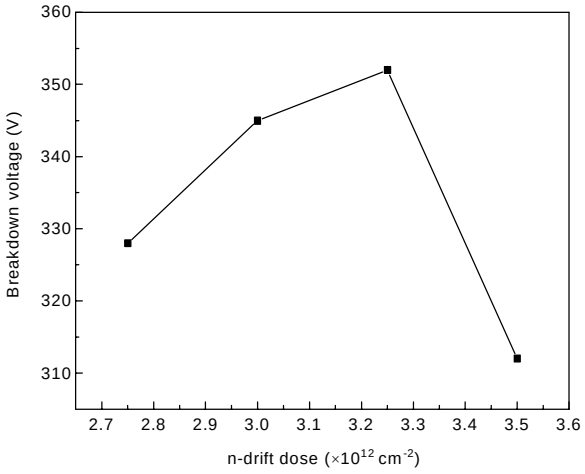


Fig. 7. Breakdown voltage characteristics of the proposed trench LDMOSFET based on the n-drift dose.

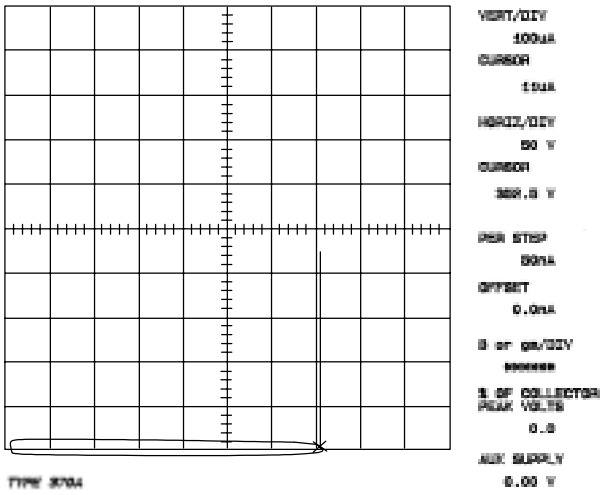


Fig. 8. Breakdown characteristics of the proposed trench LDMOSFET.

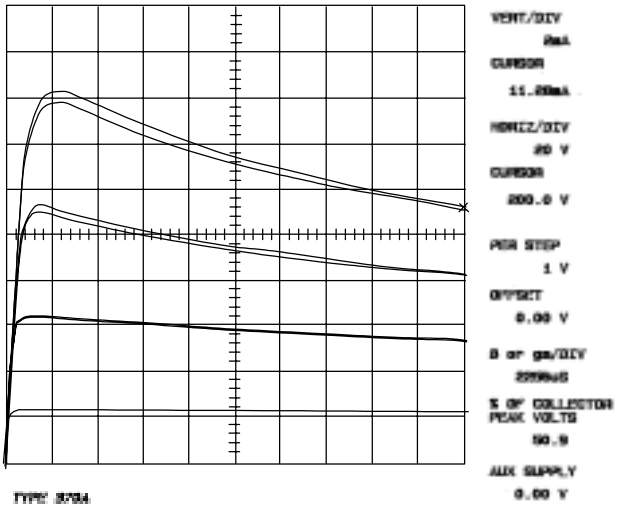


Fig. 10. Forward conduction characteristics of the proposed trench LDMOSFET.

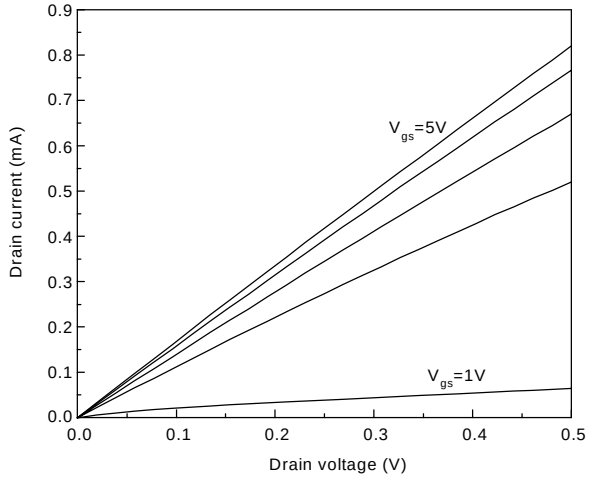


Fig. 9. Forward on-resistance characteristics of the proposed trench LDMOSFET.

Figure 10 shows the forward conduction characteristics of the proposed trench LDMOSFET. The saturation drain current at V_{gs}=5 V and V_{ds}=20 V was 16 mA with a gate width of 150 μm. The breakdown voltage of the proposed trench LDMOSFET in the on-state was over 200 V, which demonstrates that the device of the proposed trench LDMOSFET is good for a device in the output stage of a PDP scan driver IC.

IV. Conclusion

We proposed a new high voltage LDMOSFET structure for a PDP scan driver IC and developed it so as to increase the breakdown and on-resistance characteristics. The proposed structure has a trench under the gate in the drift region; with this structure the electric field at the silicon surface under the gate edge was reduced so the breakdown voltage could be increased, and drift dose could be increased so the specific on-resistance could be reduced. The breakdown voltage and the specific on-resistance of the fabricated device was 352 V and 18.8 mΩ·cm^2 with a threshold voltage of 1.0 V. The breakdown voltage of the device in the on-state was over 200 V and the saturation current at V_{gs}=5 V and V_{ds}=20 V was 16 mA with a gate width of 150 μm.

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