Fabrication and Characteristics of an InP Single HBT and Waveguide PD on Double Stacked Layers for an OEMMIC

Hong Seung Kim, Hye Jin Kim, Sun Eui Hong,
Dong Yun Jung, and Eunsoo Nam

ABSTRACT—We have explored the fabrication of an InP/InGaAs single heterojunction bipolar transistor (HBT) and a wave guide p-i-n photodiode (PD) on two kinds of double stacked layers for the implementation of an optoelectronic millimeter-wave monolithic integrated circuit (OEMMIC). We applied a photosensitive polyimide for passivation and integration to overcome the large difference between the HBT and PD layers of around 3 μm. Our experiment showed that the RF characteristics of the HBT were dependent on the location of the PD layer, while the dc performances of the HBTs and PDs were independent of the type of stacked layer used. The F_t and F_{max} of the HBTs on the HBT/PD stacked layer were 10% lower than those of the HBTs on the PD/HBT stacked layer.

Keywords—InP, heterojunction bipolar transistor (HBT), wave guide photodiode, optoelectronic millimeter-wave monolithic integrated circuit (OEMMIC).

I. Introduction

The optoelectronic millimeter-wave monolithic integrated circuit (OEMMIC) is quite attractive to users of microwave photonics systems and high speed optical communication systems [1]. Specifically, long wavelength photoreceivers and microwave/millimeter-wave photoreceivers, each incorporating photodetectors and preamplifier electronics on the same chip, have been focused on OEMMICs fabricated by InP based technology. Some previous works [2], [3] propose that, for the photoreceivers, the p^+ doped base, the n type collector, and the n^+ doped subcollector of heterojunction bipolar transistor (HBT) layers can also be used as p-i-n photodiode (PD) layers. However, such methods require selecting the base and collector thicknesses to compromise for the trade-off between the high frequency performance of the PD device and that of the HBT device.

For this work, we grew several different layers for both the PD and HBT devices to improve the performances of each. A wave guide PD was fabricated with an InP based HBT on the same InP substrate for the implementation of an OEMMIC, leading to a high external quantum efficiency. In Particular, using two different InP substrates we explored two kinds of stacked layers: one having HBT/PD layers (bottom PD structure, BPD) and the other PD/HBT sequential layers (top PD structure, TPD). Also, we investigated the dc and RF characteristics of both the HBT and PD devices. Finally, the effects of the stack sequence on the characteristics of the HBT is presented and discussed.

II. Experiment

The heterostructures were grown on 2 in-diameter Fe-doped semi-insulating (100) InP substrates by a molecular beam epitaxy. Table 1 shows the layer structure parameters of the HBT and PD stacked layers.

A 2.4 μm thick double core wave guide InGaAs/InP p-i-n PD layer, a SHBT layer composed of a 60 nm p^+ base doped with carbon at 4×10^{19} cm^{-3}, and a 500 nm n type collector doped at 1×10^{16} cm^{-3} were grown. Two different stacked

Manuscript received July 22, 2003; revised Nov. 27, 2003.

Hong Seung Kim (phone: +82 51 410 4387, email: hongseung@hhu.ac.kr) was with Basic Research Laboratory, ETRI, Daejeon, Korea and currently with Department of Semiconductor Physics, Korea Maritime University, Busan, Korea.

Hye Jin Kim (email: nolawara@etri.re.kr), Sun Eui Hong (email: sehong@etri.re.kr), Dong Yun Jung (email: dyjung@etri.re.kr), and Eunsoo Nam (email: esnam@etri.re.kr) are with Basic Research Laboratory, ETRI, Daejeon, Korea.

Table 1. Control messages employed for the ERS-based bottom-up configuration.

	Layers	Type	Thick. (nm)	Con. (cm^{-3})
HBT	Emitter contacts	$In_{0.53}Ga_{0.47}As$	100	N: 5×10^{19}
	Emitter grading	InP	50	N: 5×10^{18}
	Emitter	InP	150	N: 5×10^{17}
	Space	$In_{0.53}Ga_{0.47}As$	5	Undoped
	Base	$In_{0.53}Ga_{0.47}As$	60	P: 4×10^{19}
	Collector	$In_{0.53}Ga_{0.47}As$	500	N: 2×10^{16}
	Etch stop	InP	10	N: 2×10^{16}
	Sub Collector	$In_{0.53}Ga_{0.47}As$	500	N: 5×10^{19}
PD	P photo capping	$In_{0.72}Ga_{0.28}As_{0.61}P_{0.39}$	100	P: 5×10^{19}
	P photo clad	InP	500	P: 5×10^{18}
	P photo core	$In_{0.72}Ga_{0.28}As_{0.61}P_{0.39}$	600	P: 5×10^{18}
	i-InGaAs	$In_{0.53}Ga_{0.47}As$	600	Undoped
	N^+ photo core	$In_{0.72}Ga_{0.28}As_{0.61}P_{0.39}$	600	N: 5×10^{18}

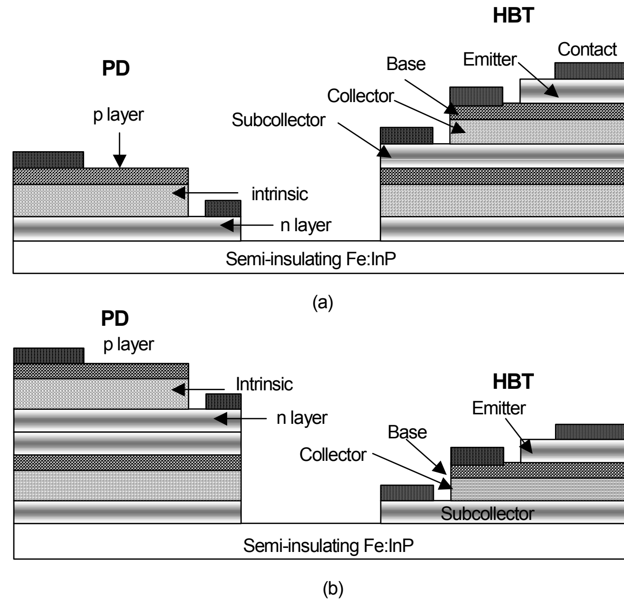


Fig. 1. Cross sectional schematic views of a HBT and wave guide PD: (a) HBT/PD stack structure (BPD) and (b) PD/HBT stack structure (TPD).

layers were grown for our experiments. Figures 1(a) and (b) show the cross-sectional schematic views of the HBT/PD (BPD) structure and the PD/HBT structure (TPD), respectively. The fabrication process for the InP HBT starts with the emitter contact (Ti (30 nm)/Pt (30 nm)/Au (100 nm)) which is formed using the lift-off technique, after which the selective wet etchings of an InGaAs cap layer and an InP emitter layer are carried out using H_3PO_4+H_2O_2+H_2O and H_3PO_4+HCl, respectively. To perform a 200 nm undercutting, we used twice the etching time required for the exact etching of a 200 nm thick InP emitter. After the emitter etching, base contact was formed and the base and collector layers were etched with H_3PO_4+H_2O_2+H_2O. A Ti (30 nm)/Pt (30 nm)/Au (100 nm) collector contact was formed on the n^+ InGaAs subcollector. In the case of the PD process, 6-µm-wide wave guides were formed by C_2H_6/O_2 reactive ion etching. For protection of the HBT or PD regions, while processing each device, we used nitride protection film. In addition, to reduce the process complexity, we made the emitter of the HBT while simultaneously making contact with both the p and n type doping areas of the PD. To overcome the difference between the p layer of the PD and the base of the HBT we applied a photosensitive polyimide for passivation and integration, instead of organic photoresists (together with either SiN or metal hard masks), all of which are typically used in microelectronic device applications as etch templates for patterning on polyimide [4]. For the experiment, we used polyimide, PI2723, from HD MicroSystems. We coated the polyimide and photo defined it with an exposure energy of 200

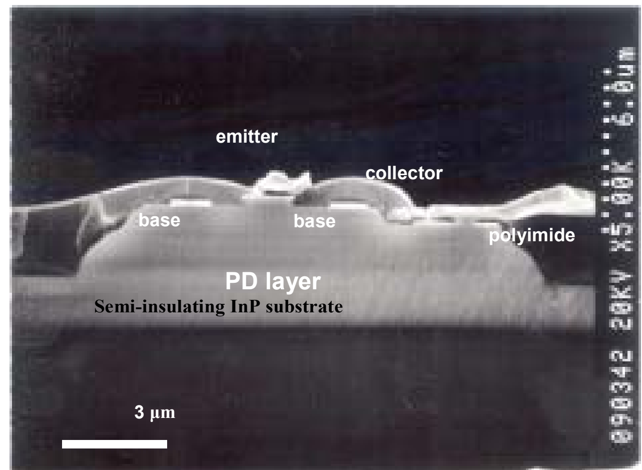
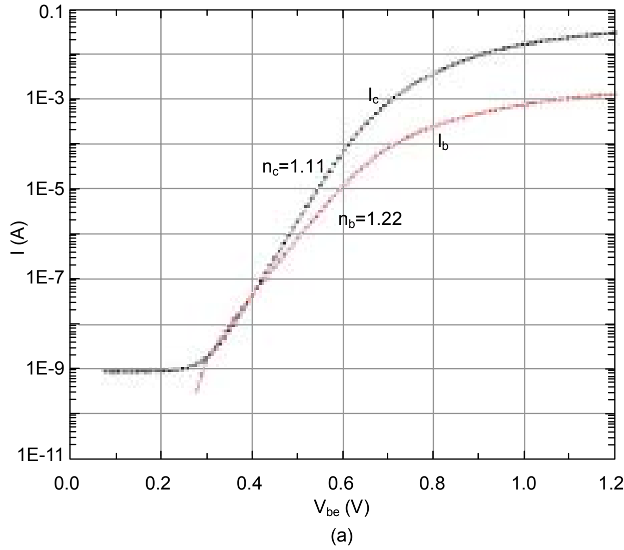


Fig. 2. A cross sectional SEM image of an InGaAs HBT formed on an HBT/PD stack structure.

mJ/cm^2 for the via hole, then cured the polyimide at 285 °C for 40 min. Figure 2 shows a cross-sectional SEM image of a single HBT formed on a BPD.

III. Results and Discussion

Figures 3(a) and (b) show a Gummel plot and an I-V characteristic of the HBT on a BPD with an emitter size of 2×10 μm^2. The collector and base currents have ideality factors of 1.11 and 1.22, respectively. The I_c-V_{ce} curve in Fig. 3(b) was obtained from high base currents between 0 and 500 µA. The dc current gain was around 25-30 with an offset voltage of less



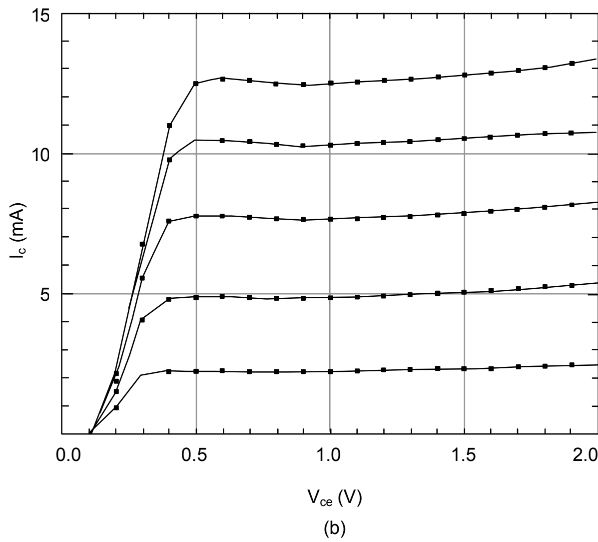


Fig. 3. (a) A Gummel plot and (b) an I-V curve obtained from I_b of 0 μA to 500 μA of an InP/InGaAs single HBT with 2×10 μm^2.

than 100 mV, and the BV_{ceo}, with a current density of 1μA/μm^2, was around 4.5 V. Also, we obtained similar dc values from the HBT. In Fig. 4, the leakage currents of the PDs of both the BPD and TPD were a few nA at –1 V and several tens nA at –5 V, even though the PD was formed on the HBT layer and met with a HBT process. Based on these results, the dc performance seems unaffected by the type of stacked layer used.

Figure 5 shows various frequency dependencies of current gain, $IH_{21}I^2$, and unilateral power gain, U, each obtained from a 2×10 μm^2 emitter geometry according to the type of stacked layer used. The HBT of the TPD structure has 107 GHz of current gain cutoff frequency F_t and 88 GHz of power gain cutoff frequency F_{max} at V_{ce} of 1 V and I_{ce} of 20 mA, while

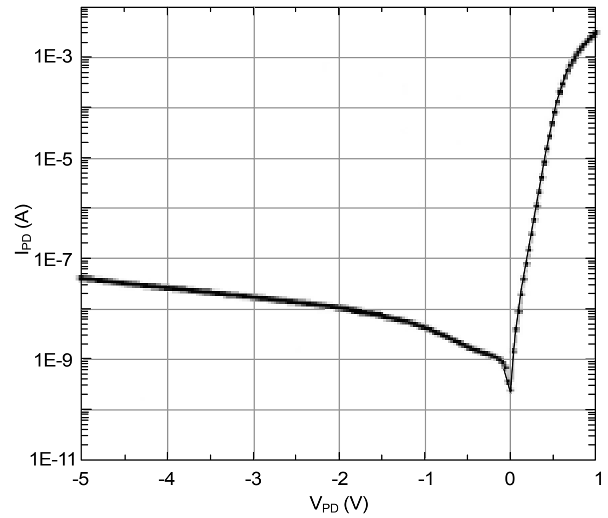


Fig. 4. The dark current of a waveguide PD of a TPD as a function of reverse bias.

the HBT of the BPD has 100 GHz of F_t and 75 GHz of F_{max} at Vc of 1 V and I_c of 20 mA. Compared with the TPD structure, F_t and F_{max} of the BPD structure were 6.5% and 15% lower, respectively. Moreover, the larger reductions of F_t and F_{max} into 82 GHz and 64 GHz, respectively, were made when the HBT of the BPD was isolated in the middle of the PD layer.

The additional capacitance of PD layer (C_{pd}) below the HBT seems to play a role in reducing F_t and F_{max}. Here, F_t is expressed by

$$\frac{1}{2\pi F_t} = \tau_b + \tau_c + \frac{kT}{qI_c}(C_{je} + C_{cb}) + (R_{ex} + R_c)C_{cb},$$

where τ_b and τ_c are the base transit time and collector charging time, R_{ex} and R_c are the parasitic emitter and collector resistance, and C_{cb} is the collector junction capacitance.

In addition, the F_{max} is defined by the following equation:

$$F_{\max} = \sqrt{\frac{F_t}{8\pi R_b C_{cb}}}.$$

As shown in the above equations, both F_t and F_{max} are dependent on the C_{cb}. Thus, it is conjectured that F_t and F_{max} of the HBT may be reduced by the addition of C_{pd} to C_{cb}. According to these equations, a 40% increase in C_{cb} would make a reduction of 15% of F_t and 20% of F_{max}. However, in our experiments, we obtained a C_{cb} value of 127 fF from the TPD, while the C_{cb} value of the BPD was 180 fF. That is, the F_t and F_{max} were reduced by 10%, even with a 40% increase in the value of C_{cb}.

In conclusion, based on the above results, we believe that

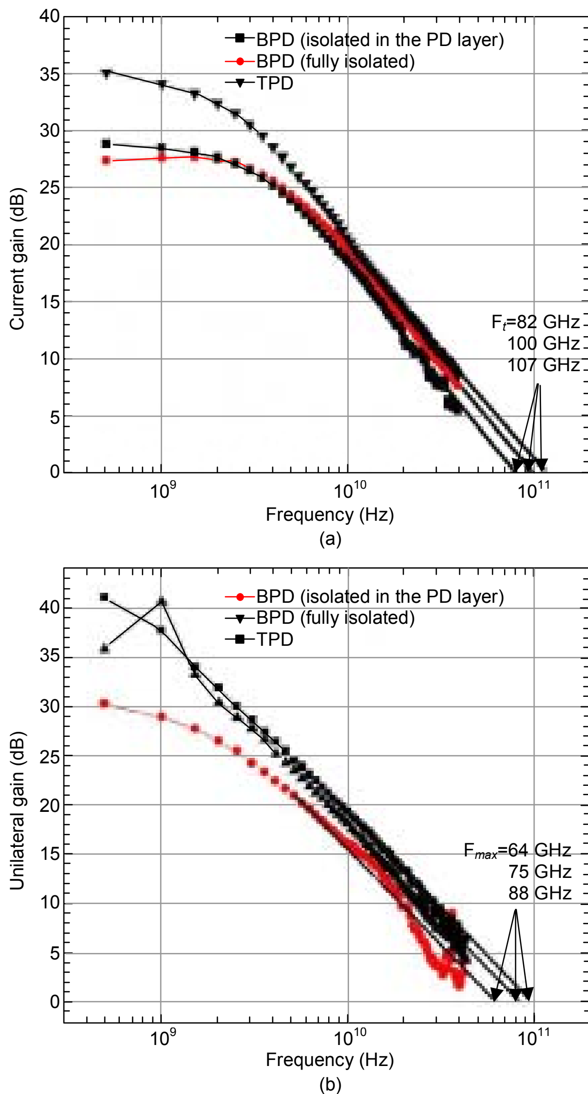


Fig. 5. (a) Current gain $|H_{21}|^2$ and (b) unilateral gain of an InP/InGaAs single HBT with a 2×10 μm^2 emitter geometry at V_{ce} of 1V and an I_c of 20 mA, according to the location of the isolation and the existence of a PD layer. Extrapolation is at –20 dB/dec.

both stack structures can be used for an OEMMIC employed in either a high speed optical communications system or microwave photonics system.

IV. Conclusion

We have explored the fabrication of an InP/InGaAs single heterojunction bipolar transistor and wave guide p-i-n photodiode on two kinds of double stack layers for the implementation of an OEMMIC. The HBTs had 25-30 of common emitter current gains and 4.5 V of breakdown voltage BV_{ceo}. Also, even though a PD was formed on the HBT layer, the dark currents were ten nA at –3 V. The HBTs on the PD/HBT stack layer had 107 GHz of current gain cutoff frequency F_t and 88 GHz of power gain cutoff frequency F_{max} at V_c of 1 V and I_c of 20 mA in a 2×10 μm^2 emitter size. The HBTs on the HBT/PD stacked layer had 100 GHz of F_t and 75 GHz of F_{max}.

References

[1] H. Kamitsuna, Y. Matsuoka, S. Yamahata, and N. Shigekawa, "Ultrahigh-Speed InP/InGaAs DHBTs for OEMMIC," *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 10, Oct. 2001, pp. 1921-1925.

[2] E. Sano, M. Yoneyama, H. Nakajima, and Y. Matsuoka, "A Monolithically Integrated Photoreceiver Compatible with InP/InGaAs HBT Fabrication Process," *IEEE J. Lightwave Technol.*, vol. 12, no. 4, Apr. 1994, pp. 638-643.

[3] S. Chandrasekhar, L.M. Lunardi, A.H. Gnauck, R.A. Hamm, and G.J. Qua, "High-Speed Monolithic p-I-n/HBT and HPT/HBT Photoreceivers Implemented with Simple Phototransistor Structure," *IEEE Photon. Technol. Lett.*, vol. 5, no. 11, Nov. 1993, pp. 1316-1318.

[4] S. Hall and C.C. Schuckert, "Single Mask Wafer Overcoat Process Using Photodefinable Polyimide," *Solid State Technology*, Oct. 1999.