# A 15 nm Ultra-thin Body SOI CMOS Device with Double Raised Source/Drain for 90 nm Analog Applications

Chang-Hyun Park, Myung-Hwan Oh, Hee-Sung Kang, and Ho-Kyu Kang

**Fully-depleted silicon-on-insulator (FD-SOI) devices with a 15 nm SOI layer thickness and 60 nm gate lengths for analog applications have been investigated. The Si selective epitaxial growth (SEG) process was well optimized. Both the single-raised (SR) and double-raised (DR) source/drain (S/D) processes have been studied to reduce parasitic series resistance and improve device performance. For the DR S/D process, the saturation currents of both NMOS and PMOS are improved by 8 and 18%, respectively, compared with the SR S/D process. The self-heating effect is evaluated for both body contact and body floating SOI devices. The body contact transistor shows a reduced self-heating ratio, compared with the body floating transistor. The static noise margin of an SOI device with a 1.1 μm² 6T-SRAM cell is 190 mV, and the ring oscillator speed is improved by 25 % compared with bulk devices. The DR S/D process shows a higher open loop voltage gain than the SR S/D process. A 15 nm ultra-thin body (UTB) SOI device with a DR S/D process shows the same level of noise characteristics at both the body contact and body floating transistors. Also, we observed that noise characteristics of a 15 nm UTB SOI device are comparable to those of bulk Si devices.**

**Keywords: Fully-depleted SOI, Si selective epitaxial growth, double raised, single raised, series resistance, self-heating, static noise margin.**

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## I. Introduction

Silicon-on-insulator (SOI) technology is penetrating the commercial market and has been included in the microelectronics roadmap as the most realistic solution for nano CMOS devices. Because the fully-depleted (FD) SOI device is fabricated on ultra-thin film SOI, it offers superior electrical characteristics over the bulk CMOS device [1] such as reduced junction capacitances, an increased channel mobility, a suppressed short-channel effect, and an excellent latchup immunity [2]. However, as dimensions of SOI CMOS devices are scaled down to the submicron regime, the source/drain (S/D) parasitic resistance becomes increasingly significant. Therefore, the raised S/D process with Si selective epitaxial growth (SEG) has been proposed to reduce the parasitic series resistance and improve the performance of FD-SOI CMOS devices [3]. However, as we scale down the SOI layer thickness to up to 15 nm, the conventional single raised (SR) source/drain process not only causes bad morphology of Si-SEG but is also not enough to reduce parasitic resistance. Therefore, the novel double-raised (DR) source/drain process is proposed and should be optimized to achieve a high performance of ultra-thin-film SOI CMOS devices.

SOI CMOS devices have many applications such as mixed-mode and high-speed circuits due to the isolation characteristics of the buried oxide layer. However, the buried oxide layer of SOI devices causes self-heating [4], which seriously degrades their performance due to the low thermal conductivity of the buried oxide. It is also reported that the body contact transistor shows better AC characteristics, such as

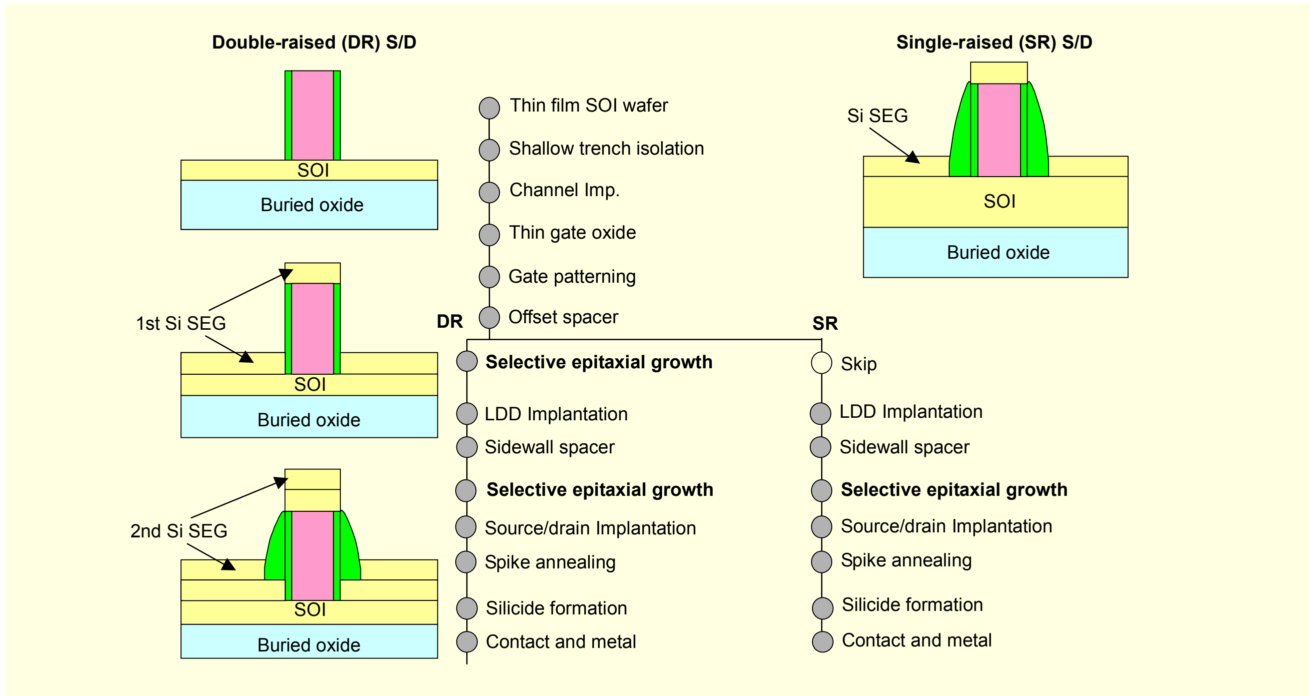


Fig. 1. Process sequence of double- and single-raised source/drain SOI transistors.

low frequency noise and AC kink [5], than the body floating transistor at a partially-depleted SOI [5]. It is necessary to analyze the characteristics of both the body contact and body floating FD-SOI devices for their analog applications.

In this paper, we propose the DR S/D process for a 90 nm technology node and investigate its operating characteristics for analog applications. The DR S/D process is compared with the conventional SR S/D process to optimize the raised source/drain process. The self-heating effect is analyzed and the static noise margin (SNM) of a 1.1 μm$^2$ SRAM cell is evaluated. Also, the speed gain of SOI inverter delay chains is analyzed. For analog application, open-loop voltage gain and low-frequency noise are investigated.

## II. Device Fabrication

The device fabrication sequence and transistor structure are summarized in Fig. 1. The shallow trench isolation process is applied to isolate the active area from the field area [6]. The channel ion implantation condition to control the threshold voltage is optimized for different SOI layer thicknesses. A thin gate dielectric film of 1.46 nm thickness is formed by the plasma nitrided oxidation. The gate polycrystalline silicon is formed by a normal hard-mask dry etch, and the offset spacer is formed by a high selectivity etch at the gate sidewall in order to suppress the short channel effect. For the DR S/D process, the first Si-SEG process is applied before the source/drain extension implantation in order to form a raised S/D. A heavily doped extension and halo region are formed under the gate in order to suppress the short channel effect and control the threshold voltage. The sidewall spacer is formed next to the offset spacer. The second Si-SEG process is employed before the deep S/D implantation and a 20 nm Si layer is grown at the source/drain. The cobalt self-aligned silicide (Salicide) is formed on the

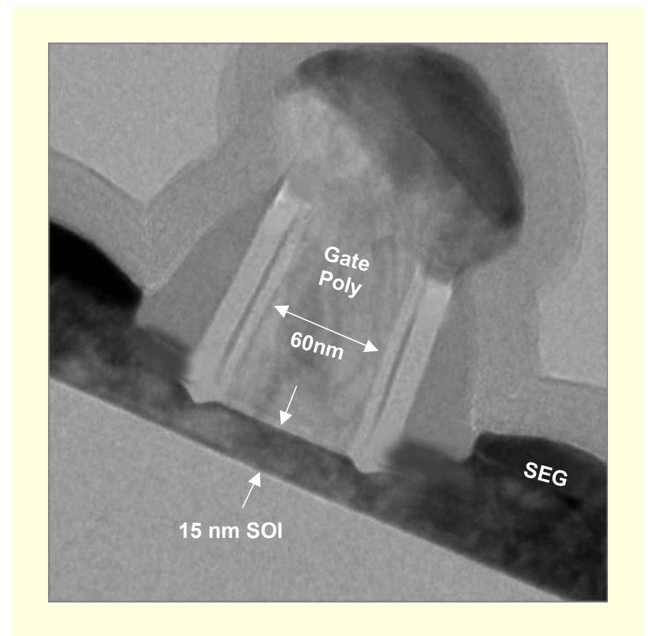


Fig. 2. A TEM photo of a double-raised source/drain SOI transistor ($T_{SOI}$ = 15 nm, $T_{GOX}$ = 1.4 nm).

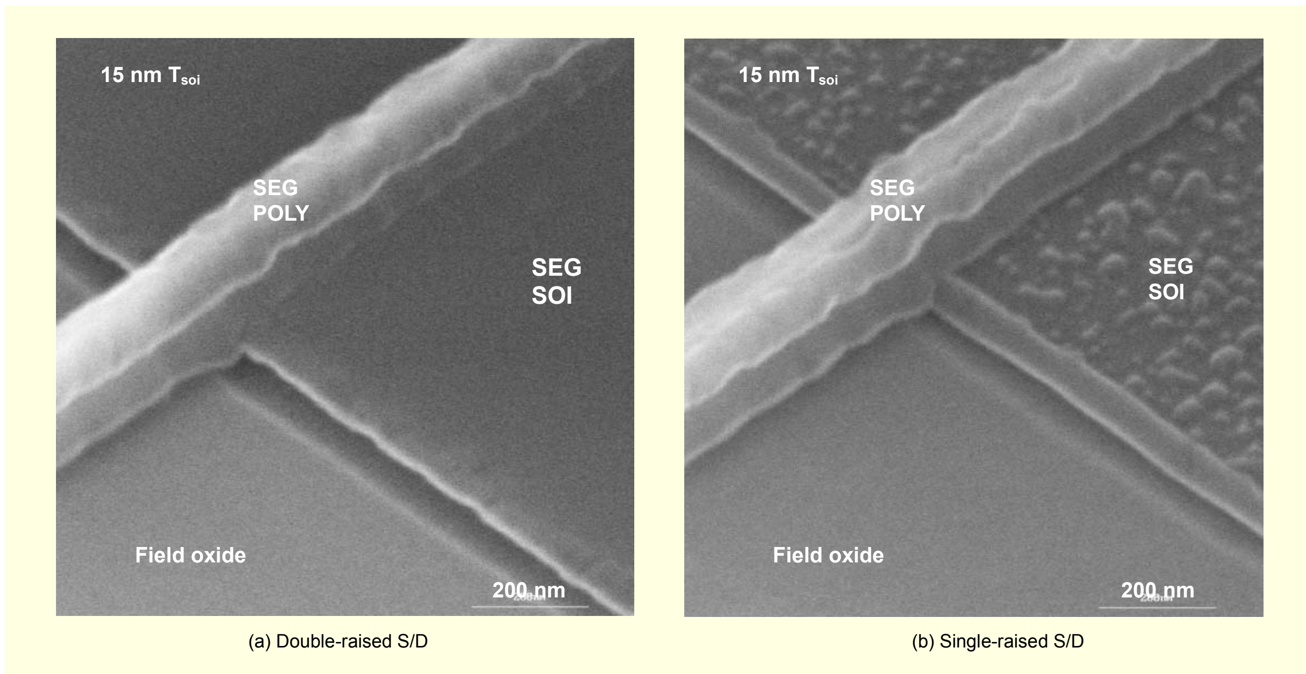


Fig. 3. SEG profiles in the active/poly region for double/single raised S/D processes.

gate and active region to reduce series resistance after deep S/D implantation. Cu interconnects with low-k dielectrics are applied for 1.1 $\mu m^2$ SRAM chips [7]. Figure 2 shows a transmission electron microscopy (TEM) cross section view of a 15 nm thick double-raised S/D FD-SOI transistor with a 60 nm gate length.

## III. Device Characteristics and Discussion

### 1. Double Raised Source/Drain FD-SOI Transistors

For the optimization of a raised S/D process, the Si-SEG process is applied for single and double raised S/D processes on a 15 nm SOI layer to investigate the effects of ion implantation and SOI thickness. Si-SEG profiles in the active and gate poly regions for DR and SR S/D processes on a 15 nm thick SOI layer are shown in Figs. 3(a) and 3(b), respectively. When the Si-SEG process is applied to a 15 nm SOI layer, the Si-SEG profile formed by the DR S/D process is better than that of the SR S/D process which has Si agglomeration [8] in the active region. For the SR S/D process, Si-SEG is not grown well due to the damage by the source/drain extension ion implantation at a thickness of 15 nm [9]. However, the DR S/D process shows a better profile because the first Si-SEG is applied before the source/drain extension ion implantation. Therefore, the DR S/D process should be used to grow the Si-SEG layer at a thickness of 15 nm.

The Si-SEG process consists of a hydrogen prebake and epitaxial growth [10]. The atmospheric pressure of the hydrogen prebake is lower than 10 Torr. As the hydrogen prebake temperature increases, shrinkage of the active region is observed for the SR S/D process, reaching 65 nm at 900°C, as shown in Fig. 4. In order to eliminate shrinkage, the total thermal budget of the Si-SEG process is reduced and no shrinkage is observed for the DR S/D process.

Figure 5 shows the threshold voltage characteristics for the single and double raised S/D processes. The DR S/D process shows better short-channel effect immunity, and a threshold

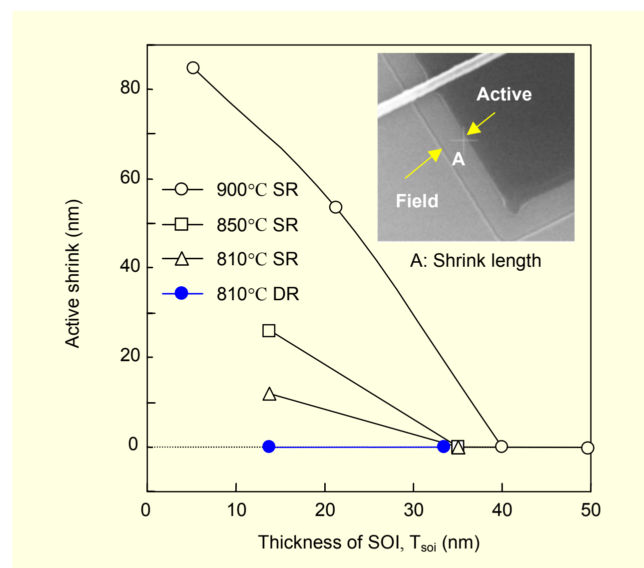


Fig. 4. Active shrink length vs. thickness of an SOI layer.

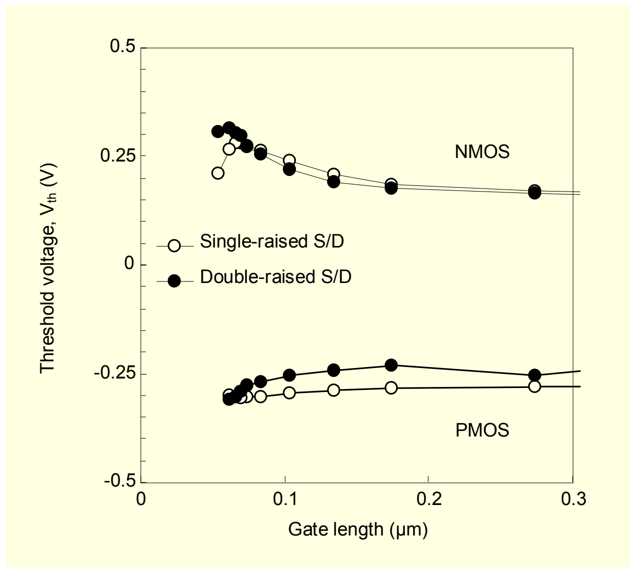


Fig. 5. Threshold voltage characteristics for single and double raised S/D processes.

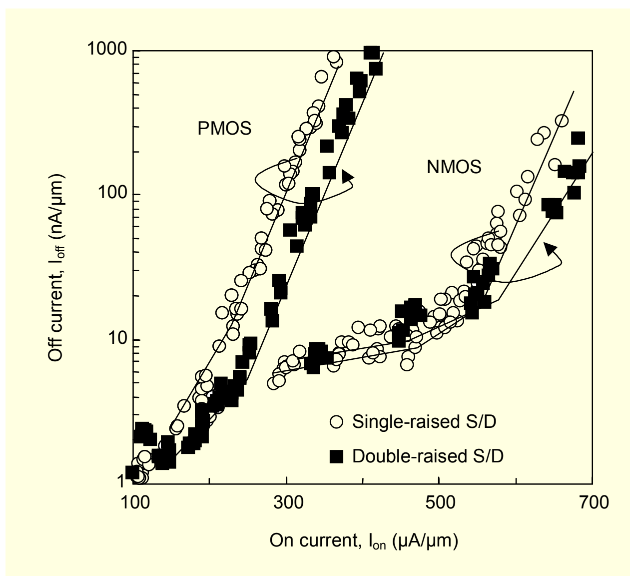


Fig. 6. On current vs. off current characteristics of NMOS and PMOS for single and double raised S/D processes.

voltage shift of 50 mV is observed for the DR S/D process in the PMOS due to the boron penetration. On current vs. off current ($I_{on}$-$I_{off}$) characteristics for NMOS and PMOS are shown in Fig. 6. The DR S/D process shows a better transistor performance than the SR S/D process for both NMOS and PMOS due to the lower series resistance as shown in Fig.7. For the DR S/D process, the saturation currents of both NMOS and PMOS are improved by 8 and 18 %, respectively, at a given off-current, relative to the SR S/D process. This indicates that the low sheet resistance of the source/drain extension of the DR

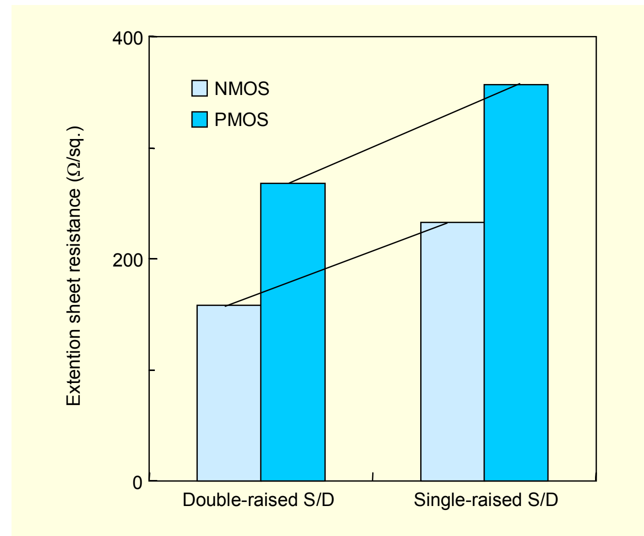


Fig. 7. Extension sheet resistance characteristics.

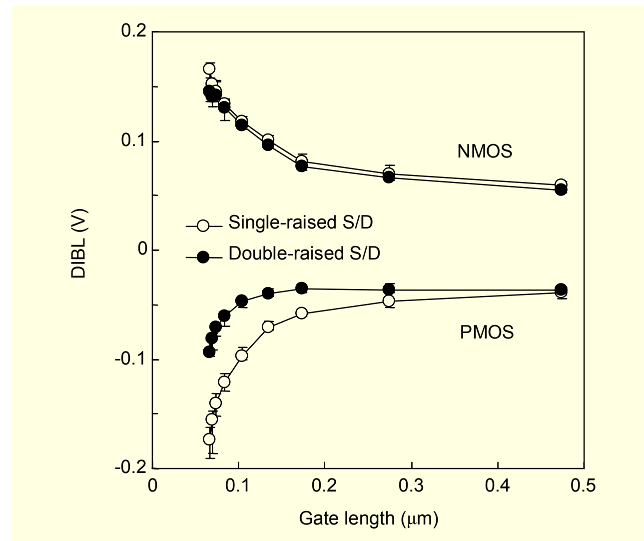


Fig. 8. DIBL with respect to gate length.

S/D process contributes to the higher performance than in the SR S/D process [11].

Figure 8 shows that the drain induced barrier lowering (DIBL) characteristics of a DR S/D device with a 70 nm gate length are dramatically improved by 3.8 and 52 % for NMOS and PMOS, respectively. For both DR and SR S/D devices, no kink effects are observed in the output conductance characteristics as shown in Fig. 9.

## 2. SRAM Cell, Self-Heating, Ring Oscillator, and Analog Characteristics

The area and stability of a cell are two important factors for SRAM cell design. Cell stability determines the soft-error rate

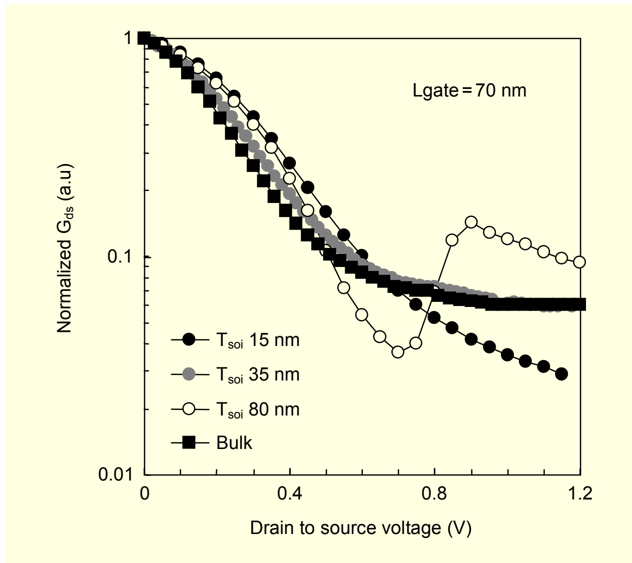


Fig. 9. Normalized conductance ($G_{ds}$) vs. drain to source voltage ($V_{ds}$).

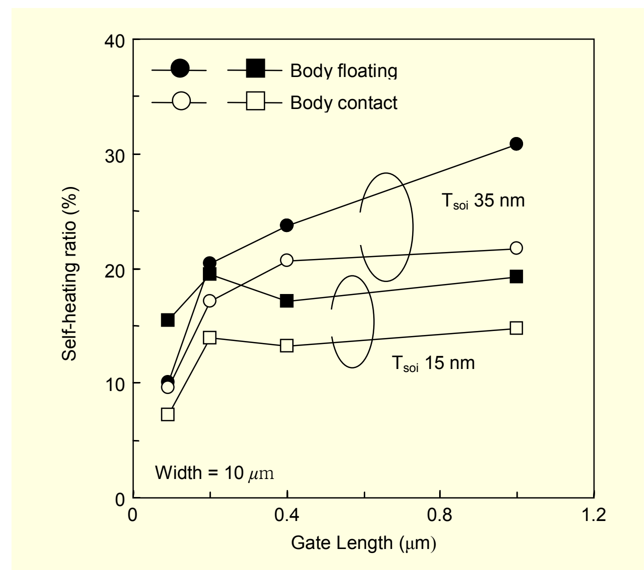


Fig. 11. Self-heating ratio vs. gate length.

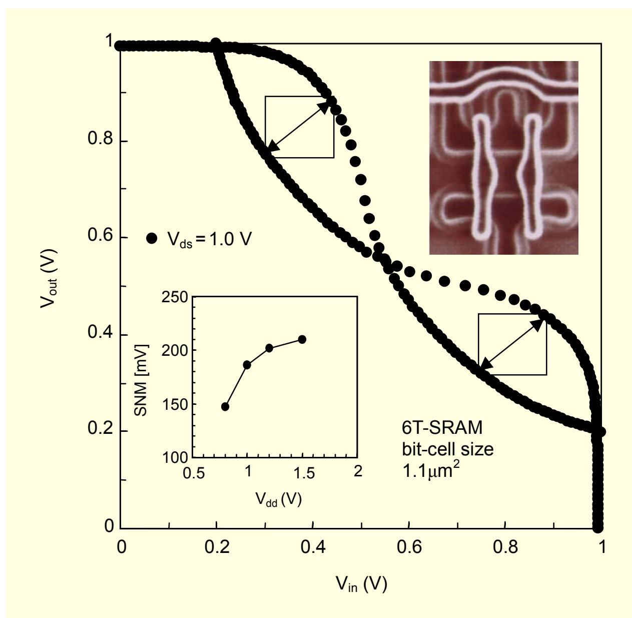


Fig. 10. Butterfly curves and static noise margin of a 1.1 $\mu m^2$ DR SOI 6T-SRAM cell.

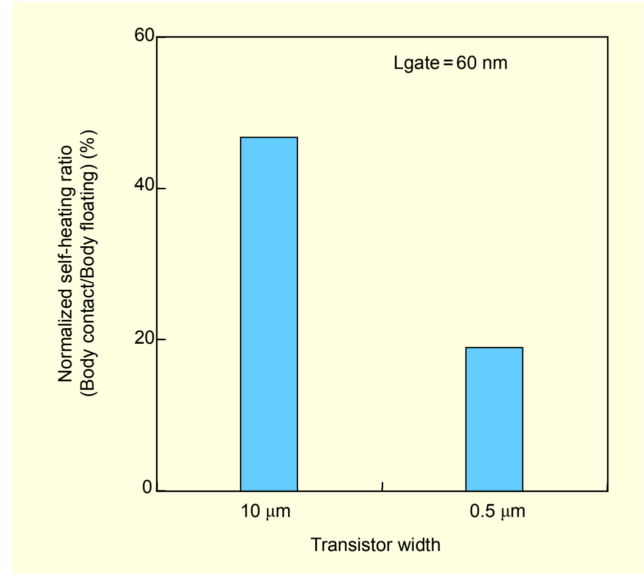


Fig. 12. Self-heating ratio vs. gate width.

and the sensitivity of the memory to process tolerances and operating conditions. The two aspects are interdependent since designing a cell for improved stability requires a larger cell area [12]. The SNM characteristics of a 1.1 $\mu m^2$ 6T SRAM cell show a highly stable butterfly curve with an SNM of 190 mV at $V_{dd}$ = 1.0V, as shown in Fig. 10. The SNM increases by 44% as $V_{dd}$ increases from 0.8 V to 1.5 V.

The method of measuring output current-voltage (IV) characteristics of an SOI CMOSFET by applying short pulses to the gate is employed to investigate the self-heating effect [4]. Using the pulsed IV technique with a low duty cycle, self-heating is avoided as the device is conducting only for a relatively short time. As a result, the measured AC drain current can be much greater than the measured DC, in which significant self-heating occurs. This explains the low DC transistor performance level of an SOI CMOS device. Figure 11 shows the self-heating ratio, defined as DC current over AC current, for the single and double raised S/D processes. As the gate length decreases, the self-heating ratio decreases and both the single and double raised S/D processes show a reduced self-heating effect on the body contact transistor due to the dissipation of the heat, when compared with the body floating transistor. As gate width

is decreased from 10 to 0.5 μm, the self-heating ratio of the body contact SOI device to body floating device also decreases from 46.7 to 19 %, as shown in Fig. 12.

The propagation delay is experimentally determined by constructing a ring oscillator with a larger and odd number of CMOS inverters. The ring oscillator delay time of DR S/D devices is improved by up to 25 % compared with that of bulk devices, and the delay time of DR S/D devices is comparable to that of SR S/D devices as shown in Fig. 13.

The analog characteristics of a DR S/D SOI device are investigated. Figure 14 shows that the DR S/D process has a higher open-loop voltage gain than the SR S/D process for both NMOS and PMOS. Noise characteristics of SOI devices are also evaluated as shown in Fig. 15, showing that the body contact transistor has better noise stability than the body floating transistor up to an SOI thickness of 35 nm. It is also shown that a 15 nm ultra-thin body (UTB) SOI device with a DR S/D process shows the same level of noise characteristics for both body contact and body floating transistors. Noise characteristics of DR S/D SOI devices are comparable to that of bulk devices.

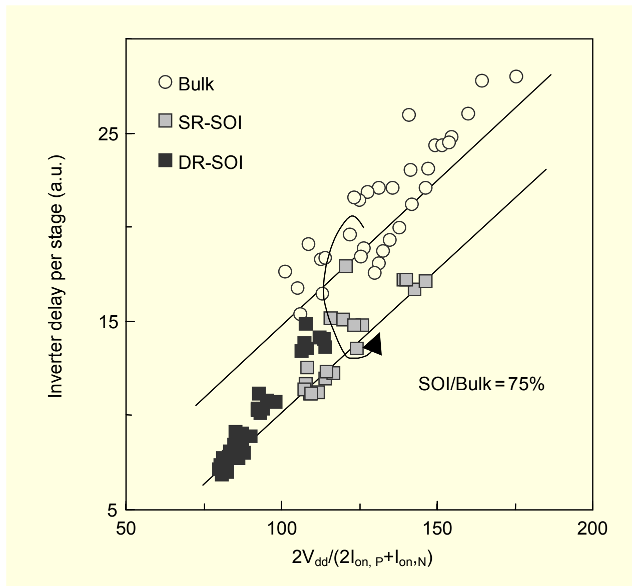


Fig. 13. Measured inverter delay of the ring oscillator.

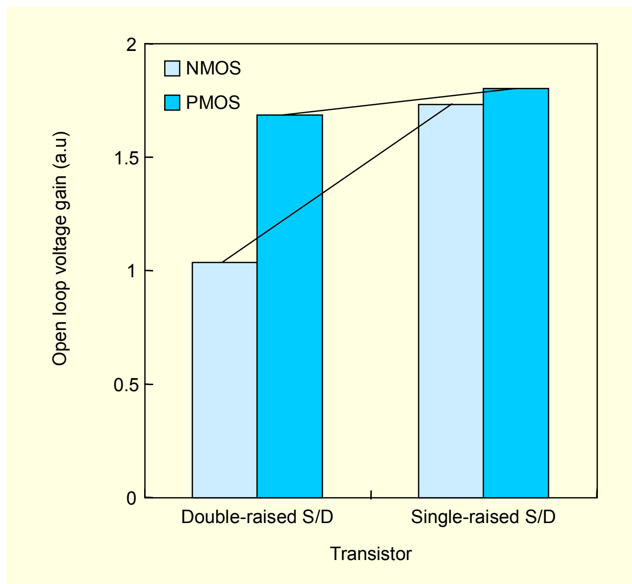


Fig. 14. Open-loop voltage gain.

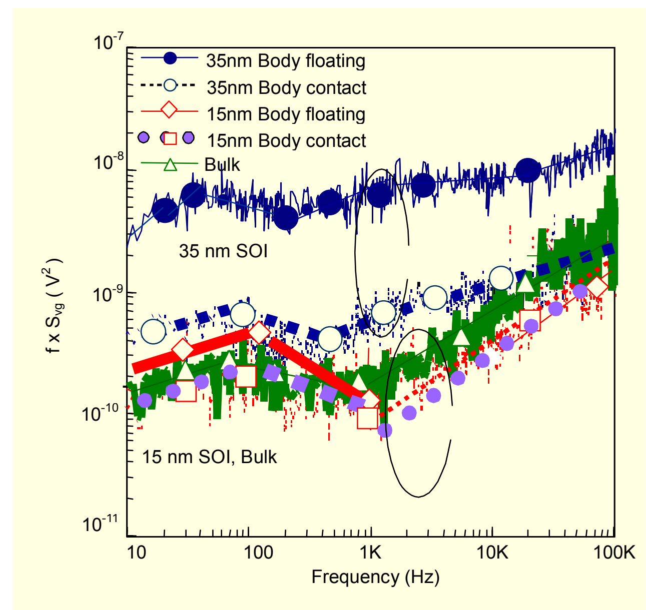


Fig. 15. Product of input referred gate noise power and frequency vs. frequency.

## IV. Conclusions

A 15 nm UTB SOI CMOS device with the optimized DR source/drain process for a 90 nm technology node is investigated in order to evaluate analog characteristics of SOI CMOS devices. Ultra-thin Si channel devices with a thickness of 15 nm and a gate length of 60 nm are fabricated. Both the single and double raised source/drain processes using an optimized Si-SEG process is investigated in order to reduce parasitic resistance and improve the saturation current. The DR S/D process shows a better profile than the SR S/D process because the first Si-SEG is applied before the source/drain extension ion implantation. Therefore, the DR S/D process should be used to grow the Si-SEG layer at a thickness of 15 nm. The DR source/drain process shows a better transistor performance than the SR source/drain process due to the lower series resistance, showing 8 and 18 % saturation current improvements for NMOS and PMOS, respectively. The self-

heating effect is evaluated for both a body contact and body floating SOI CMOS. The body contact SOI CMOS shows a reduced self-heating ratio, compared with the body floating SOI CMOS. The static noise margin characteristics of a 1.1 $\mu m^2$ 6T SRAM cell show a highly stable butterfly curve with an SNM of 190 mV at $V_{dd}$ = 1.0 V. The ring oscillator delay time of double raised S/D SOI devices is improved by up to 25 % compared with that of bulk devices. The DR S/D process has a higher open-loop voltage gain than the single SR S/D process for both NMOS and PMOS. Noise characteristics of SOI devices show that a 15 nm UTB SOI device with a DR S/D process shows the same level of noise characteristics at both body contact and body floating transistors. Also, we observed that noise characteristics of 15 nm DR S/D SOI devices are comparable to that of bulk devices. We conclude that 15 nm ultra thin body SOI CMOS devices with a DR source/drain process are suitable for analog applications.

## References


[1] T. Ohno, Y. Kado, M. Harada, and T.T. Tsuchiya, "Experimental 0.25-μm-Gate Fully Depleted CMOS/SIMOX Process Using a New Two-Step LOCOS Isolation Technique," *IEEE Trans. Electron Devices*, vol. 42, 1995, pp. 1481.

[2] T.C. Hsiao, N.A. Kistler, and J.C.S. Woo, "Modeling the I-V Characteristics of Fully Depleted Submicrometer SOI MOSFET's ," *Electron Device Lett.*, vol. 15, 1994, pp. 45.

[3] R. Chau, J. Kavalieros, B. Doyle, A. Murthy, N. Paulsen, D. Lionberger, D. Barlage, R. Arghavani, B. Roberds, and M. Doczy, "A 50 nm Depleted-Substrate CMOS Transistor (DST)," *Int. Electron Device Meet. Technical Digest*, 2001, pp. 62.

[4] K.A. Jenkins, J.Y.-C. Sun, and J. Gautier, "Characteristics of SOI FET's Under Pulsed Conditions," *IEEE Trans. Electron Devices*, vol. 44, 1997, pp. 1923.

[5] Y.C. Tseng, W.M. Huang, D. Monk, D. Diaz, J.M. Ford, and J.C.S. Woo, "Comprehensive Study on AC Characteristics in SOI MOSFETs for Analog Applications," *Symp. VLSI Tech. Dig.*, 1998, pp. 112.

[6] Hyeokjae Lee, Young June Park, Hong Shick Min, Jong Ho Lee, Hyungsoon Shin, Wookyung Sun, and Dae-Gwan Kang, "Effects of Shallow Trench Isolation on Silicon-on-Insulator Devices for Mixed Signal Processing," *J. Korean Phys. Soc.,* vol. 40, 2002, pp. 653.

[7] Y.W. Kim, J.H. Ahn, T.S. Park, C.B. Oh, K.T. Lee, H.S. Kang, D.H. Lee, Y.G. Ko, K.S. Cheong, J.W. Jun, S.H. Liu, J. Kim, J.L. Nam, S.R. Ha, J.B. Park, S.A. Song, and K.P. Suh, Symp. "Robust Process Integration of $0.78m^2$ Embedded SRAM with NiSi Gate and Low-K Cu Interconnect for 90 nm SoC Applications," *VLSI Tech. Dig.*, 2003, pp. 69.

[8] Y. Ono, M. Nagase, M. Tabe, and Y. Takahashi, "Thermal Agglomeration of Thin Single Crystal Si on $SiO_2$ in Vacuum," *Jpn. J. Appl. Phys.*, vol. 34, 1995, pp. 1728.

[9] M.H. Oh, C.H. Park, H.S. Kang, C.B. Oh, Y.W. Kim, and K.P. Suh, "Fully Depleted SOI CMOS Device with Raised Source/Drain for 90 nm Embedded SRAM Technology," *Solid State Devices and Materials*, 2003, pp. 756.

[10] Yongjae Lee, Youngshig Choi, and Jichel Bea, "A Novel Structure MOSFET's Fabricated by Using SiGe Selective Epitaxial Growth Method and Laser Induced Atomic Layer Doping Method," *J. Korean Phys. Soc.*, vol. 41, 2002, pp. 82.

[11] Dong-Soo Woo, Boo-Sik Park, Jong Duk Lee, and Byung-Gook Park, "Fabrication of a 0.2-μm Ultra-Thin SOI Inverted Sidewall Recessed Channel CMOS with Single-Type Polysilicon Gate," *J. Korean Phys. Soc.*, vol. 40, 2002, pp. 68.

[12] E. Seevinck, F.J. List, and J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE J. Solid-State Circuits*, vol. 22, 1987, pp. 748.

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